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REGULAR PAPER

A simple structure for noise-shaping SAR ADC in 90 nm CMOS technology

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ABSTRACT

This paper presents a simple structure for error feedback based noise-shaping successive approximation register (NSSAR) analog-to-digital converter (ADC), which obviates the need for a high output swing, fast-settling and high gain Operational Transconductance Amplifier (OTA). The ADC has a simple structure and its quantization noise is extracted and transferred via a finite impulse response (FIR) filter, without any attenuation. To make a good matching, a 5-bit segmented array is utilized as a digital-to-analog converter (DAC). In this way, the required total capacitance of the ADC is reduced more than 96% compared to a 10-bit conventional SAR (CSAR) ADC. Also, due to noise-shaping property the comparator specifications are relaxed. The ADC is designed and simulated in 90 nm CMOS technology with HSPICE simulator. Simulation results show that the ADC's average power consumption is about 4.4 μW at a 0.5 V power supply. By using an oversampling ratio (OSR) of 16, the ADC achieved maximum SNDR and SFDR of 59.6 dB and 58 dB, respectively, from transient noise simulation. The figure of merit (FoM) is about 56.4 fJ/conversion-step.

1. Introduction

Successive approximation register (SAR) ADCs are highly power-efficient data converters which are widely utilized in portable electronic devices and power management systems such as DC–DC converters. Although, this kind of ADC is a good candidate for the moderate-resolution and moderate-speed applications, achieving higher effective resolution is quite challenging, due to the limited accuracy of the SAR circuit blocks [1–6]. Most of SAR ADCs employ the binary weighted charge redistribution array as a digital-to-analog converter (DAC) block, such that the number of capacitors increases exponentially with respect to number of bits. Therefore, the accuracy of the ADC may be deteriorated due to poor matching of capacitor array. As a result, the value of the unit capacitor must be chosen large enough to meet the matching requirements. Besides, the DAC power consumption is also exponentially increased [7–9]. Also, decreasing the value of the least significant bit voltage ($V_{LSB} = V_{Full\text{-}scale}/2^{(Number\ of\ bit)}$) causes the meta-stability problem for the comparator. Therefore, to overcome latching error a power hungry pre-amplifier is needed to drive the comparator [9]. Moreover, in higher resolutions the ADC conversion time will be increased due to several cascaded blocks in digital section and the DAC *RC* time constant [10]. Digital calibration techniques are most popular ways to reduce the static and dynamic errors [11–13]. However, the complexity of the implementation and the converting procedure is raised as well as the overall power consumption.

Using the noise-shaping technique associated with oversampling is another techniques to improve the SAR ADC's performance in higher resolution [14–18]. However, due to a passive sampling plus the low feedback factor in [14] the modulator performance is degraded. The introduced structure in [15] is more sensitive to the circuit non-idealities such as the passive sampling and coefficients of the loop filter (which consists of a cascaded Infinite Impulse Filter (IIR) with FIR filter). The reported works in [16,17] introduce other noise-shaping ADCs, which are based on error feedback scheme [19] and obviates the need for high output swing and high-gain OTA. In [18], another structure was proposed to provide noise-shaping property by using only three capacitors. However, it suffers from the clocking complexity since six different clock phases (Φ_1–Φ_6) are required. Moreover, the simulation result of this structure is based on system level implementation and circuit non-idealities such as charge injection, clock feed-through and effect of parasitic capacitors are not considered.

In this paper, a simple structure for error feedback based noise-shaping SAR ADC is presented. The proposed ADC is straightforward in implementation and reduces the total number of capacitors while simultaneously relaxes the required OTA specifications.

The rest of the paper is as follows. Section 2, describes the architecture of the proposed NSSAR ADC. In Section 3, the circuit level

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design considerations of each building block are described. The simulation results of the proposed ADC and the comparison with several state-of-the-art ADCs are provided in Section 4. Finally, Section 5 concludes the paper.

2. Proposed architecture

2.1. Quantization error extracting

Fig. 1(c) shows the conceptual diagram of the proposed structure which is based on the error feedback scheme. In order to provide the noise-shaping in SAR ADC, the quantization error must be extracted first. Note that this step is carried out at the end of each conversion phase. As shown in Fig. 1(a), in [15] the quantization error is extracted by connecting a few capacitors to the DAC capacitors. Due to the charge sharing, the quantization error will be attenuated and the modulator performance is degraded. Also, the extracted error is transferred via several branches into the active adder, which increases the modulator sensitivity to mismatch of their coefficients. Note that the active adder is realized by an OTA in this scheme. Hence, the OTA requires a high gain-bandwidth product (GBW) due to lower feedback factor. The introduced structure in [16] is shown in Fig. 1(b). As is seen to provide an equivalent third-order noise-shaping, a cascade of FIR and infinite impulse response (IIR) filters are utilized in this scheme. Although the utilized OTA in this structure has a relaxed requirement because it drives small parasitic capacitors, but to avoid the instability resulting from the FIR filter coefficients, a specific range for the OTA gain is needed necessitating a careful circuit design. Fig. 1(c) illustrates the proposed method to exploit the quantization error. Unlike the previous works, the dummy capacitor of the DAC is used to extract and transfer the quantization error. In the next subsection, the method of extracting the quantization noise without attenuation will be explained.

2.2. Improved noise-shaping

The complete circuit level and timing diagram of the proposed structure is shown in Fig. 2. Similar to the conventional charge redistribution SAR ADC, the capacitor array serves as both the DAC and the sample & hold (S/H) circuit. But to make the noise-shaping, the difference between the input voltage and quantization error of previous sample is applied to the ADC's input at each sampling phase. Also, the conversion phase of this structure is same as the conventional type that uses the binary search algorithm to generate output digital bits. Fig. 3 shows an example of the proposed method for 4 bit binary weighted SAR ADC. The ADC operation is as follows: By assuming $\Phi_1 = 1$ and $\Phi_2 = 0$, the residue capacitors C_{r1} are connected to the DAC and act as dummy capacitors ($C_{r1,2} = C_u$) whereas the residue capacitors C_{r2} are connected to OTA inputs and transfer the previous quantization error (Fig. 3(a)). Note that the OTA acts as a unity gain buffer in closed loop configuration. Once the sampling phase starts, the bottom-plate of all capacitors excluding the residue capacitors C_{r2}, are connected to input voltage whereas their top-plate are connected to previous quantization error through the OTA. So, the capacitor array samples the difference of the

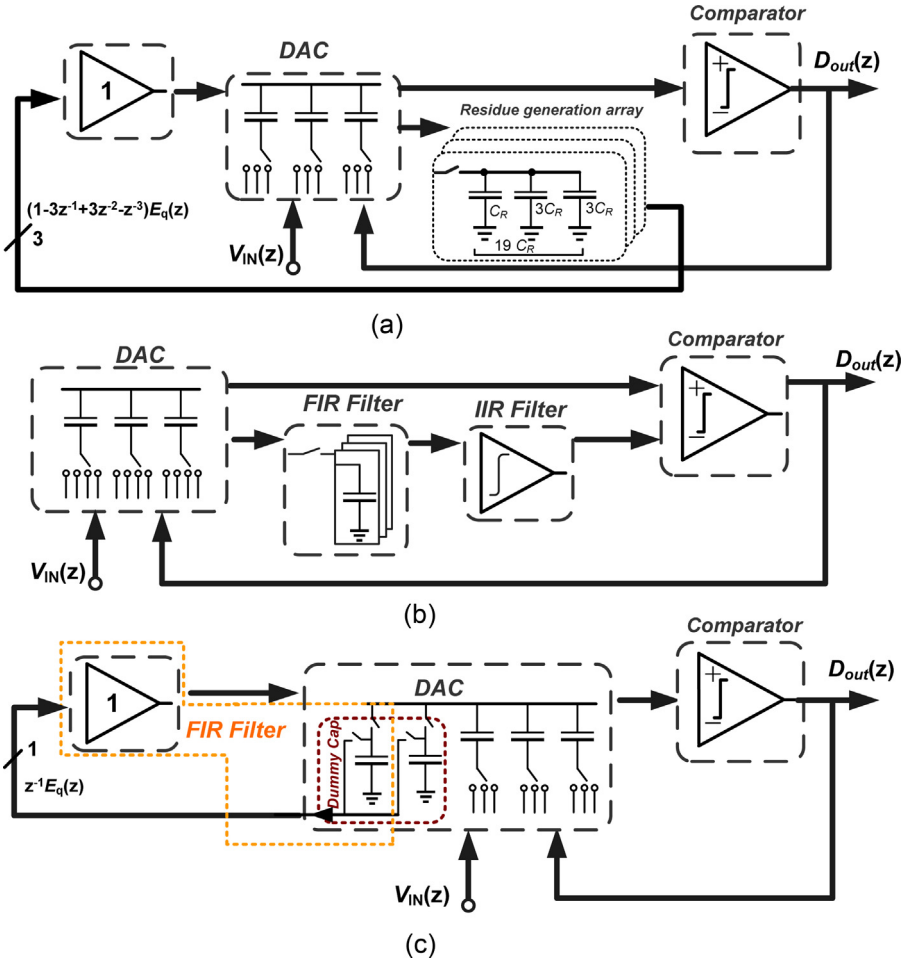

Fig. 1. Quantization error extracting (a) structure of [14], (b) structure of [15] and (c) proposed method.

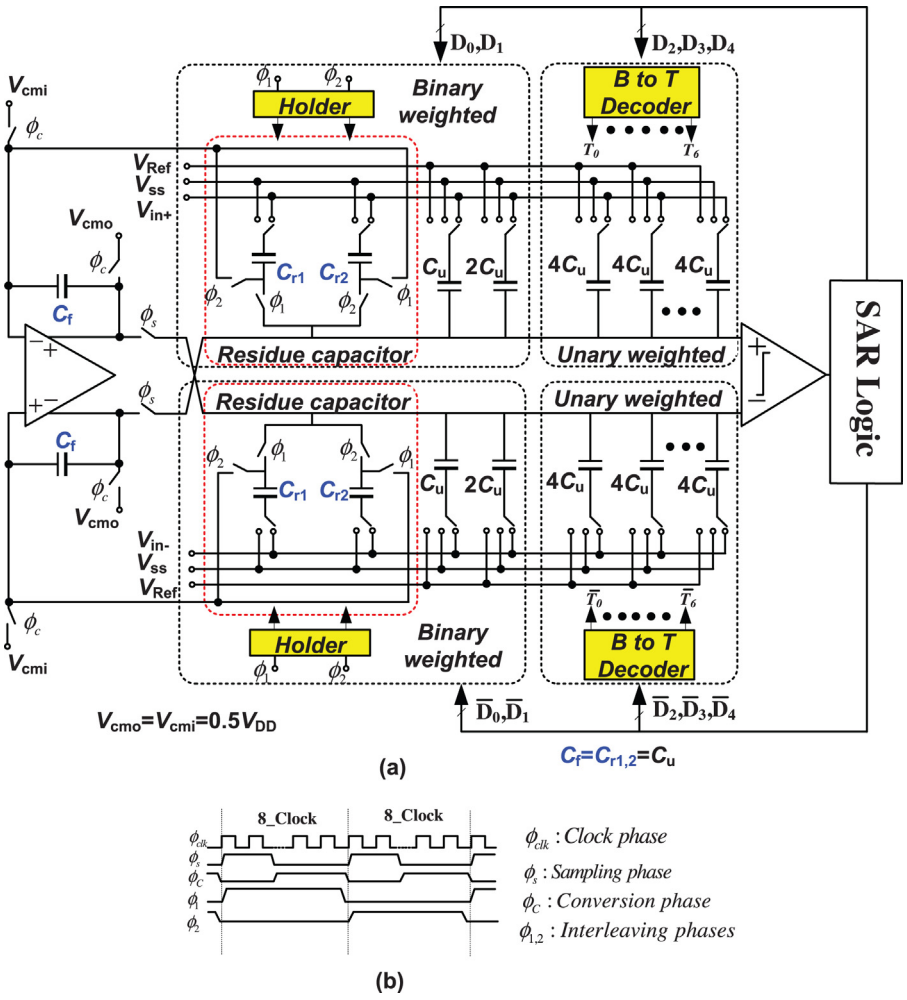

Fig. 2. (a) Complete schematic of proposed structure (b) timing diagram.

previous quantization error and input voltage. Note that this capacitor will contain quantization error as long as its bottom plate voltage stays unchanged. Therefore, an additional *D*-latch (Holder) is used to maintain its bottom plate voltage during next interleaving phase (i.e. during Φ_1 for C_{r2} and during Φ_2 for C_{r1}). When the conversion phase (Φ_c) begins, the OTA is disconnected from DAC capacitors and the feedback capacitor, C_f ($C_f = C_u$) is reset to avoid accumulation. The OTA is idle during this phase, thus to save more power, it can be turned off. The digital control logic performs the binary search algorithm and changes the bottom-plate voltage of capacitors until the sampled voltage is approximated (Fig. 3(b)). Before beginning the next sampling phase, the interleaving phase Φ_2 goes high and the residue capacitors role is changed. Therefore, the residue capacitors C_{r2} are connected to DAC capacitors while C_{r1} transfers the previous quantization error via the OTA. Thereafter, the next sampling phase is started and the bottom-plate of the capacitors (excluding C_{r1}) is connected to the input voltage while their top-plate is connected to the previous quantization error (Fig. 3(c)).

Note that at the end of the conversion phase, the V_{DAC} voltage (i.e. $V_{DAC+} - V_{DAC-}$) is given by:

$$V_{DAC}[n] = e_q[n-1] - V_{in}[n] + \sum_{i=0}^{m-1} D_i[n] \frac{V_{Ref}}{2^{m-i}} \quad (1)$$

where $e_q[n-1]$ (i.e. $e_{q+}[n-1] - e_{q-}[n-1]$) is the quantization error of the previous sample which is differentially stored in the residue capacitors, $V_{in} = V_{in+} - V_{in-}$, and the summation expresses output bits of the SAR logic in the analog form. On the other hand, the value of the quantization error of the present sample is given by (in differentially mode):

$$V_{DAC}[n] = e_q[n] \quad (2)$$

By situating the relation (2) into (1), the following relation is obtained:

$$e_q[n] - e_q[n-1] = -V_{in}[n] + \sum_{i=0}^{m-1} D_i[n] \frac{V_{Ref}}{2^{m-i}} \quad (3)$$

where the term $e_q[n] - e_q[n-1]$ represents a first-order noise-shaping. In other words, the equivalent analog output of the ADC, V_{out}, at the end of the conversion phase is given by:

$$V_{out}[n] = V_{in}[n] + e_q[n] - e_q[n-1] \quad (4)$$

It is clear that, the input signal directly appears at the output. So the signal transfer function is equal to 1 (STF(z) = 1) while the quantization error is first-order shaped which means the noise transfer function is equal to $1 - z^{-1}$ (NTF(z) = $1 - z^{-1}$). Note that in this calculation we assume a unity gain for the close loop configuration. However the finite open loop dc gain (A_v) decreases the closed-loop gain as $G = 1 - 1/A_v$ and changes the NTF to $1 - G \times z^{-1}$. So the finite open loop gain moves the noise transfer function (NTF) zero of the ADC from $z = 1$ to inside of the unit circle in z-plane whereas the location of the pole is not changed. This increases the in-band

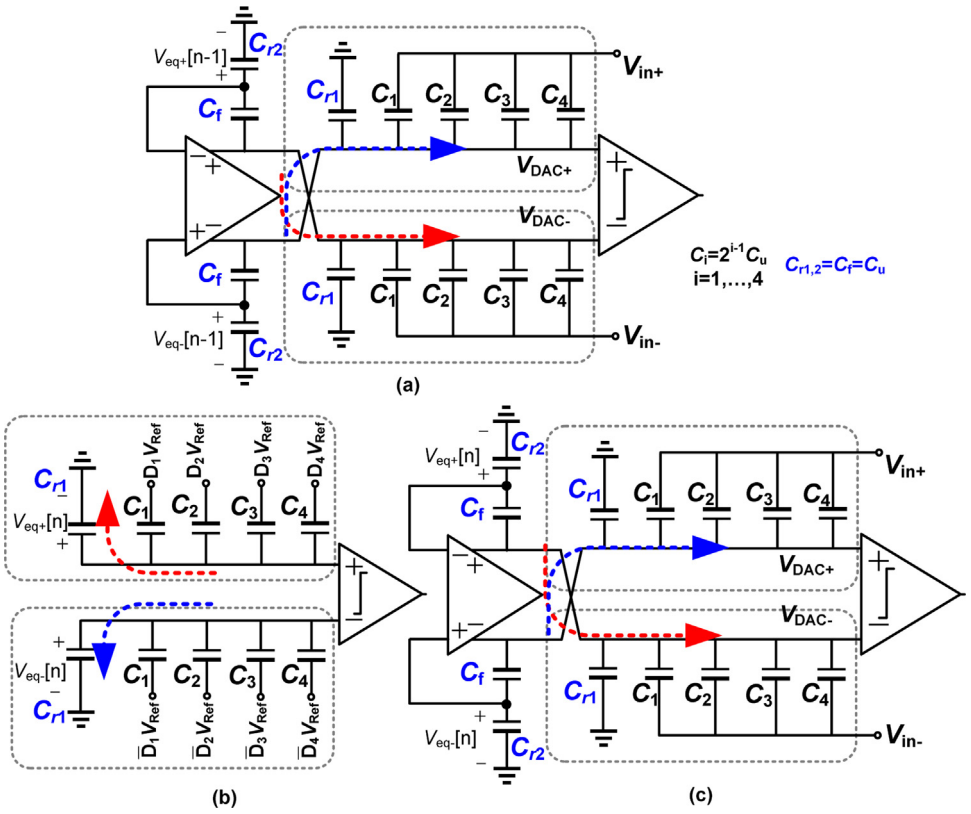

Fig. 3. Example of the proposed structure for 4bit binary weighted SAR ADC (a) sampling phase, (b) end of conversion phase and (c) next sampling phase.

quantization noise and may degrade the ADC's accuracy. According to the behavioral simulation a signal-to-quantization noise ratio (SQNR) more than 63 dB is achieved when the OTA dc gain is as low as 10 dB.

Briefly, by using the above mentioned method, the first order of noise-shaping is provided without any attenuation. Since the quantization error is transferred only by using the dummy capacitors of the DAC, the *GWB* requirement for the OTA is alleviated.

3. Circuit Implementation

Due to the trade-off between the area occupation, power consumption, accuracy and conversion rate, the ADC can be realized by different number of bits of DAC and oversampling ratios (OSRs). Note that, utilizing a higher resolution quantizer increases the area occupation as well as the power consumption of the capacitor array with respect to the number of bits. However, it obviates the need for large output swing of the OTA and also enhances the ADC dynamic range due to small value of the quantization error. On the other hand, the oversampling ratio is another parameter which affects the ADC's accuracy and the conversion rate. Therefore, based on behavioral system simulation results, it is found that the system can provide the maximum SQNR of 63 dB by using 16X OSR and a 5 bit quantizer. The ADC is designed to achieve SQNR up to 63 dB.

The fully-differential configuration is chosen in the circuit level implementation, due to both better common-mode rejection and distortion performance. The OTA structure and the switch implementations are similar to [17].

3.1. Capacitor array and linearity issue

The key parameter in the capacitor array is the unit capacitor (C_u), because the ADC area occupation, power consumption and also linearity are dependent on the unit capacitor value. The unit capacitor value is determined from the capacitor matching consideration, the kT/C noise and design rules of utilized technology [7]. Usually the maximum standard deviation of differential nonlinearity error (DNL) is used for matching requirement evaluation [20]. To meet the matching requirement with small unit capacitor, the capacitor array is implemented by a segmented DAC (i.e. 2 bit binary weighted and 3 bit unary weighted). Since only one capacitor is changed in the unary weighted capacitor array during each bit cycle, the worst case for the DNL, may occur at transition from 000000011 (V_{DAC1}) to 000000100 (V_{DAC2}). In order to estimate the standard deviation of capacitor mismatch, the voltage V_{DAC} must be calculated by considering the capacitor mismatch. Note that in ideal case, the value of the voltages V_{DAC1} and V_{DAC2} is obtained from Eqs. (5) and (6), respectively and V_{DAC} is equal to the V_{LSB} voltage:

$$V_{DAC(00\ldots011)} = V_{DAC1} = \frac{3C_u}{32C_u}V_{Ref} \tag{5}$$

$$V_{DAC(00\ldots0100)} = V_{DAC2} = \frac{4C_u}{32C_u}V_{Ref} \tag{6}$$

$$V_{DAC} = V_{DAC2} - V_{DAC1} = \frac{4C_u - 3C_u}{32C_u}V_{Ref} = V_{LSB} \tag{7}$$

On the other hand, by assuming the standard deviation of the unit capacitor $\Delta C_u (C_u = C_u + \Delta C_u)$, the standard deviation of V_{DAC} can be approximated as:

$$\begin{aligned} &C_u = C_u + \Delta C_u \quad \Rightarrow \quad (V_{DAC})_{std} = V_{DAC2} - V_{DAC1} \\ &= \frac{4(C_u + \Delta C_u) - 3(C_u + \Delta C_u)}{32(C_u + \Delta C_u)}V_{Ref} \\ &= \frac{4C_u + \sqrt{4}\Delta C_u - 3C_u - \sqrt{3}\Delta C_u}{32C_u + \sqrt{32}\Delta C_u}V_{Ref} \approx \frac{C_u + \left(2 - \sqrt{3}\right)\Delta C_u}{32C_u}V_{Ref} \end{aligned} \tag{8}$$

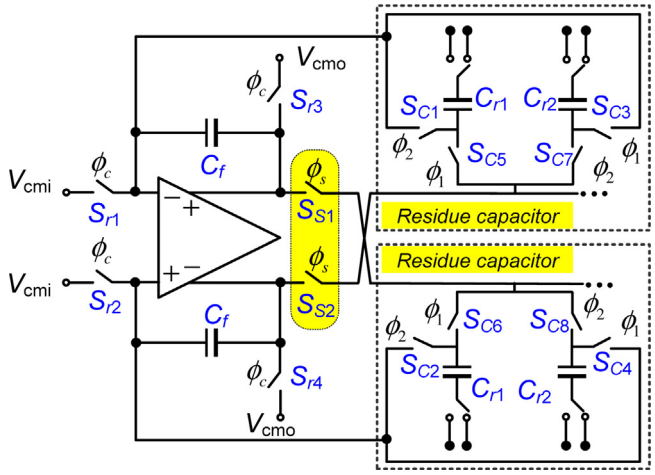

Fig. 4. Equivalent circuit for analyze the thermal noise of the FIR filter switches.

As a result we obtain:

$$V_{\mathrm{DNL,std}} = V_{\mathrm{DAC,Ideal}} - V_{\mathrm{DAC,std}} = \left(\frac{C_u + \left(2-\sqrt{3}\right)\Delta C_u}{32C_u} - \frac{1}{32}\right) V_{\mathrm{Ref}} = \frac{\left(2-\sqrt{3}\right)\Delta C_u}{32C_u} V_{\mathrm{Ref}} \tag{9}$$

$$\Rightarrow \quad 3 \times V_{\mathrm{DNL,std}} < \frac{V_{\mathrm{LSB}}}{2} \Rightarrow \quad \frac{\Delta C_u}{C_u} < 1\%$$

Therefore, for various targeted accuracy, different values are obtained for the $\Delta C/C$. For example in relation (9), to meet 11 bit accuracy the value of $\Delta C/C$ must be less than 1% which corresponds to a 12 fF capacitance in utilized technology. Besides, to determine the value of unit capacitor from the thermal noise consideration, the on-resistance of the switches should be taken into consideration as the sources of thermal noise. For the sake of simplicity, it is assumed that there is no correlation between the thermal noise sources. Thus, during the sampling phase the kT/C noise of capacitor array can be approximated as:

$$\overline{V}^2_{n,\mathrm{DAC}} \approx \frac{kT}{32C_u} \tag{10}$$

where k is the Boltzmann constant and T is the temperature in Kelvin. For thermal noise analysis of the FIR filter switches (S_{C1-8} and $S_{S1,2}$ switches), the illustrated equivalent circuit in Fig. 4 is used. By assuming infinite open loop dc gain for OTA, the worse case thermal noise will be:

$$\overline{V}^2_{n,\mathrm{FIR}} \approx \frac{kT}{C_u} + \frac{kT}{C_u} = 2\frac{kT}{C_u} \tag{11}$$

The first term in this relation is the kT/C noise of the previous sample which is transferred to the output like the quantization error. The second term indicates the thermal noise of the switches connected to inputs of OTA when the interleaving phases going to be changed (i.e. $S_{C1,2}$ when Φ_2 going to high and $S_{C3,4}$ when Φ_1 going to high). Due to the oversampling property, only a fraction of noise falls in band of interest. Hence, for fully differential mode the total kT/C in ADC's input can be approximated as follows:

$$\overline{V}^2_n = \frac{\overline{V}^2_{n,\mathrm{switch}} + \overline{V}^2_{n,\mathrm{DAC}}}{\mathrm{OSR}} \approx \frac{2}{16}\left[2 \times \frac{kT}{C_u} + \frac{kT}{32C_u}\right] \tag{12}$$

It is clear that the contribution of the FIR filter noise in overall kT/C noise is dominant. From the thermal noise consideration, the value of C_u is obtained about 25 fF. Note that, from the reported relations in [7], the value of unit capacitor for a 10-bit CSAR ADC is obtained more than 30 fF, according to the matching requirement

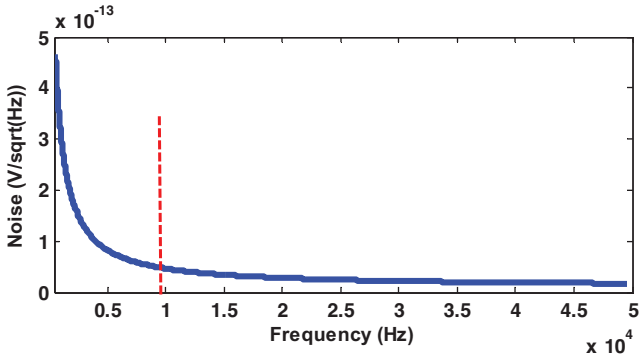

Fig. 5. OTA noise characteristic curve.

(in similar technology). Although, the minimum value of the metal-insulator-metal (MIM) capacitance in the used process is about 49 fF, the unit capacitor with the chosen value can be implemented in custom designed form.

In FIR filter noise calculation, the contribution of the flicker noise is ignored. But to estimate the value of the flicker noise, the mean square value of the OTA noise is simulated. As is shown in Fig. 5, the in-band (200 Hz to 50 kHz) mean square value flicker noise is about $2.04 \times 10^{-9}\ V^2$ whereas the signal power is $120 \times 10^{-3}\ V^2$ resulting in the signal to flicker noise ratio of 77.7 dB. Thus the flicker noise effect is negligible.

From the above, it can be concluded that in spite of relaxed matching requirement, the thermal noise of the FIR filter switches impose a large unit capacitor to the DAC. Although, increasing the oversampling ratio will obviate the thermal noise consideration, it complicates the decimation filter implementation.

Note that, the drawn charge from reference voltage in the segmented DAC is less than the conventional binary weighted DAC and it can be calculated as relation (13) at each clock cycle:

$$Q_1 = C_{s1}\left[V_{\mathrm{Ref}} - V_{\mathrm{DAC1}}\right]$$

$$Q_2 = \frac{C_{s1}}{2}\Delta V_{\mathrm{DAC2}} + D_4\left[C_{s2}\left(V_{\mathrm{Ref}} + \Delta V_{\mathrm{DAC2}}\right) + \frac{C_{s1}}{2}\Delta V_{\mathrm{DAC2}}\right]$$

$$Q_3 = \frac{C_{s1}}{4}\Delta V_{\mathrm{DAC3}} + (D_3 + D_4)\frac{C_{s1}}{2}\Delta V_{\mathrm{DAC3}} + D_4\left(\frac{C_{s1}}{4} + \frac{C_{s2}}{2}\right)\Delta V_{\mathrm{DAC3}} + D_4 D_3 \frac{C_{s2}}{2}\Delta V_{\mathrm{DAC3}} + D_4 D_3 C_{s3}\left(V_{\mathrm{Ref}} + \Delta V_{\mathrm{DAC3}}\right)$$

$$\begin{aligned} Q_4 = {} & \left[\frac{C_{s1}}{4}(D_2 + D_3 + D_4) + \frac{C_{s1}}{4}(D_3 + D_4) + \frac{C_{s1}}{4}(D_2 D_3 + D_4) + \frac{C_{s1}}{4}(D_4)\right. \\ & \left. + \frac{C_{s2}}{2}\left((D_3 + D_4)D_2 + (D_3 D_4)\right) + D_2 D_3 D_4 C_{s3}\right]\Delta V_{\mathrm{DAC4}} + C_{s4}\left(V_{\mathrm{Ref}} + \Delta V_{\mathrm{DAC4}}\right) \\ Q_5 = {} & \left[\frac{C_{s1}}{4}(D_2 + D_3 + D_4) + \frac{C_{s1}}{4}(D_3 + D_4) + \frac{C_{s1}}{4}(D_2 D_3 + D_4) + \frac{C_{s1}}{4}(D_4) + \right. \\ & \left. \frac{C_{s2}}{2}\left((D_3 + D_4)D_2 + (D_3 D_4)\right) + D_2 D_3 D_4 C_{s3} + D_1 C_{s4}\right]\Delta V_{\mathrm{DAC5}} + C_{s5}\left(V_{\mathrm{Ref}} + \Delta V_{\mathrm{DAC5}}\right) \end{aligned} \tag{13}$$

where $C_{si} = (2^{5-i})C_u$, $V_{\mathrm{DACi}} = V_{\mathrm{Ref}}/2^i$ and ΔV_{DACi} is equal to $V_{\mathrm{DACi-1}} - V_{\mathrm{DACi}}$ (i.e. i=1,2,3,4,5). In the utilized capacitor array, the maximum drawn charge from V_{Ref} will occur in down transitions (when the output bits are zero):

$$Q_{\mathrm{total\text{-}down}} = Q_{1-\mathrm{down}} + \cdots + Q_{5-\mathrm{down}} = \frac{441}{32}C_u V_{\mathrm{Ref}} \tag{14}$$

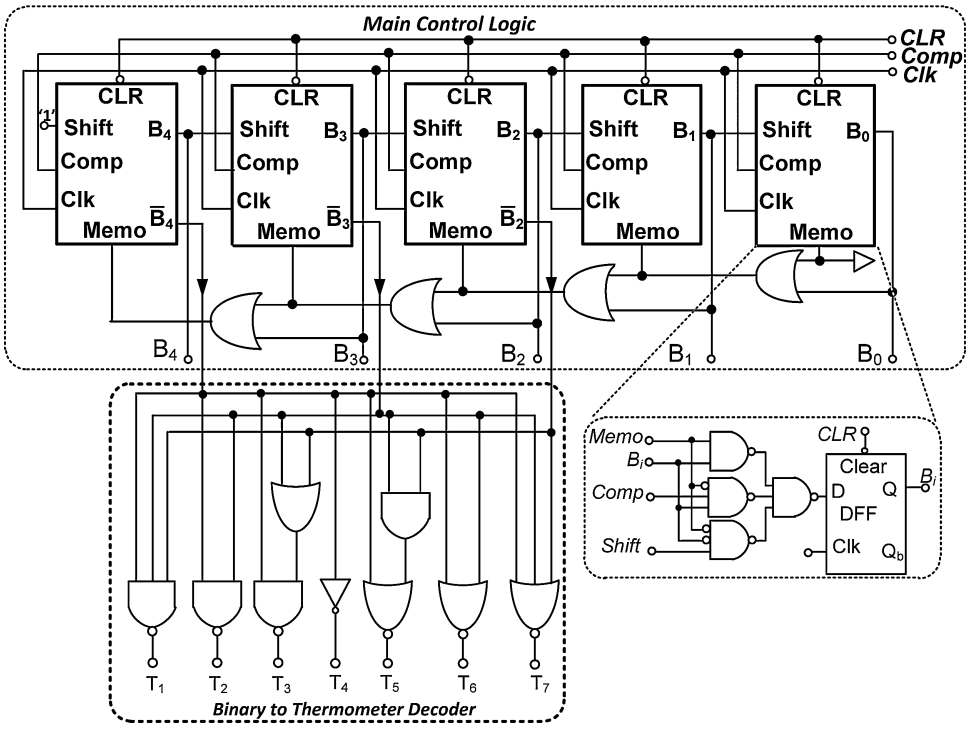

Fig. 6. Digital control logic.

According to [10], the power consumption of the reference voltage supply due to capacitor switching for an m—bit SAR-ADC can be written as:

$$P_{V_{\mathrm{Ref}}} = \frac{f_{clk}}{m+1} V_{\mathrm{Ref}} \sum_{i=1}^{m} Q_i \tag{15}$$

where f_{clk} is the clock frequency. Substituting (14) in (15), gives the worst case power consumption $\left(P_{V_{\mathrm{Ref,NS}}}\right)$ in the utilized segmented DAC.

$$P_{V_{\mathrm{Ref}}} = \frac{f_{clk,\mathrm{NS}}}{k+1} \times \left(\frac{441}{32}\right) C_{u,\mathrm{Ns}} V_{\mathrm{Ref}}^2, \qquad k = 5 \tag{16}$$

On the other hand the worst case power consumption of the 10-bit CSAR ADC $\left(P_{V_{\mathrm{Ref,C}}}\right)$ is approximated as:

$$P_{V_{Ref,C}} = \frac{2^N f_{clk,c} C_{u,c}}{N+1} \times \left\{\left(\frac{5}{6}\right) - \left(\frac{1}{2}\right)^N - \frac{1}{3}\left(\frac{1}{2}\right)^{2N}\right\} V_{Ref}^2, \quad N = 10 \tag{17}$$

By assuming the similar value for the both unit capacitor of NSSAR and CSAR and by considering that the $f_{clk,NS}$ is OSR times of $f_{clk,C}$, the ratio of the $P_{V_{\mathrm{Ref,NS}}}$ to $P_{V_{\mathrm{Ref,C}}}$ is approximately:

$$\frac{P_{V_{\mathrm{Ref,NS}}}}{P_{V_{\mathrm{Ref,C}}}} \approx \frac{2.3 \times \mathrm{OSR}}{77} \approx 0.48 \tag{18}$$

Despite the increase in the clock frequency due to OSR, the power that the reference voltage source supplies into the capacitor array is minimized by utilizing the segmented structure for the DAC. Note that the overall power consumption of NSSAR ADC will be more than CSAR ADC due to higher power dissipation of the analog part (OTA). But, since the 5 large capacitors are omitted in NSSAR ADC DAC, the required total capacitance of the ADC is reduced more than 96% compared to 10-bit CSAR ADC.

3.2. Comparator structure

The noise-shaping advantage is that the input-referred offset and noise of the comparator are shaped similarly to the

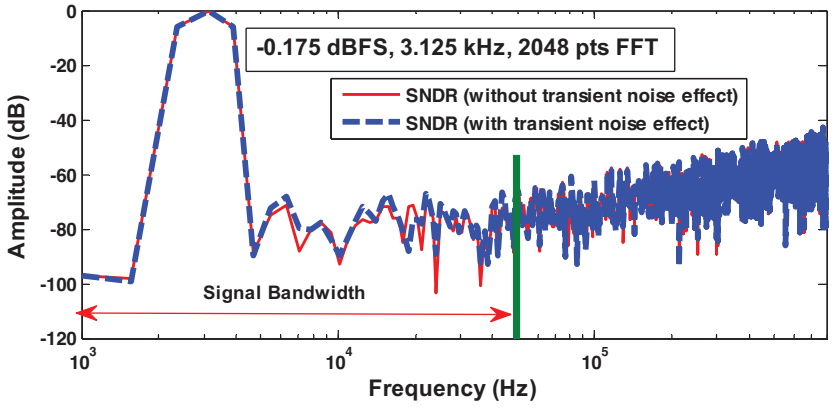

Fig. 7. Output spectrum of ADC (TT @ 27 °C).

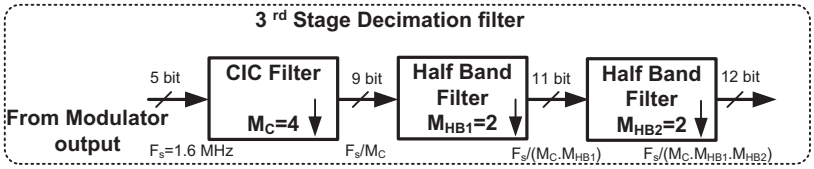

Fig. 8. Decimation filter structure.

quantization noise. Hence, the comparator requirement is relaxed. The introduced structure in [21] is utilized in the proposed ADC. The comparator is comprised of a preamplifier and the latch stage. Since, the input voltage of the comparator is around the input common mode voltage, the n-type input preamplifier is used in this design. Also, to reduce the parasitic capacitances and also power consumption, the minimum size transistors are employed in this comparator. The minimum voltage that the comparator must resolve is equal the least significant bit voltage (V_{LSB}) which is less than 16 mV in this case. Based on, the overdrive recovery test it is found that the comparator can detect the 1 mV input signal difference. The clock frequency of this simulation is chosen to be 12.8 MHz which is equal to the master clock frequency of the ADC. Also, the worst case delay of the simulated comparator is less than 0.57 ns.

3.3. Digital control logic

Fig. 6 shows the schematic diagram of digital control logic which uses a non-redundant structure [22] to generate the necessary controlling signals of the comparator and switches of the capacitor array. As is seen this block is comprised of 5 multiple internal shift registers and an additional binary to thermometer decoder to drive the bottom-plate of the unary weighted capacitors array. This decoder converts the 3 most significant binary bits to the 7 thermometer bits. The internal structure of each shift register consists of the D flip-flop to save the comparator decision and the decoder-multiplexer.

4. Simulation results

To compare the proposed structure with previous works, the ADC with 16X OSR, 50 kHz input bandwidth and 5-bit charge redistribution capacitor array is designed and simulated in 90 nm CMOS process. In order to evaluate the performance of the proposed ADC, the fast Fourier transform (FFT) analysis for 2048 data points is performed and the signal to noise and distortion ratio (SNDR) of the ADC is calculated. Resulting output spectrum with a Hann window for $a-0.175$ dBFS input range, 3.125 kHz sine wave input and 50 kHz signal bandwidth is shown in Fig. 7. The mismatch between the residue capacitor, C_{r1} and C_{r2}, may affect the quantization error as well as the SNDR. So by assuming 2%

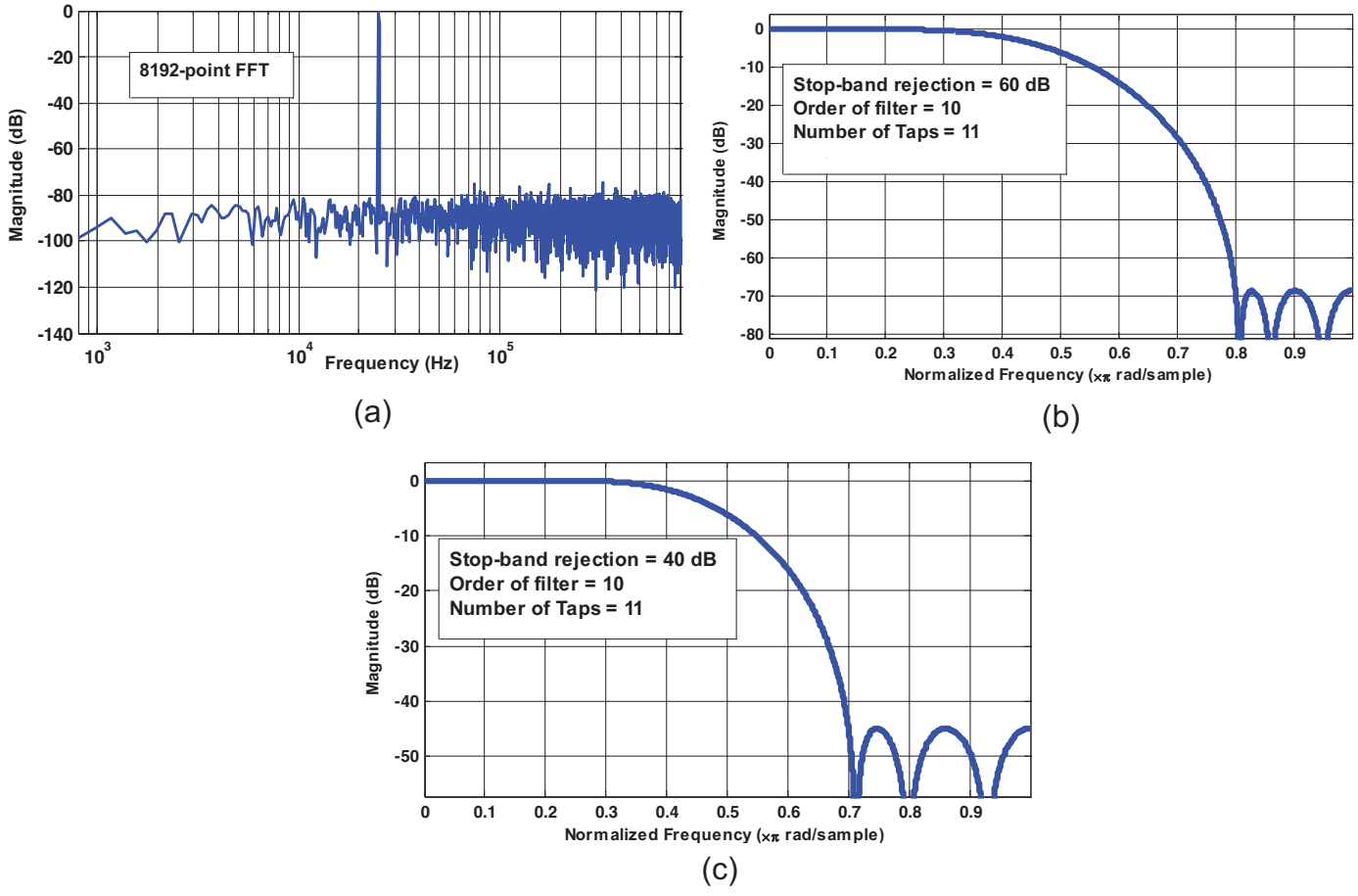

Fig. 9. (a) Output spectrum with decimation filter and (b) frequency response of first half-band filter (c) and the second half-band filter.

mismatch between the residue capacitor it is found that the mismatch degrades the SNDR by 0.39 dB. As a result, this SNDR degradation leads to a loss of 0.065-LSB. According to the relation (12), the mean-square value of the overall kT/C noise of the ADC is about $42 \times 10^{-9}\ V^2$ (in-band fully differential noise) whereas the signal power is $120 \times 10^{-3}\ V^2$ and the quantization noise power is about $71 \times 10^{-9}\ V^2$. Therefore, by considering all noise effect, the realistic SNDR of the ADC is obtained about 60.23 dB. To verify the validation of this calculation the transient noise analysis was performed for proposed ADC. Since this type analysis shows the effect of noise on the signal magnitude, it can be a good estimate for the noise circuit. The resulted SNDR from transient noise simulation is obtained 59.6 dB which is smaller than the value calculated by relation (12). The reason is that, in this calculation the effect of the parasitic capacitors as well as the jitter is not considered. Also, according to this simulation result, the SFDR of the ADC is near to 68 dB, which implies that proposed structure has a good linearity performance.

From the Hspice simulation results, the average power consumption of the proposed ADC for a 0.5 V single power supply is less than 4.4 μW. The simulated ADC performance in different process corner cases and the contribution of each part of the ADC in total power consumption (without transient noise effect) is summarized in Table 1. The following figure-of-merit (FoM) is used to compare the simulated ADC performance with several recently reported low-power SAR ADCs:

$$\text{FoM} = \frac{\text{Power}}{2 \times \text{BW} \times 2^{\text{ENOB}}} \tag{19}$$

Table 1
Performance summary of the simulated NSSAR ADC by adding the circuit noise from theoretical calculation.

Parameter	TT @ 27°C	SS @ 85°C	FF @ -40°C
SNDR	60.23 dB	57.6 dB	62 dB
SFDR	71 dB	69.5 dB	73 dB
ENOB	9.72 bit	9.28 bit	10 bit
ADC Power dissipation			
Comparator	60.5 nW	59 nW	58 nW
DAC	410 nW	321 nW	328.5 nW
FIR Filter	3.57 μW	3.72 μW	3.36 μW
Digital Logic	365 nW	293 nW	426 nW
Total power consumption	4.4 μW	4.39 μW	4.17 μW
Sampling rate	1.6 MHz		
Oversampling ratio	16		
Signal bandwidth	50 kHz		
Supply voltage	0.5 V		
Technology	90 nm CMOS		

Table 2 provides a comparison of this work with the current state-of-the-art low power SAR ADCs. Note that, the reported FoM in Table 2 is obtained by considering the transient noise effect. This FoM is calculated excluding the power consumption of the decimation filter and it is somewhat large in comparison with some recent works, but note that the proposed structure has a relaxed

Table 2
Performance comparison of the simulated ADC with several recently reported low-power SAR ADCs.

Reference	Process	DAC Resolution	Sampling Rate	Supply (V)	Input range	Power consumption	SNDR (dB)	ENOB (bit)	FoM (fJ/c-s)
TCAS II'12 [4]	0.35 μm	10 bit	100 kS/s	2	2 Vp-p	1 mW	60	9.67	-
JSSC'12 [7]	0.13 μm	10 bit	1 kS/s	0.4 ,1	1 Vp-p	53 nW	57	9.1	94.5
JSSC'12 [8]	0.18 μm	10 bit	200 kS/s	0.6	1 Vp-p	1.041 μW	57.46	9.34	8.03
JSSC'07 [9]	0.18 μm	12 bit	100 kS/s	1	1 Vp-p	25 μW	65.3	10.55	165
AICSP'10 [13]	0.18 μm	12 bit	100 kS/s	1.8	2.4 Vp-p	579.6 μW	68.74	11.13	2590
JSSC'12 [15]	65 nm	8 bit	90 MS/s	1	-	806 μW	62	10 t	35.7
AICSP'13 [16]†	90 nm	-	2 GS/s	1.2	1.2 Vp-p	9.58 mW	64	10.34	159
AICSP'13 [17]†	90 nm	8 bit	800 kS/s	0.5	rail-to-rail	4.53 μW	66.08	10.68	27.6
CTA'12 [20]	0.35 μm	10 bit	2 kS/s	1	rail-to-rail	130 nW	58.40	9.4	96
ISCAS'09 [24]†	0.13 μm	10 bit	100 kS/s	1	1 Vp-p	1 μW	57	9.17	17
ISSCC'11 [25]	65 nm	10 bit	20 kS/s	0.55	-	206 nW	55	8.85	22.4
ISCAS'11 [26]†	90 nm	10 bit	1 MS/s	1	1 Vp-p	7 μW	57.14	9.2	11.9
ISCAS'12 [27]†*	0.18 μm	8 bit	16 kS/s	1.2	-	450 nW	49.9	8	132
NEWCAS'12 [28]†	0.18 μm	9 bit	25 kS/s	1	-	160 nW	53	8.51	17
This work†	**90 nm**	**5 bit**	**1.6 MS/s**	**0.5**	**0.49 Vp-p**	**4.4 μW**	**59.6**	**9.6**	**56.4**

[a] Simulation results.

anti-aliasing filter and reduces considerably the required total capacitance in comparison to other higher resolution SAR ADCs. Furthermore, to make a fair comparison this issue must be considered. Although the decimation filter is not considered in circuit level implementation, the required architecture for the designed prototype is modeled in MATLAB and Simulink. Based on required specifications of each application, the decimation filter architecture is different [23]. In our design, to further reduce the overall power consumption, a multistage configuration is used which comprises a 2^{end} order Sinc filter (as Cascaded Integrator Comb filter) and two half-band filters by order of 10 (Fig. 8). The resulting output spectrum of the ADC (after the decimation filter) and the frequency response of half-band filters is shown in Fig. 9. By using this architecture for the decimation filter, the ADC SQNR is degraded about 0.3 dB. Thus, the out band quantization noise of proposed structure can be removed with employing a simple structure decimation filter.

5. Conclusions

A simple structure for error feedback based noise-shaping SAR ADC was presented in this paper. The first order noise-shaping property was provided by using a single stage OTA and some switch which act as FIR filter. In proposed structure the quantization error was extracted and transferred by using only the dummy capacitor of the 5-bit segmented DAC which was done without any attenuation. Also, the required total capacitance of the ADC was reduced more than 96% compared to the conventional 10 bit SAR ADCs.

From the simulation results, the maximum SFDR of the ADC is obtained 58 dB for −0.175 dBFS input level, which implies that the proposed structure has a good linearity. The proposed ADC is designed and simulated in 90 nm CMOS technology with 0.5 V single power supply. Hspice simulation results show that the average power consumption of the ADC is about 4.4 μW (by turning off the OTA in the conversion phase) and achieves the maximum SNDR of 59.6 dB, resulting in a FoM of 56.4 fJ/conversion-step.

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