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AN EFFICIENT LOW-POWER SIGMA-DELTA MODULATOR FOR MULTI-STANDARD WIRELESS APPLICATIONS*

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This paper describes the design and implementation of a reconfigurable low-power sigma-delta modulator (SDM) for multi-standard wireless communications in a 90 nm CMOS technology. Both architectural and circuital reconfigurations are used to adapt the performance of the modulator to multi-standard applications. The feasibility of the presented solution is demonstrated using system-level simulations as well as transistor-level simulations of the modulator. HSPICE simulation results show that the proposed modulator achieves 76.8/78.9/80.8/85/89.5 dB peak signal-to-noise plus distortion ratio (SNDR) within the standards WiFi, WiMAX, WCDMA, Bluetooth and GSM with the bandwidth of 12.5 MHz, 10 MHz, 1.92 MHz, 0.5 MHz, and 250 kHz, respectively, under the power consumption of 37/37/12/5/5 mW using a single 1 V power supply.

Keywords: Multi-standard receivers; sigma-delta modulator; wireless communication standards.

1. Introduction

Growth of wireless communication standards combined with the limited success of previous generations of cellular systems forced the development of fourth generation systems (4G). These new systems are designed to fulfill the requirements of different standards, so comprising multi-standard receivers. Generally, three different receiver architectures including super-heterodyne, homodyne (zero-IF), and low-IF are used in integrated circuits.[1] As shown in Fig. 1(a) the super-heterodyne architecture mainly consists of two down-converting mixers. But, this structure needs at least one image reject and one channel selection filter with high quality factors and hence requiring several passive off-chip components.[1] So, this receiver architecture is not

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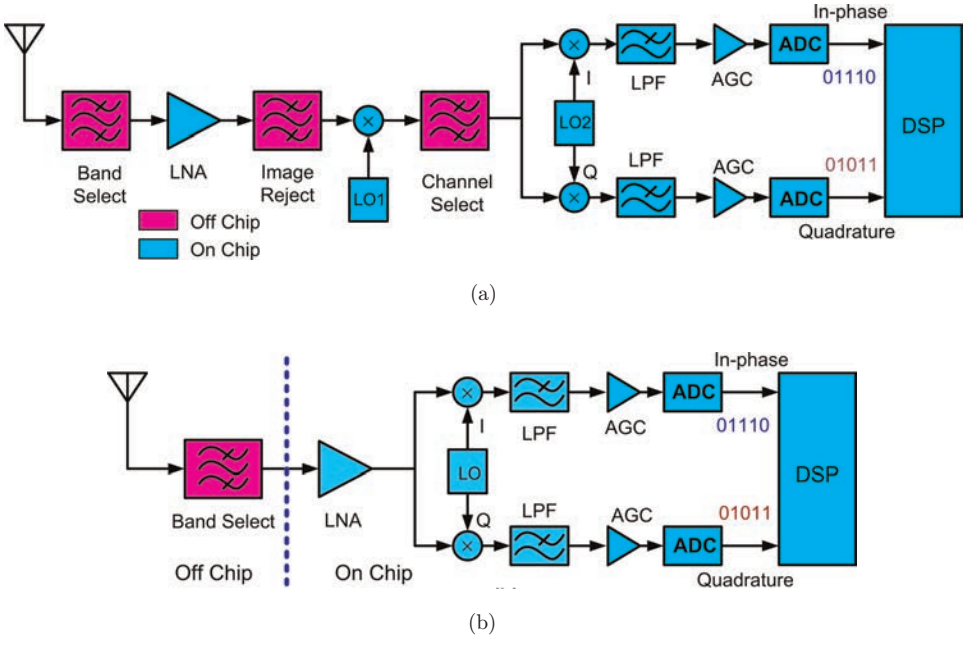

Fig. 1. General block diagram of (a) super-heterodyne and (b) zero-IF receivers.

suitable for integrated multi-standard applications while as shown in Fig. 1(b) the zero-IF and low-IF receivers consist of a simple RF front-end and only one off-chip band-select filter is needed and the other components are realized as on-chip.

After I/Q down-conversion, baseband analog-to-digital converters (ADCs) are used to digitize the received analog signal to be processed by the following digital signal processor. This ADC is one of the most challenging building blocks in a multi-standard system requiring a wide range of sampling rate and dynamic range (DR) to digitize the input signals with different bandwidths.

In this paper, a multi-standard ADC for a typical five modes low-IF, zero-IF receiver is introduced. The receiver is reconfigured as low-IF with an IF frequency of 125 kHz in the GSM standard[2,3] to relax the RF front-end requirements. Table 1

Table 1. Typical ADCs and our targeted multi-standard ADC specifications in different five communication standards.

Receiver architecture	Wireless standard	Signal bandwidth	Typical ADC ENOB	Targeted ADC ENOB
Zero-IF	IEEE 802.11/WiFi	12.5 MHz	7–11 bits	11 bits
Zero-IF	IEEE 802.16/WiMAX	10 MHz	7–11 bits	11 bits
Zero-IF	WCDMA	1.92 MHz	9–12 bits	12 bits
Zero-IF	Bluetooth	0.5 MHz	11–12 bits	12 bits
Low-IF	GSM	0.25 MHz	11–14 bits	14 bits

shows our targeted multi-standard ADC specifications compared with the typical ADC specifications associated with different standards, including WiFi, WiMAX, WCDMA, Bluetooth and GSM. The targeted ADC's effective number of bits (ENOBs) is higher than the typical resolutions needed in different standards to compensate the possible fabrication degradations and also to relax the RF front-end and preceding analog circuits' specifications. Vast variations in bandwidth and ENOBs make the design of such a reconfigurable low-power solution very challenging. In a multi-standard ADC not only both power consumption and chip area should be optimized for different operation modes, but also globally robustness against circuit non-idealities and also reconfiguration capability should be increased. It means in a multi-standard ADC, a single circuit which should be designed efficiently must adapt to different sets of specifications required for each operation mode. The sigma-delta modulators (SDMs) realized by switched-capacitor (SC) circuits are good candidates for this purpose.[4]

The paper is organized as follows. In Sec. 2, a multi-standard SDM capable of covering the requirements of five mostly used wireless communication standards is proposed. The system level simulation results including the mismatch and circuit non-idealities are presented in Sec. 3. Section 4 describes the transistor level implementation of the proposed multi-standard SDM. The circuit level simulation results are reported in Sec. 5. Finally, Sec. 6 concludes the paper.

2. Proposed Multi-Standard Sigma-Delta Modulator

DMs fall into two main categories. First are the single stage modulators, which benefit from the relaxed analog circuit building blocks, but, suffer from the stability problems in high order loop filter implementations which are inevitable in wideband input signals. Second are the multistage noise-shaping modulators (MASHs) which are well known for their stability while suffering from the existing leakage effects due to the mismatch between the analog and respected digital blocks.[5] To reduce this problem in MASH modulators, highly accurate analog circuits should be designed to be matched with the digital filters used at the end of each stage.

Recently, a new multi-loop modulator called sturdy MASH (SMASH) architecture has been presented in Ref. 6 which benefits from the stability of simple MASH modulators while the analog circuit requirements are relaxed like the single stage architectures. For a two-stage SMASH architecture shown in Fig. 2, the output signal is given by:

$$Y(z) = \mathrm{STF}_1(z)X(z) + \mathrm{NTF}_1(z)[1 - \mathrm{STF}_2(z)]E_1(z) + \mathrm{NTF}_1(z)\mathrm{NTF}_2(z)E_2(z)\,, \quad (1)$$

where STF and NTF denote the signal transfer function and noise transfer function, respectively. In this architecture, the quantization errors from the previous stages are shaped without using any digital filter. Additionally, it can be canceled using a low distortion topology[7,8]; i.e., a unity STF in the second stage. Indeed, this topology

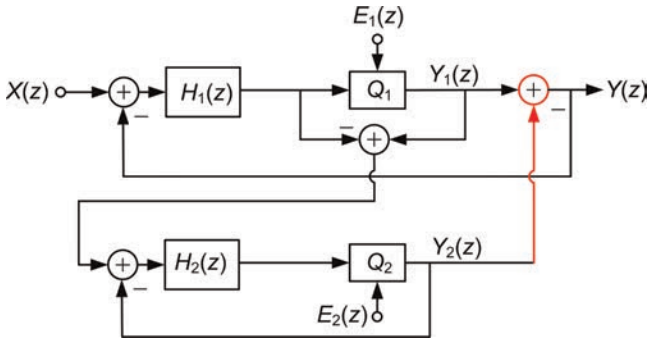

Fig. 2. Block diagram of a two-stage SMASH SDM.[6]

replaces the error cancellation logic required in traditional MASH modulators by properly combining the output of the stages by direct feedback paths from the 2nd stage output to the 1st stage input.

To implement a multi-standard ADC capable of dealing with five different performance requirements shown in Table 1, a flexible low power SMASH solution is proposed. The proposed reconfigurable modulator is represented in Fig. 3 which is able to process the signals from five distinguishable standards while the sampling frequency changes between only two different values; 200 and 62.5 MHz. This modulator is reconfigured to three architectural modes where each mode satisfies the requirements of one or two operation standards.

The 3-bit quantizers are used in both the first and second stages to achieve higher resolution while using a low oversampling ratio (OSR). However, note that feeding

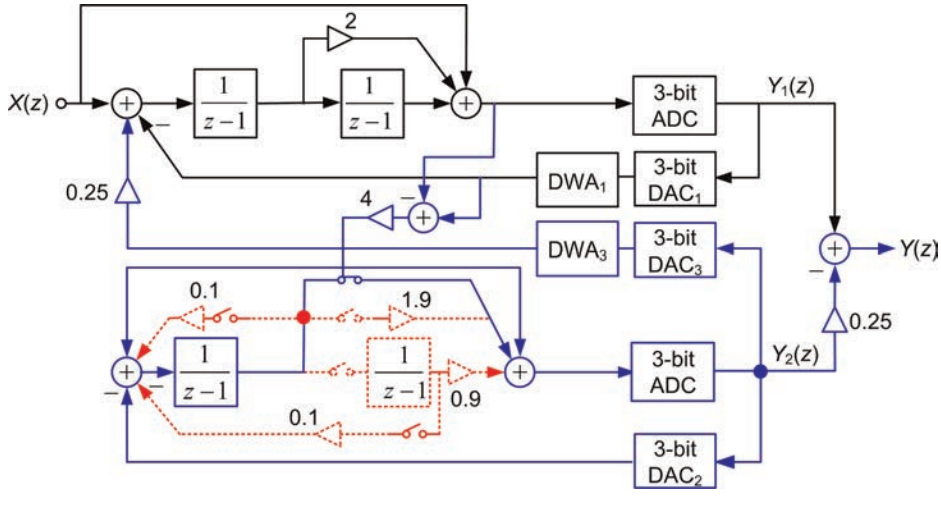

Fig. 3. Proposed multi-standard SDM.

the second stage output back to the first stage input as shown in Fig. 2 requires a DAC with double full scale and one more bit than the largest of the resolutions of the ADCs in the stages in order to account for the digital summation of the stages outputs if $d = 1$. In the case of $d = 4$ which is used here, a $p = 6$ multi-bit DAC is needed in the first stage loop filter making its realization very difficult. In general, the resolution of this extra DAC is $p = \max(m, n + \log_2(d)) + 1$ where m and n are the number of quantization bits in the first and second stages, respectively.[9]

On the other hand, tight timings for the quantizer and the digital adder used in the first stage loop of Fig. 2 might become impractical for high sampling rates, especially when the DAC linearization techniques are needed. Figure 3 shows a way to solve this problem and also to avoid the need for an extra high resolution DAC in the first stage modulator. The digital adder is replaced by an extra DAC at the input of the 1st integrator in the first stage loop filter and another digital adder at the final output. In other words, the digital adder in Fig. 2 is replaced by one analog adder realized together by the first integrator and one digital adder outside of the first stage modulator's loop.

The nonlinearity of internal multi-bit DACs caused by mismatch is one of the limiting factors of SDMs performance employing the multi-bit quantization. As shown in Fig. 3, there is three multi-bit DACs in the modulator architecture. Among them, the two DACs, DAC1 and DAC3 are the most critical ones because they are directly added to the input signal. So, the data weighted averaging (DWA) algorithm[10] was used to correct the mismatch caused errors in these two DACs.

2.1. *Different operation modes*

He proposed multi-standard SDM is configured to operate at three different modes to support five communication standards as discussed in detail in the following.

2.1.1. *SMASH 2-2 sigma-delta modulator*

The proposed SMASH 2-2 SDM is used for WiFi and WiMAX communication standards with sampling frequency of 200 MHz to achieve 11 bits of resolution. In this architecture, the second stage is a unitary STF architecture[7] to ideally eliminate the first stage quantization noise and relax the second stage analog circuits' requirements.

The optimum NTF is extracted to fulfill the requirements mentioned in Table 1. In wideband standards; i.e., WiFi and WiMAX the OSR is limited by the VLSI technology and power consumption. So, a couple of the NTF zeros are placed optimally at the inband frequencies to achieve the required resolutions. For this purpose, the derivation of the noise power inside the signal bandwidth is set to zero and the optimum value of g is calculated as:

$$g_{\text{opt}} = \frac{2\sin\frac{3\pi}{\text{OSR}} - 18\sin\frac{2\pi}{\text{OSR}} + 90\sin\frac{\pi}{\text{OSR}} - \frac{60\pi}{\text{OSR}}}{24\sin\frac{\pi}{\text{OSR}} - 3\sin\frac{2\pi}{\text{OSR}} - \frac{18\pi}{\text{OSR}}} . \tag{2}$$

Also, an interstage gain of 4 is used to further reduce the second stage quantization noise in overall modulator output signal. Hence, the modulator's ideal output signal is given by:

$$\begin{aligned} Y(z) &= X(z) - E_2(z)\frac{\mathrm{NTF}_1(z)\mathrm{NTF}_2(z)}{4} \\ &= X(z) - E_2(z)\frac{(1-z^{-1})^2(1-(2-g)z^{-1}+z^{-2})}{4}\,. \end{aligned} \tag{3}$$

2.1.2. *SMASH 2-1 sigma-delta modulator*

To fulfill the requirements of WCDMA standard in Table 1, the last integrator in the architecture shown in Fig. 3 is turned off to reconfigure the modulator as SMASH 2-1 with an NTF as:

$$Y(z) = X(z) - E_2(z)\frac{(1-z^{-1})^2(1-z^{-1})}{4}\,. \tag{4}$$

In this mode, the OSR is increased to 16, while the sampling frequency is reduced to 62.5 MHz because of the lower signal bandwidth in this communication standard.

2.1.3. *Second-order sigma-delta modulator*

Finally, the second stage of the presented SMASH architecture is turned off completely to simplify the modulator architecture as a second-order single-stage topology. This operation mode is used for Bluetooth and GSM standards with the OSR of 64 and 128, respectively, and the same sampling frequency as the previous mode, i.e., 62.5 MHz.

3. System Level Simulation Results and Analog Circuits Requirements

As discussed in Ref. 6, the relaxed analog blocks are the main property of SMASH topology compared with the conventional MASH architecture. The specifications of the operational transconductance amplifier (OTA) used to realize the first integrator in different operation modes are obtained using behavioral modeling of analog building blocks through system level simulations in MATLAB and Simulink[11] and the results are shown in Table 2. As shown in this table, the DC-gain requirement of

Table 2. DC-gain, unity gain bandwidth (GBW), and slew-rate (SR) of the first OTA in different operation modes.

Operation mode	DC-gain (dB)	GBW (MHz)	SR ($V/\mu S$)
SMASH 2-2 (Mode I)	30	500	200
SMASH 2-1(Mode II)	30	250	150
Second order single-stage (Mode III)	35	250	150

the first integrator in single stage mode is higher than the others because of the high value of OSR in Bluetooth and GSM operation modes.

The DWA algorithm was used to alleviate the modulator performance degradation due to the mismatch between the unit capacitors in DAC1 and DAC3. As shown later in Fig. 6, the value of the unit capacitors in DAC1 and DAC3 is 160 and 40 fF, respectively. This corresponds to a mismatch value of 0.25% and 0.7% with metal-insulator-metal (MIM) capacitors used in the simulated 90 nm CMOS technology in DAC1 and DAC3 unit capacitors, respectively. Table 3 summarizes the system level simulation results with nonlinear DACs and improving the performance by employing the DWA algorithm. For each simulation 40 Monte Carlo iterations were used and the averaged signal-to-noise plus distortion ratio (SNDR) was reported in Table 3. As is seen, the modulator performance degradation is negligible when using the DWA algorithm and on the other hand since the targeted SNDR is limited by the circuit noise rather than the quantization noise, so, the effect of DAC nonlinearities are alleviated by employing the DWA algorithm. It is worth mentioning that the DWA algorithms were simulated only in the system level and their circuit realization were not performed.

The SNDR degradation because of the mismatch between the analog interstage coefficient, $d = 4$, and its corresponding digital estimate in the presented modulator is studied. Figure 4 shows the SNDR degradation versus this mismatch when the modulator is in SMASH 2-2 and SMASH 2-1 operation modes. The sensitivity of SMASH modulators due to this mismatch is like the conventional MASH modulators since the first stage quantization error leakage is shaped similarly in both MASH and SMASH modulators.[12] Here, in the SMASH 2-2 operation mode, the SNDR degradation with 1% mismatch between the analog interstage coefficient and its corresponding digital coefficient is less than 3 dB.

Figure 5 shows the Monte Carlo simulation results of SNDR by considering 1% random mismatch between the nominal values in the scaling factors of the proposed $\Sigma\Delta$ modulator in SMASH 2-2 configuration. The mismatch in each modulator's coefficient was considered equal to three times of the standard deviation of a Gaussian random variable and independent random variables were used for different coefficients. The worst-case SNDR degradation is less than 3 dB in WiFi and WiMAX operation standards while it is less than 2 dB in WCDMA, Bluetooth and GSM modes.

Table 3. The effects of multi-bit DAC nonlinearities and their linearization by DWA algorithm.

BW (MHz)	Architecture	OSR	SNDR with ideal DACs (dB)	SNDR with real DACs (dB)	SNDR with DWA algorithm (dB)
12.5	SMASH 2-2	8	82	68.5	80
10	SMASH 2-2	10	83.5	70	82
1.92	SMASH 2-1	16	90	71	87
0.5	Second order single-stage	64	90	75	90
0.25	Second order single-stage	128	103	77.4	102

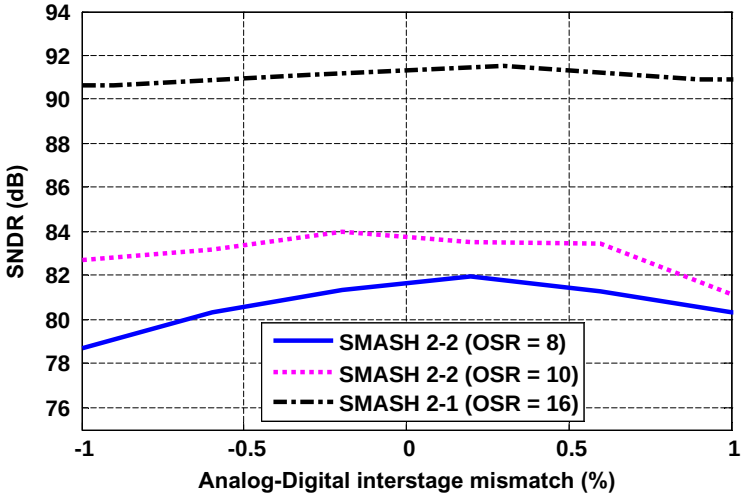

Fig. 4. SNDR degradation versus the mismatch between the analog interstage coefficient d and its corresponding digital estimate.

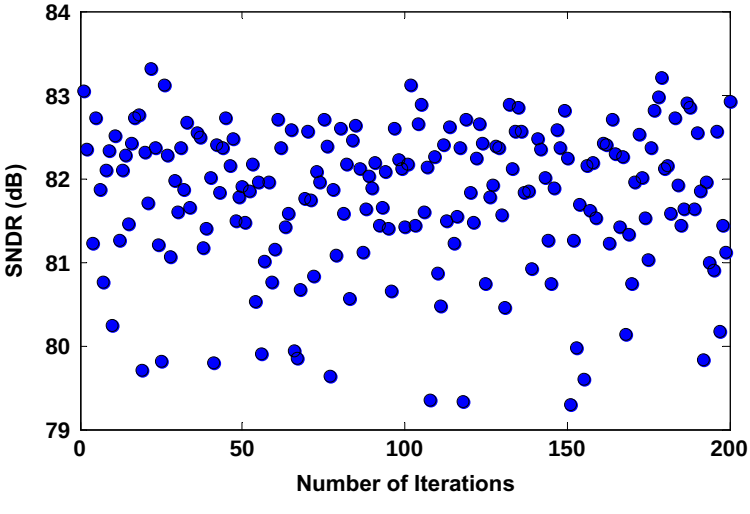

Fig. 5. SNDR versus the coefficients variation in SMASH 2-2 modulator with OSR = 8.

It is worth mentioning that in all system level simulations, including DAC non-linearities, mismatch between analog interstage coefficient and its digital estimate, and random variations of modulator's coefficients, the other circuit non-idealities listed in Table 2 were also considered.

4. Transistor Level Implementation

The proposed modulator is implemented using a 90 nm CMOS technology with 1 V power supply. As mentioned before, the last adder in the first loop of the SMASH architecture is implemented in the analog form on the first integrator to solve the problems caused by its digital implementation. Figure 6 shows the SC realization of the first integrator combined with this adder. The circuit samples the input signal V_{in} during ϕ_1 and then in the next phase; i.e., ϕ_2 it samples V_{DAC1} and V_{DAC3} and integrates these three sampled signals combined with adding the results of these integrations. The transfer function of this block is given by:

$$V_{o1}(z) = \frac{C_{S1}}{C_{I1}} \frac{z}{z-1}(z^{-1}V_{\text{in}} - V_{\text{DAC1}} + 0.25\,V_{\text{DAC3}}) \tag{5}$$

which shows the delaying and non-delaying integrating combined with adding operation on three signals of V_{in}, V_{DAC1} and V_{DAC3}. Here, the dashed lines show the paths allocated for DAC3 in Fig. 3 which will be eliminated in the third operation mode used in Bluetooth and GSM standards.

4.1. *Capacitor sizing*

The thermal noise is a critical factor in the performance of SDMs. In the presented multi-standard solution, by determining the transfer functions of each thermal noise power and then integrating them in to the respective signal band,[5] it is seen that the first integrator thermal noise affects the modulator performance directly whereas the other integrators thermal noise is shaped as:

$$P_{\text{th}-i} = \frac{4kT\pi^{2(i-1)}}{(2i-1)\text{OSR}^{2i-1}C_{si}}\,, \tag{6}$$

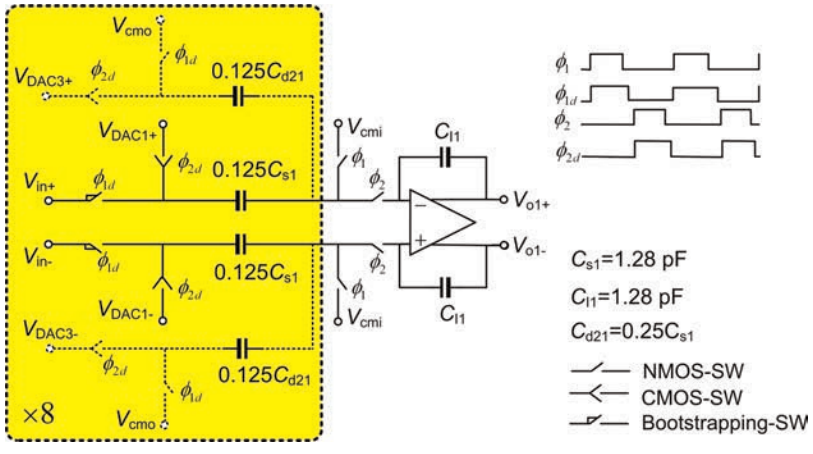

Fig. 6. The first integrator circuit in the proposed modulator.

where C_{si} is the sampling capacitor in the ith integrator. According to the required DR in the modulator, the sampling capacitors are evaluated as $C_{s1} = 1.28\,\text{pF}$, $C_{s2} = 0.3\,\text{pF}$, $C_{s3} = 0.2\,\text{pF}$, $C_{s4} = 0.2\,\text{pF}$ for the first to fourth integrators, respectively. It is worth mentioning that in all operational modes the modulator's resolution is limited by the circuit noise rather than the quantization noise to achieve a low power design.

4.2. *OTA architecture and transistor level reconfiguration*

According to moderate DC-gain and high GBW required for the amplifiers listed in Table 2, a pMOS input pair folded-cascode OTA, shown in Fig. 7, is used to realize the SC integrators. The folded-cascode amplifier is widely used in low voltage high speed applications because of its large output swing, low input common-mode voltage, and nearly single pole response.

To make the modulator an optimum low power multi-standard solution, the same OTAs are used for different standards while their bias circuit is changed from one standard to the other to optimize the power dissipation in different operation modes. Therefore, the modulator contains only five OTAs which are biased differently in targeted operation standards. Generally, realizing five different ADCs to fulfill the requirement of Table 1 needs 18 amplifiers; five for WiFi, five for WiMAX, four for WCDMA, two for Bluetooth and two for GSM, while the presented multi-standard ADC is implemented using only 10 different amplifiers consisting of five OTAs combined with three different bias circuits to realize its integrators and active adders in the whole targeted operation standards. Hence, the modulator contains 10 different amplifiers which occupy the area as large as only five mentioned OTAs with three different bias circuits. In this case, the modulator area is as large as only a

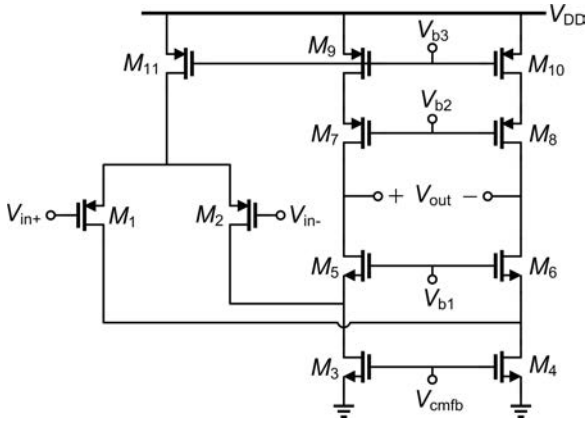

Fig. 7. PMOS input pair folded-cascode fully-differential amplifier.

Table 4. Simulated power consumption of the first amplifier in three different architectural operation modes.

Operation mode	Combination	Power consumption (mW)
SMASH 2-2 (Mode I)	$OTA_1 + Bias_1$	7.1
SMASH 2-1 (Mode II)	$OTA_1 + Bias_2$	4.2
Second order single stage (Mode III)	$OTA_2 + Bias_2$	2.8

single standard modulator while it fulfills the requirements of five different communication standards.

Also changing the OTAs' bias circuits decreases their power dissipation from wideband standards to the narrowband standards according to the relaxed unity GBW as mentioned in Table 2. Table 4 shows the power consumption of the first amplifier used in the three previously mentioned architectural operation modes in typical-typical process corner case.

4.3. *Multi-bit quantizers*

Using a multi-bit quantizer decreases the total quantization noise in the SDMs and enhances the modulator's stability while employing an aggressive noise shaping. So, in the presented multi-standard SMASH modulator, a 3-bit quantizer is used in the second stage. Also, the use of a 3-bit quantizer in the first stage decreases its quantization noise floor to relax the output swing of the active adder before the quantizer of the second stage. A dynamic latch with a negligible kickback noise[13] shown in Fig. 8 is used to realize these 3-bit quantizers. To decrease the modulator power consumption in different operation standards, the adder before the quantizer in the first stage of the modulator is realized using the passive adding concept. So, a two stage preamplifier shown in Fig. 9 is used before the dynamic latch to decrease its offset voltage error. The input offset storage (IOS) technique is also used to implement this passive adder as shown in Fig. 10.[14] Using this technique the destroying

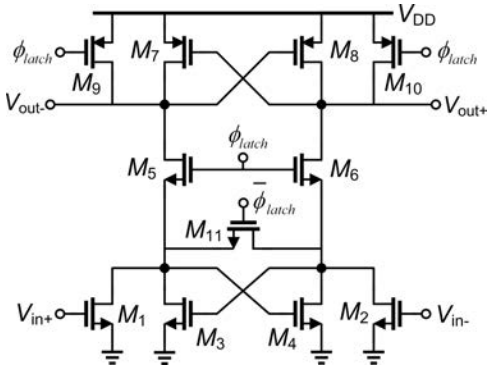

Fig. 8. Dynamic latch circuit used in the 3-bit quantizers.

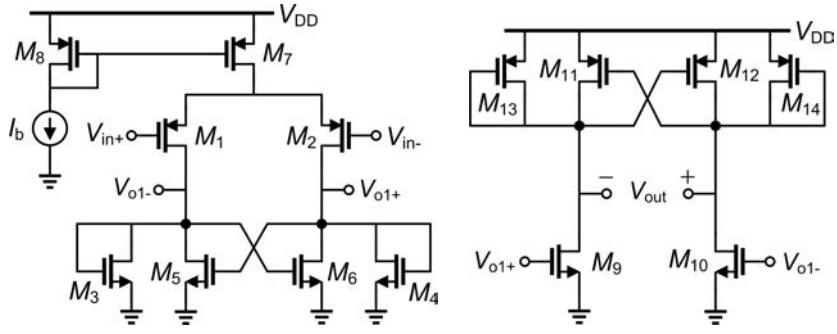

Fig. 9. (a) First stage and (b) second stage of a two-stage preamplifier used in the first stage quantizer.

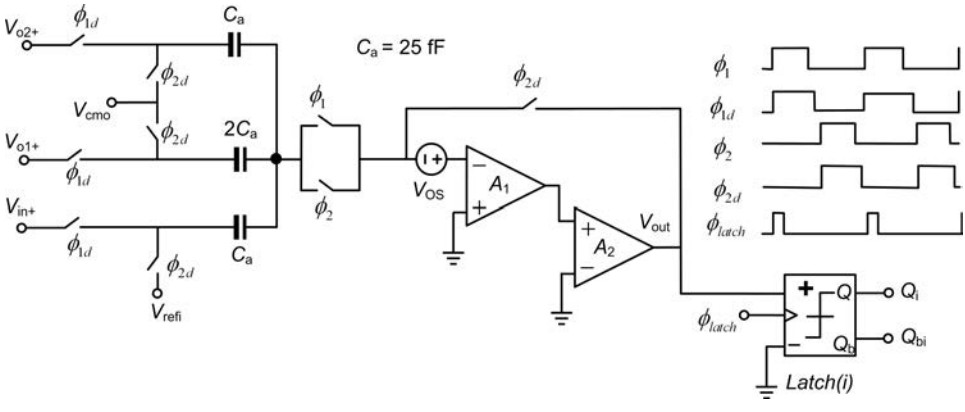

Fig. 10. Realization of the passive adder combined with the offset storage technique used in the first stage quantizer (shown as single-ended for simplicity).

effect of preamplifier's offset voltage ($V_{\rm OS}$) on the performance of the first quantizer and the total modulator is decreased. In this circuit the equivalent signal at $V_{\rm out}$ node is given by:

$$V_{\rm out} = V_{\rm in} + 2V_{o1} + V_{o2} - V_{\rm Ref} \tag{7}$$

which is needed at the input of the first stage quantizer.

The adding node before the quantizer in the second stage is realized using an active adder shown in Fig. 11. This circuit adds different signals with different weights and signs needed in the modulator architecture. Since the first adder is implemented using the passive adding concept, its output signal would not be available to be used in the second stage. Therefore, the second adder must add both previous signals ($V_{\rm in}$, V_{o1} and V_{o2}) and new signals (V_{o3}, V_{o4}) as needed in this node.

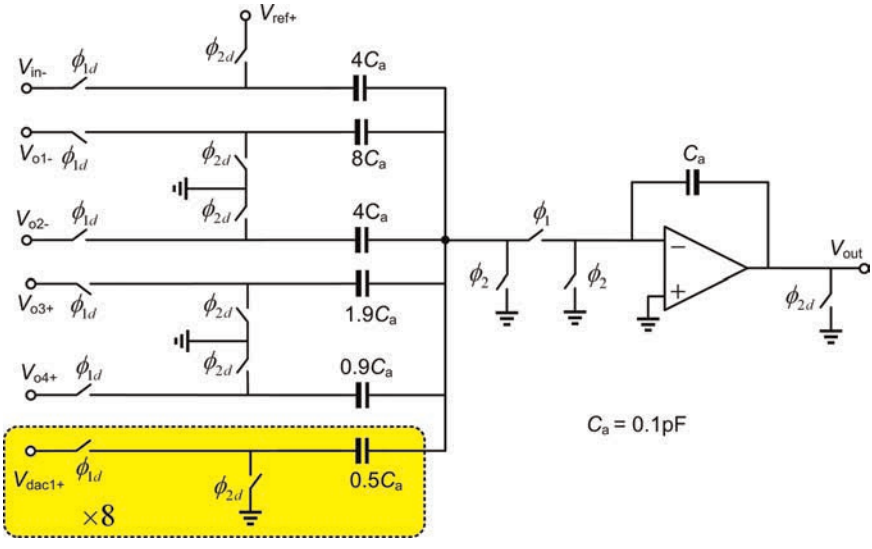

Fig. 11. Realization of the active adder used in the second stage modulator (shown as single-ended for simplicity).

So, its output at the end of ϕ_1 after complete settling reaches as:

$$V_{\text{out}} = 4(V_{\text{dac1}} - V_{\text{in}} - 2V_{o1} - V_{o2}) + 1.9V_{o3} + 0.9V_{o4}. \tag{8}$$

4.4. *Switches*

In the modulator architecture different types of MOS switches are used to optimally fulfill the required specifications. As shown in Fig. 6 the input signal sampling switches of the integrators are implemented using the bootstrapping technique presented in Ref. 15 to achieve the required linearity while it is sufficient for the DAC paths to employ the CMOS switches. In the other switches which are connecting a constant voltage node to the other node, simple nMOS or pMOS switches are used.

5. Circuit Level Simulation Results

The circuit level simulation results of the proposed reconfigurable multi-standard SDM implemented in a 90 nm CMOS technology were performed with HSPICE. To evaluate the modulator noise floor in different communication standards, different sinusoidal input signals were applied to the modulator and then its SNDR was calculated using the circuit level simulations regarding also the circuit thermal noise. Figure 12 shows the presented multi-standard modulator's output power spectral density (PSD), excluding the circuit noise, for five different operation standards.

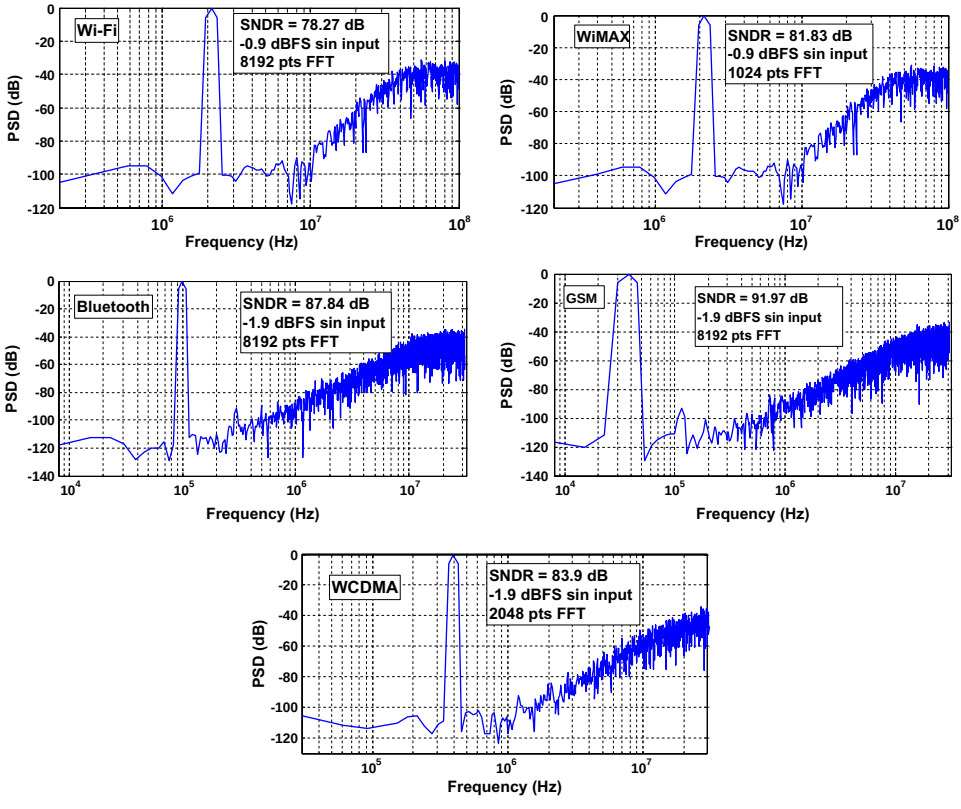

Fig. 12. PSD of the modulator output for different operation standards excluding the circuit noise.

Figure 13 shows the simulated DR of the proposed multi-standard SDM for different operation modes by excluding the circuit noise. The data to plot the SNDR curves was directly derived from HSPICE transient simulations where the circuit noise is not considered. Table 5 summarizes the performance of simulated multi-standard SDM in different process corner cases by considering the temperature variations. In this table, the effect of the circuit noise was also considered.

To compare this work with the other previously reported state-of-the-art SDMs the following figure of merit (FoM) is considered:

$$\text{FoM} = \frac{P}{2^{\text{ENOB}} \times f_N} \tag{9}$$

where P and ENOB refer to the modulator power consumption and ENOBs, respectively, and f_N shows the Nyquist rate of the converter. Table 6 compares this work with some of the previously reported SDMs. In this table, SNDR of the

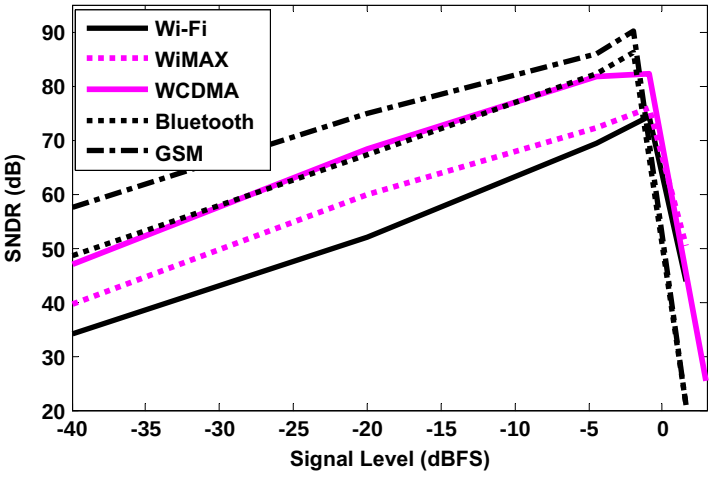

Fig. 13. Proposed modulator DR for different operation standards excluding the circuit noise.

modulator is calculated regarding both quantization and circuit thermal noises. It is worth mentioning that the power consumption of DWA algorithms used to linearize the mismatch induced errors in DAC_1 and DAC_3 unit capacitors has not been considered in the simulation results. Nonetheless, since the power supply voltage is very low and it is 1 V and an advanced CMOS technology was utilized, hence, the dynamic power consumption of DWA algorithms will be much less than that of the analog part of the modulator. Therefore, by considering the power consumption of DWA algorithms the achieved FoM will be affected very little and an outstanding FoM will be also achieved.

As shown in Table 6, the presented multi-standard modulator has a good value of FoM compared with previously reported SDMs. Using SMASH architecture with relaxed analog building blocks combined with optimally designed amplifiers in different operation standards has decreased our modulator power consumption meanwhile the modulator achieves a higher SNDR in each operation standard compared to the existing modulators. As mentioned before, the amplifiers are optimally used in different operation standards with different bias circuits. Hence, the modulator provides required performance for five different communication standards while its total area is near the area of an ordinary SDM which provides the same requested parameters for only WiFi communication standard.

It should be noted that although the reported results for the presented multi-standard SDM are based on HSPICE simulation results while most of the other modulators are implemented on chip, but its outstanding FoM verifies its performance as a good candidate for multi-standard wireless applications and it is also expected a better FoM to be achieved from the measurement results.

Table 5. The presented multi-standard modulator performance summary in three different process corner cases.

			SS @ 85°C		TT @ 25°C		FF @ 40°C			
BW (MHz)	Architecture	OSR	$SNDR_{max}$ (dB)	SFDR (dB)	$SNDR_{max}$ (dB)	SFDR (dB)	$SNDR_{max}$ (dB)	SFDR (dB)	Power (mW) TT @ 25°C	FoM (pJ/Conversion)
12.5	SMASH 2-2	8	68.8	75	76.8	84	79	87	37	0.26
10	SMASH 2-2	10	68.8	77	78.9	85	80	87	37	0.25
1.92	SMASH 2-1	16	77	88	80.8	91	81.8	90	12	0.34
0.5	Second order single-stage	64	84.8	89	85	91	86	90	5	0.34
0.25	Second order single-stage	128	87	89	89.5	92	90.5	94	5	0.41

Table 6. Performance comparison of the proposed ΣΔ modulator with the state-of-the-art modulators.

Work	Technology	V_{DD} (V)	Topology	f_N (MHz)	$SNDR_{max}$ (dB)	f_s (MHz)	Power (mW)	FoM (pJ/ Conversion)
This Work*	90 nm	1	SMASH 2-2	25	76.8	200	37	0.26
[16]	0.25 um	2.5	Continuous time complex high order	20	53.9	320	18.4	2.27
[17]	0.13 um	1.2	MASH 2-2	20	61.7	240	20.5	1.03
[18]	0.18 um	1.8	Fourth order single-stage	25	52	400	18	2.21
[19]*	0.35 um	2.2	MASH 2-1-0	20	59	200	18.9	1.3
[20]	0.18 um	1.8	MASH 2-2-2	16	48.5	64	27.5	7.9
[21]	0.13 um	1.2	Fourth order single-stage	30	63.7	300	70	2.04
[22]	65 nm	1.2	4-channel MASH 2-2	25	52	208	110	13.5
[23]*	0.13 um	1.2	Third order single-stage	10	54	320	5.5	1.34
[24]	0.18 um	1.8	MASH 1^8	8.33	60.1	50	95	13.98
This Work*	90 nm	1	SMASH 2-1	3.84	80.8	62.5	12	0.34
[19]*	0.35 um	2.2	MASH 2-1	4	62	91.7	7.4	1.8
[20]	0.18 um	1.8	MASH 2-2-2	4	78.9	64	27.5	0.95
[21]	65 nm	1.2	2-channel MASH 2-2	3.84	80	208	55.2	1.74
[25]	90 nm	1.2	Second order, continuous time	3.84	62.4	312	12.5	3
[26]	0.25 um	2.5	Third order single-stage	4	52	184.32	8	6.16
[27]	0.13 um	1.2	MASH 2-1	3.84	61.7	38.4	4.3	1.13
[28]	0.18 um	1.8	Third order single-stage	2	56.8	100	22.2	10.25
[29]	90 nm	1.2	MASH 2-1 multirate	4	65	80 320	6.83	1.07
[29]	90 nm	1.2	MASH 2-1 single rate	4	58	80	6.43	2.48
[30]*	0.35 um	1.8	Second order single-stage	3.84	51	25.6	5.5	4.95
[31]	0.25 um	1.5	Fifth order single-stage	4	63.4	150	2.7	0.56
[32]	0.5 um	2.5	MASH 2-2-1	4	87	64	150	2.06
[33]*	90 nm	1.2	2-path first order	4	56	60	1.56	0.76
This Work*	90 nm	1	Second order single-stage	1	85	62.5	5	0.34
[20]	0.18 um	1.8	MASH 2-2	1	76	64	6.3	1.22
[19]*	0.35 um	2.2	Second order single-stage	1	72	90	5.5	1.69
[29]	90 nm	1.2	Second order single-stage	1	76	90	3.7	0.72
[32]	0.5 um	2.5	MASH 2-1-1	1	95	64	90	1.96

Table 6. (*Continued*)

Work	Technology	V_{DD} (V)	Topology	f_N (MHz)	$SNDR_{max}$ (dB)	f_s (MHz)	Power (mW)	FoM (pJ/ Conversion)
[34]	0.18 um	2.7	Second order single-stage	1	77	23	30	5.2
This Work*	90 nm	1	Second order single-stage	0.5	89.5	62.5	5	0.41
[19]*	0.35 um	2.2	Second order single-stage	0.4	85	48.6	4.6	0.79
[26]	0.25 um	2.5	Third order single-stage	0.4	72	104	8	6.16
[29]	90 nm	1.2	Second order single-stage	0.2	77	50	3.43	2.97
[30]*	0.35 um	1.8	Second order single-stage	0.4	71	25.6	5.5	4.75
[35]	0.18 um	1.8	MASH 2-2	0.36	84	13	5	1.08
[36]	0.35 um	3.3	Third order single-stage	0.2	57	6.4	13.1	113
[37]	0.18 um	1	MASH 2-2	0.04	84	2	0.66	1.28
[38]	0.18 um	0.5	Fourth order single-stage	0.156	71	10	0.86	1.91

*Simulation results.

6. Conclusions

A reconfigurable SDM has been presented in a 90 nm CMOS with 1 V power supply. The modulator benefits from both architectural and circuital reconfigurations to fulfill the required specifications of WiFi, WiMAX, WCDMA, Bluetooth and GSM standards regarding the optimal power consumption and chip area issues. The modulator performance has been verified through extensive system level and circuit level simulations in different corner cases and temperature variations for the targeted operation standards.

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