INTEGRATION, the VLSI journal 55 (2016) 212–219

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

An NTF-enhanced incremental ΣΔ modulator using a SAR quantizer

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ARTICLE INFO

Article history:
Received 8 January 2016
Received in revised form
13 April 2016
Accepted 6 June 2016
Available online 16 June 2016

Keywords:
Incremental data converters
Sigma-delta modulators
Charge redistribution SAR ADCs
Error-feedback
Noise-shaping
Switched-capacitor circuits

ABSTRACT

In this paper, a noise transfer function (NTF) enhanced incremental sigma-delta (ΣΔ) modulator is presented. It employs a charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) in an error-feedback scheme to achieve an extra noise-shaping order. Using a multi-bit SAR quantizer not only improves the stability and power consumption but also facilitates the realization of both the adder situated in front of the quantizer and the whole error-feedback loop. As a design example, a multiplexed 2nd-order modulator based on the proposed architecture is simulated in TSMC 90 nm CMOS technology using Spectre with a 1 V single power supply. The simulation results show a signal-to-noise and distortion ratio (SNDR) of 85.3 dB within a signal bandwidth of 20 kHz (1 kHz/channel) at 5 MHz sampling frequency. The power consumption for each channel is 8.6 μW.

1. Introduction

Analog-to-digital converters (ADCs) used in biomedical applications, such as detecting biological signals like electroencephalographic (EEG) and electrocardiogram (ECG), usually confront many challenges. These converters require high accuracy while they should consume low power and area. Moreover, due to the nature of input signals, the ability of multiplexing is also an important consideration. Regarding these desired characteristics, an incremental analog-to-digital converter (IADC) is a well-suited candidate for such low frequency cases [1].

As shown in Fig. 1, incremental modulators are basically resettable sigma-delta modulators which enable them to be easily multiplexed between different channels. In other words, they are ΣΔ converters operating in a transient mode. For one conversion, the number of clock periods within two reset pulses is called the oversampling ratio (OSR). Indeed, both the loop and digital filters are reset every OSR number of clock periods. After each reset, the converter can be switched between different channels. Furthermore, the digital filter following the incremental modulator is much simpler than the decimation filter in conventional ΣΔ modulators [2].

The substantial issue in designing an IADC is speeding up the conversion rate. To lower the conversion time, similar techniques to ΣΔ modulators are utilized. The achievable SNDR with a constant OSR will be increased accordingly with the order of the modulator. There are two general ways to increase the modulator's order. One is using a high-order single-loop filter whose design theory is discussed in [2], and the other one is making use of cascaded or multi-stage noise-shaping (MASH) architectures [3]. In addition, due to the fact that the quantization noise is available in the analog form on the last integrator's output at the end of each conversion, another method that is called extended counting is introduced in [4,5] to further enhance the resolution. It usually contains a first- or second-order incremental converter in the first stage as the coarse quantizer. Then in the second stage, a Nyquist-rate converter is used as the fine quantizer. In some designs, the component sharing is also used to reduce both the die area and power consumption [6].

In the proposed modulator, an error-feedback scheme using a SAR ADC is employed in a unity signal transfer function (STF) topology to reduce the power consumption by increasing the overall noise-shaping order by one without adding an extra integrator. In addition, the adder situated in front of the quantizer is realized efficiently by utilizing the SAR sampling capacitors. Also, a simple operational transconductance amplifier (OTA) is added to apply the unit delay in the feedback path as well as the active feed-forward adder.

From the viewpoint of comparison, this structure has some advantages over other modulators. To compare with a conventional IADC, it is important to mention that a conventional 2nd-order feed-forward modulator needs three amplifiers to be realized with an active adder. However, in this paper, a 2nd-order

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http://dx.doi.org/10.1016/j.vlsi.2016.06.006
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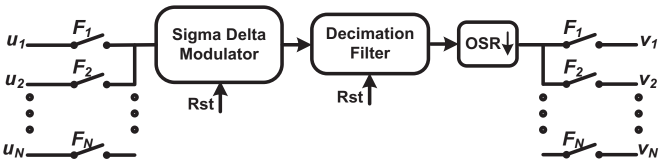

Fig. 1. Block diagram of a multiplexed incremental ADC.

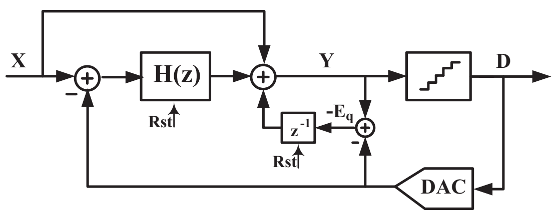

Fig. 2. An incremental noise-coupled modulator [7].

feed-forward IADC is presented using only two amplifiers with an active adder. Although using a passive adder eliminates one OTA and leads to lower power dissipation, the adder output is attenuated and it is sensitive to parasitic capacitors and kickback noise. Moreover, it should be mentioned that according to the presented architecture, the required DC gain and swing of the utilized OTAs are relaxed. As another example, in a conventional noise-coupled IADC [7] with a flash quantizer, the number of requisite comparators is exponentially proportional to the number of bits. However, by using a SAR quantizer, this number will considerably shrink to only one comparator. Moreover, the quantization noise extraction which is vital in an error feedback scheme can be performed more easily by employing a SAR ADC rather than a flash one. Additionally, the SAR's capacitors contribute to the input signal sampling through the input feed-forward path which is added in front of the quantizer. To address a drawback of using a SAR ADC instead of the flash one, the need of generating higher clock can be mentioned. Yet, since this method is utilized for low frequency applications, it does not impose any real limitation. As another instance for comparison, consider an extended counting modulator like the one presented in [5] which uses one more quantizer in the second stage compared to the presented modulator, so the area and power consumption will become more relatively.

The remaining of the paper is organized as follows. Firstly, in Section 2, the proposed structure is presented. In Section 3, a design example is discussed in both system and circuit levels. Then, the building blocks are described. The simulation results are included in Section 4, and finally, the conclusion is given in Section 5.

2. Proposed incremental ΣΔ modulator

2.1. The noise-coupled structure

In the proposed incremental ΣΔ modulator, the enhancement of NTF is realized by employing an error-feedback scheme in a low-distortion feed-forward architecture. In other words, the noise-coupled technique is utilized to improve the noise-shaping order by one without using an additional integrator. Regarding Fig. 2, the modulator's output in z-domain is obtained as:

$$D(z) = \left[X(z) - D(z)\right]H(z) + X(z) + E_q(z) - z^{-1}E_q(z) \tag{1}$$

So, we have:

$$D(z) = X(z) + \frac{\left(1 - z^{-1}\right)}{\left(1 + H(z)\right)}E_q(z) \tag{2}$$

where $1/(1+H(z))$ is the NTF of the conventional modulator excluding the error-feedback loop, which provides Lth-order of noise-shaping itself. Therefore, the new NTF can be written as:

$$NTF_{New} = \left(1 - z^{-1}\right)NTF_{conventional} \tag{3}$$

Additionally, using a unity STF structure reduces the output swing of the integrators, and hence, decreases the distortion because only the quantization noise is processed by the integrators [8]. However, the implementation of the extra analog adder placed in front of the quantizer has been always a complicated issue. In most cases, an additional switched-capacitor amplifier is added to implement the summation [9]. Nevertheless, in some instances to get much less power consumption, a passive summation is realized. However, the passive adder attenuates the added signals resulting in decreased reference voltages in the comparators. To alleviate the effect of offset voltage of the comparators, a preamplifier is needed preceding the regenerative latch in comparators. So, this also results in more power consumption in the ADC realization. Moreover, the passive adder suffers from high sensitivity to the parasitic capacitors and the elements' mismatch [10].

With regard to the above discussions, the main difficulty in the implementation of the architecture shown in Fig. 2 is the realization of the error-feedback loop as well as the feed-forward adder. The quantization noise extraction and the way to apply a unit delay through the feedback path are two main issues. In the proposed modulator, a SAR ADC is utilized as the quantizer to simplify the implementation of not only the error-feedback loop but also the feed-forward adder. A SAR ADC is typically known as a low power ADC which is widely used in biomedical applications and wireless sensor networks. The intrinsic merits of a SAR ADC make it a better option in comparison with the flash one for a noise-coupled structure. For example, it needs only one comparator, while its counterpart requires 2^n-1 comparators where n is the ADC number of bits. Furthermore, a SAR ADC can store the quantization noise by performing one more cycle through the conversion process. So, the quantization noise extraction which is a fundamental function in an error-feedback scheme will be accomplished quite simply. In addition, the technique introduced in [11] is utilized to provide the unit delay in the feedback path. By this means, a simple OTA is added to buffer the quantization noise. Besides, it acts as an active adder to add the integrators' output in front of the quantizer. Moreover, the SAR sampling capacitors can contribute in the input signal sampling preceding the quantizer. Furthermore, it is worth mentioning that the capacitors mismatch error in DAC array of the SAR ADC is Lth-order shaped in this structure. In the following section, further details regarding the SAR ADC contributions will be explained.

2.2. Structure of the proposed incremental ΣΔ modulator

In this paper, a novel Incremental ΣΔ modulator is presented which is shown in Fig. 3. In this structure, the error-feedback scheme and an active feed-forward summation is realized by a charge redistribution SAR ADC and a simple OTA. The implementation of the error-feedback loop and the feed-forward path is shown in Fig. 4. To shed light on the noise extraction issue, assume that the SAR algorithm performs for one more cycle in a conversion process. Then, at the last operation, the comparator's decision of the least significant bit is applied to the charge redistribution DAC array. So, the difference between the input signal and the digital output, which is called the quantization noise, is stored on the dummy capacitor at the comparator's input [12]. For example, if a three-bit SAR ADC functions four cycles in the conversion time, it can store the quantization noise at the end of each conversion.

The next step is to apply the unit delay to the extracted quantization error according to Fig. 3. Likewise the technique introduced in [11], a relaxed OTA is used to buffer the noise which is saved on the dummy capacitor at the end of ϕ_1 as shown in Fig. 4. In other words, the quantization noise of the previous phase is stored on the dummy capacitor and it is considered to be converted at the next phase. Since the dummy capacitor stores and transfers the quantization noise itself, there is no charge sharing concern here. Besides, the integrators' outputs are added through C_i capacitors using the same OTA at ϕ_2. Note that, since the integrators' output swings are small, due to the usage of a low-distortion architecture, there will be no concern about nonlinearity effects and high voltage swing for the OTA which buffers and adds at the same time.

The final path to be added is the input signal's feed-forward path in Fig. 3. This path will be directly applied to the bottom plate of the SAR sampling capacitors which is depicted in Fig. 4. This direct path owing to the use of a SAR ADC, eliminates the requirement of an extra active circuit [13]. Bear in mind that the dummy capacitor does not participate in the input sampling since it is involved in the noise extraction process. Consequently, a voltage reduction coefficient equal to $(2^nC-C)/2^nC$ will appear across the path, where C and n denote the unit capacitance of the DAC array and the quantizer's resolution, respectively. Accordingly, to avoid the increase of the whole loop swing, the same gain should be applied on the primary input signal's path by the sampling process of the first integrator.

Eventually, it is worth mentioning that in an error-feedback noise-shaping SAR ADC, the comparator's non-idealities such as the input-referred offset and circuit noise are shaped similar to the quantization noise. Yet, it does not affect the DAC error of the SAR ADC, E_{DAC}, which is defined as the difference between the ideal and the real DAC voltages. Indeed, only by using the error-feedback structure in an incremental ΣΔ modulator, as performed in the proposed architecture, Lth-order of shaping will be achieved for the DAC error of the SAR ADC. This fact will be substantiated through the z-domain derivations as it is modeled in Fig. 5:

$$D(z) = Y(z) + E_q(z) - E_{DAC}(z) \tag{4}$$

$$Y(z) = \left[X(z) - D(z)\right]H(z) + X(z) - z^{-1}\left[-Y(z) + D(z) + E_{DAC}(z)\right] \tag{5}$$

So, we have:

$$D(z) = X(z) + \frac{\left(1-z^{-1}\right)}{1+H(z)}E_q(z) - \frac{1}{1+H(z)}E_{DAC}(z) \tag{6}$$

As it is clear, the DAC array's non-idealities of the SAR ADC, E_{DAC}, is Lth-order shaped at the final output.

3. Design example

In this section, a design prototype of a 2nd-order modulator is provided in order to assess the efficiency of the proposed structure. It is aimed to achieve 14-bit resolution in a 90 nm CMOS technology. The input signal bandwidth is around 20 kHz for 20 channels (1 kHz/channel). The system model and the switched-capacitor circuit are presented. Additionally, the circuit design of each block is described in the following sections.

3.1. System level analysis

The proposed 2nd-order modulator followed by a cascaded integrator decimation filter is depicted in system level in Fig. 6. The modulator processes the input signal every *OSR* number of clock periods, and then resets all memory blocks prior to the next conversion. Therefore, regarding Fig. 6, the adder's output, Y, can be found at the end of M clocks, where M is equal to the *OSR* number:

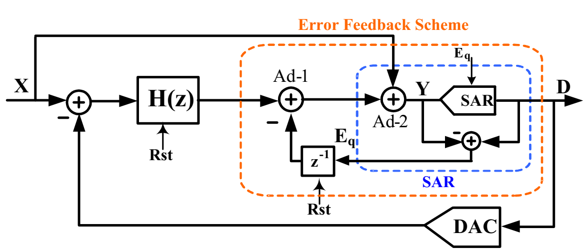

Fig. 3. Proposed incremental sigma-delta modulator.

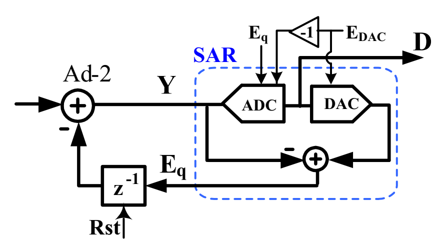

Fig. 5. SAR DAC error modeling.

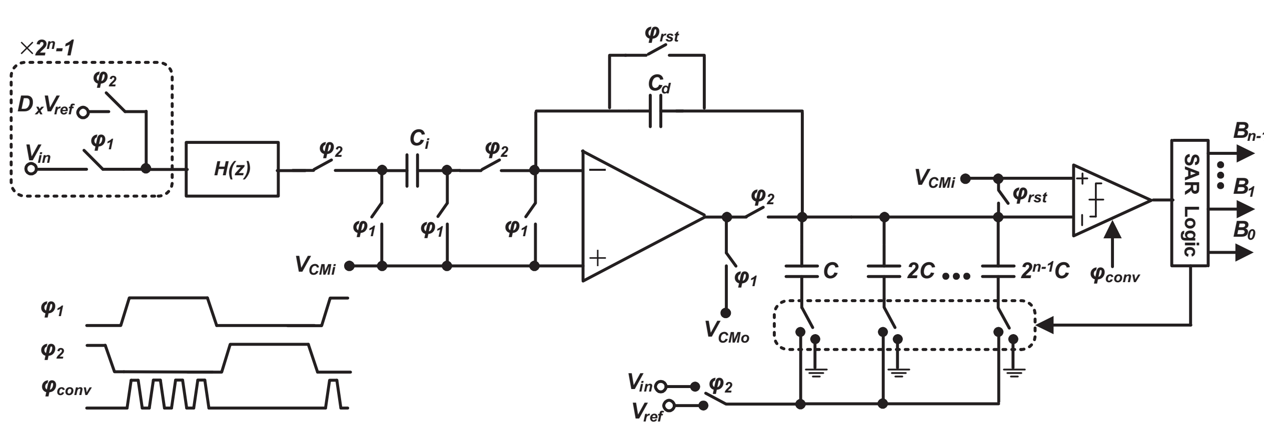

Fig. 4. The implementation of the error-feedback loop and the feed-forward path in the proposed incremental ΣΔ modulator.

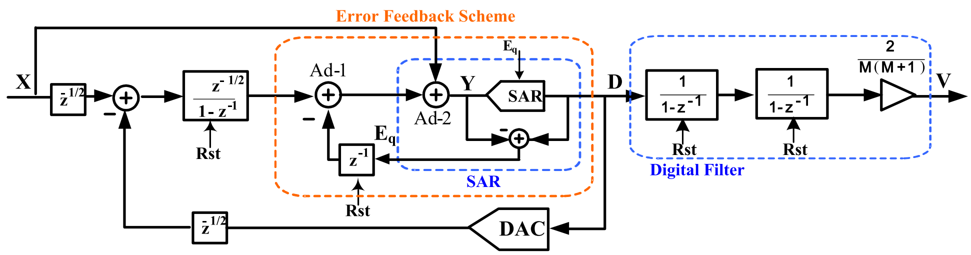

Fig. 6. Proposed second-order incremental ADC.

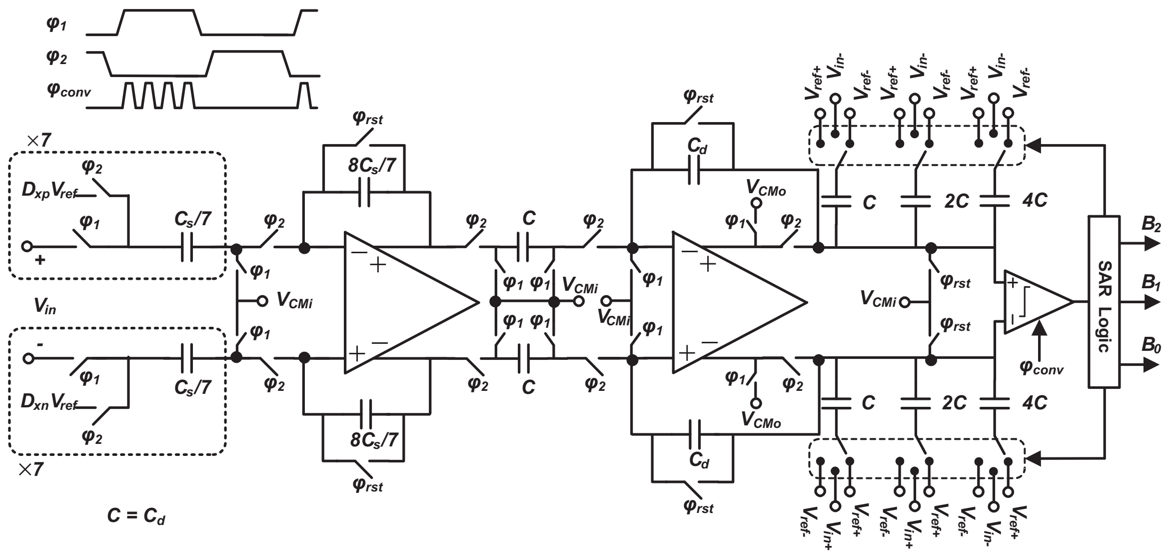

Fig. 7. Switched-capacitor implementation of the proposed second-order incremental modulator.

$$Y[0] = X[0]$$
$$Y[1] = X[1] + X[0] - D[0] - D[0] + Y[0]$$
$$= (X[1] + X[0]) + X[0] - D[0] - D[0]$$
$$Y[2] = X[2] + X[1] + X[0] - D[1] - D[0] - D[1] + Y[1]$$
$$= (X[2] + X[1] + X[0]) + (X[1] + X[0]) + X[0]$$
$$- (D[1] + D[0]) - D[0] - (D[0] + D[1])$$
.
.
.
$$Y[M] = \sum_{l=0}^{M}\sum_{k=0}^{l} X[k] - \sum_{l=0}^{M-1}\sum_{k=0}^{l} D[k] - \sum_{l=0}^{M-1} D[k] \tag{7}$$

Besides, According to the linear model, the following equation can be written for the last cycle:

$$D[M] = Y[M] + E_q[M] \tag{8}$$

Thus, by placing Eq. (7) in Eq. (8), we have:

$$E_q[M] = \sum_{l=0}^{M}\sum_{k=0}^{l} X[k] - \sum_{l=0}^{M}\sum_{k=0}^{l} D[k] \tag{9}$$

So, due to the fact that the quantizer's error is bounded between $-V_{QLSB}/2$ and $+V_{QLSB}/2$, where V_{QLSB} is the least significant bit of the quantizer employed in the modulator, the following relation is achieved:

$$-\frac{V_{QLSB}}{2} \le \sum_{l=0}^{M}\sum_{k=0}^{l} X[k] - \sum_{l=0}^{M}\sum_{k=0}^{l} D[k] \le +\frac{V_{QLSB}}{2} \tag{10}$$

Since V_{QLSB} is equal to $2V_{FS}/2^n$, where n denotes the quantizer's number of bits, Eq. (10) is rewritten as:

$$-\frac{V_{FS}}{2^n.(M+1)^2} \le \bar{X} - \frac{2}{(M+1)^2}\sum_{l=0}^{M}\sum_{k=0}^{l} D[k] \le +\frac{V_{FS}}{2^n.(M+1)^2} \tag{11}$$

Hence, as the difference between the input signal and the equivalent digital output is always bounded between half of the converter's *LSB* voltages, the effective number of bit (*ENOB*) is achieved as:

$$ENOB = \log_2\left(\frac{V_{FS}}{V_{LSB}}\right) = \log_2\left(\frac{2^n.(M+1)^2}{2}\right)$$
$$= 2\log_2(M+1) + n - 1 \tag{12}$$

As it is clear, the *ENOB* of the proposed incremental modulator is equal to the conventional second-order incremental modulator. In other words, an extra first order noise-shaping is provided in the proposed modulator through the SAR ADC.

3.2. Circuit level implementation

The complete differential circuit of a 2nd-order incremental modulator with a 3-bit SAR quantizer is depicted in Fig. 7, which qualifies the desired specifications according to the discussions given in [2] and the behavioral system level simulations. To explain the circuit operation, one cycle of the conversion is investigated. Two non-overlapping clock phases with similar duration time, ϕ_1 and ϕ_2, are used. Suppose that the input signal has been sampled into the integrator's sampling capacitors at ϕ_1, while the SAR quantizer has finished its conversion at the end of ϕ_1. Thus, the DAC output is ready at the integrating phase, ϕ_2. At this time, the integrator's output is simultaneously transferred through the capacitor C and saved on the dummy capacitor, C_d. Besides, the previous quantization error which has been stored in the dummy capacitor, in the previous phase, is placed in the feedback during ϕ_2. In addition, the bottom plates of the charge redistribution DAC capacitors of the SAR ADC are sampling the input signal directly at ϕ_2. The time interval between input sampling at ϕ_1 and ϕ_2 has no considerable effect because the input signal is a low frequency, and so it does not differ very much. All in all, the first OTA is sampling at ϕ_1 and integrating at ϕ_2, whereas the SAR quantizer is sampling at ϕ_2 and converting at ϕ_1. By this timing, the DAC output is prepared at the positive edge of ϕ_2.

It is worth to mention that although the OTA in the integrator is loaded by both integrating and summation capacitors in ϕ_2. But, by this way, the SAR ADC is operated in ϕ_1 instead of the non-overlapping time between clock phases. So, although the load of the OTA has been increased, the ADC total power consumption is decreased since the operating time of the SAR ADC is increased to half of the clock period instead of operating in just the non-overlapping time.

With regard to the previous descriptions, the addition operation shown by Ad-1 and Ad-2 is illuminated by giving the time-domain derivations. The relevant circuit in the single-ended structure is illustrated in Fig. 8, with considering two non-overlapping clock phases, ϕ_1 and ϕ_2. In this figure, V_{intg} is the integrator's output. Since the SAR ADC converts the data in ϕ_1, the comparator's input, V_{cmp}, is equal to the quantization noise at the end of this phase:

$$V_{cmp}[n-1] = E_q[n-1] \tag{13}$$

At the end of ϕ_2, the voltage which is ready to be converted by the next phase is equal to $V_{in}[n] - V_{cmp}[n]$. Thus, the output voltage will be acquired by adding the quantization noise to this voltage as follows:

$$D[n] = V_{in}[n] - V_{cmp}[n] + E_q[n] \tag{14}$$

By using the charge conservation law, which states that the net charge of an isolated node remains constant, at the input node of

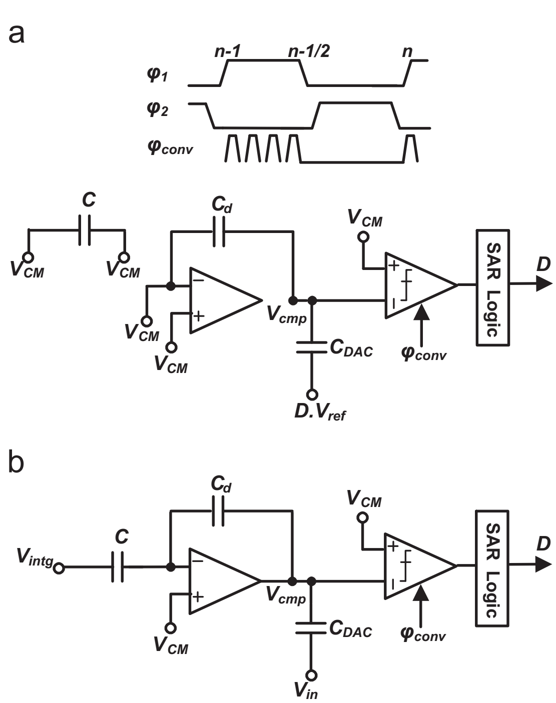

Fig. 8. (a) Addition circuit in ϕ_1, and (b) addition circuit in ϕ_2.

the OTA, we have:

$$C_d E_q[n-1] = C_d V_{cmp}[n] + C V_{intg}[n] \tag{15}$$

Considering both Eqs. (13) and (15), and recalling that C_d is equal to C, Eq. (14) can be rewritten as:

$$D[n] = V_{in}[n] + E_q[n] - E_q[n-1] + V_{intg}[n] \tag{16}$$

which confirms the adding function of the Ad-1 and Ad-2 blocks in Fig. 6.

Preceding the next sub-section, it is worth mentioning that the value of the input sampling capacitors which is estimated in order to get to a thermal noise lower than −92 dB. Since only the thermal noise of the first integrator is noticeable, the input sampling capacitor, C_s, is assumed to be 420 fF.

In the following sub-sections, the building blocks of the proposed modulator are explained briefly.

3.3. *Operational transconductance amplifiers*

From the behavioral system level simulations, DC gains of 35 dB and 40 dB are estimated for the first and second OTAs, respectively. Since the integrator's output swing is small, around 0.2 V, a simple folded-cascode OTA is employed to reach the desired specifications. Likewise, the same topology is utilized for the second OTA. Because it adds up and buffers just the quantization noise, then the output swing is small again, less than 0.35 V. The total static power for each OTA including the bias circuit is 22.2 μW and 27 μW, respectively.

3.4. *SAR quantizer*

A typical SAR ADC consists of three parts; a capacitive array, which functions as both sampler and DAC, a comparator, and a digital control logic. The designs of these three parts are introduced in the following.

3.4.1. *Capacitive array*

As mentioned in the previous section, due to the shaping of the DAC array's non-idealities by one, for a 14-bit ADC with an *OSR* of 128, DAC capacitors should qualify utmost 6-bit accuracy in a 3-bit SAR quantizer. This is because of the fact that the difference of the resolutions between a 2nd and 1st order modulator, regarding [2], is equal to:

$$2\log_2(M) + n - 1 - \left(\log_2(M) + n\right) = 6 \tag{17}$$

where M is the *OSR* number and n is the quantizer's resolution.

Pursuant to an error calculation of a charge redistribution DAC addressed in [14], and by considering $3\sigma_{DNL,max} \le 0.5LSB$, where $\sigma_{DNL,max}$ is the maximum standard deviation of differential non-linearity (DNL) error and *LSB* is the least significant bit of the SAR quantizer, 15 fF unit capacitor is exploited to realize the 6-bit accuracy and decrease the parasitic capacitors' effects. Note that the thermal noise effects are not considerable since it is shaped by one order when it is modeled in Fig. 6.

3.4.2. *Digital control logic*

A digital control logic usually is included in a SAR ADC in order to generate the signals which control the comparator and DAC switches. Besides, it determines the output digits. A 3-bit non-redundant SAR logic [15] is employed to use just n flip–flop instead of $2n$ ones. Therefore, three multiple input registers are required, whereas each register has a memorization, a data load from the comparator's output, and a right shift input. To select one of the inputs, a decoder-multiplexer is added before each D flip–flop as shown in Fig. 9. Note that all blocks are implemented by NAND gates.

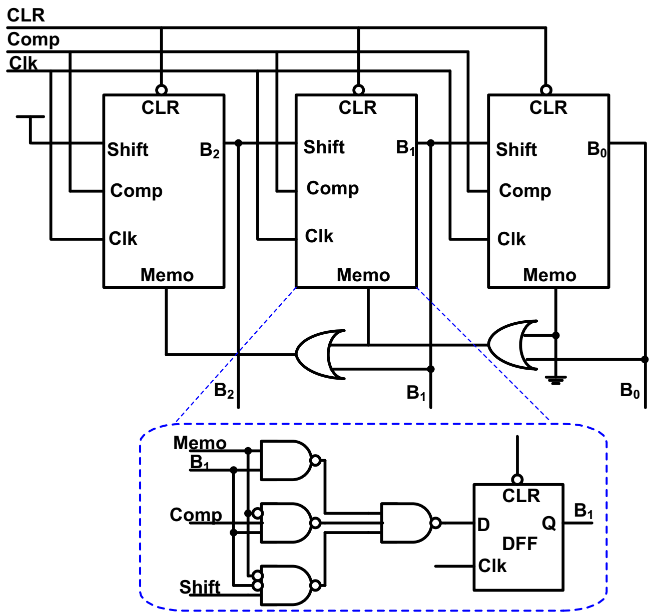

Fig. 9. SAR ADC control logic.

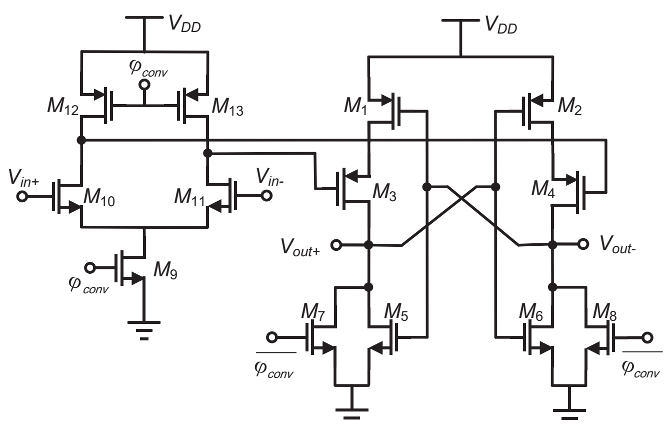

Fig. 10. Double-tailed dynamic latched comparator [16].

3.4.3. Comparator

Power consumption is a crucial parameter in the proposed ADC, so a fully dynamic double-tailed latched comparator shown in Fig. 10 is utilized [16]. In this structure, the pre-amplification and latch regeneration are performed at the same phase, called the evaluation phase. This topology has separated input and output stages resulting in lower kickback noise and latch offset. Furthermore, it is worth mentioning that the comparator's design was not challenging, as the SAR ADC is a 3-bit quantizer and the sampling clock rate is not too high. The power consumption of 76 nW is just dynamic and the comparator consumes no static power.

3.5. DAC

The input sampling capacitors of the first integrator are shared within DAC capacitors in the feedback path, so they should be large enough to avoid mismatch errors of 0.2% and qualify for 14 bit accuracy. To relax the capacitors' size, a dynamic element matching (DEM) technique based on data weighted averaging (DWA) algorithm is applied. This technique shapes the DAC mismatch induced errors by first order to the high frequencies [17]. This method is simulated in system level simulations in MATLAB. According to the simulation results, the DWA algorithm prevents SNDR degradation while considering 0.2% random mismatch among the 3-bit DAC unit elements used in the feedback path.

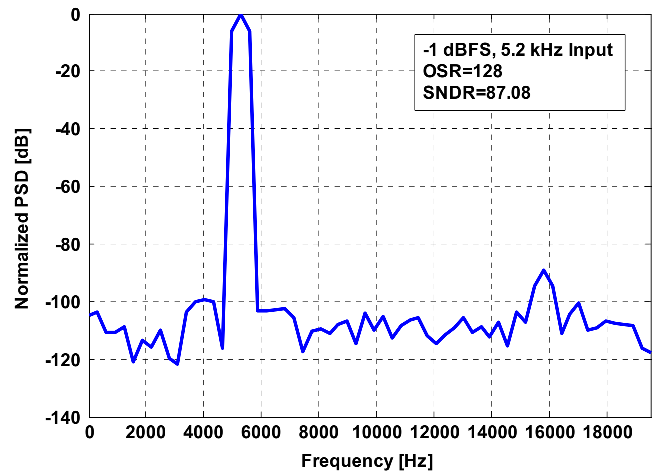

Fig. 11. Simulated output spectrum of the proposed incremenral ADC exculding the circuit noise.

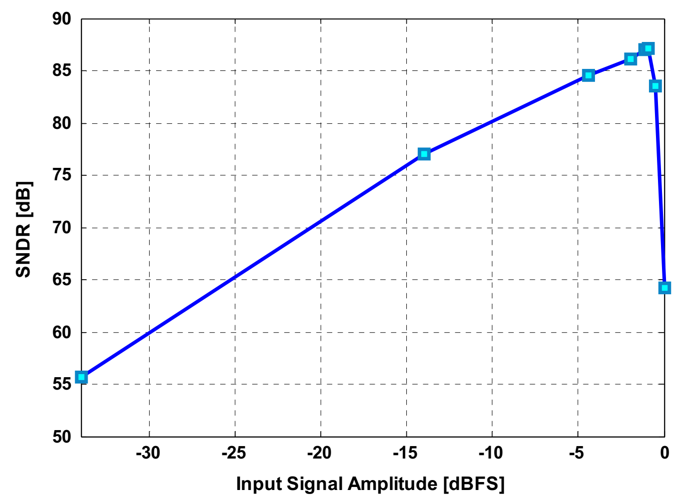

Fig. 12. Simulated SNDR versus the input signal amplitude exculding the circuit noise.

Table 1
Performance summary of the proposed incremental modulator.

Parameter	90-nm CMOS		
	FF @ -40 °C	TT @ 27 °C	SS @ 85 °C
SNDR	85.1 dB	85.3 dB	84.4 dB
ENOB	13.83	13.87	13.72
Power dissipation	130.1 μW	172 μW	225.7 μW
Sampling rate	5 MHz		
Oversampling ratio	128		
Signal bandwidth	0.976 kHz		
Number of channels	20		
Power supply voltage	1 V		

4. Circuit level simulation results

The designed ADC has been simulated in TSMC 90-nm standard CMOS technology using Spectre with 1 V power supply. The modulator samples 20 channels with around 1 kHz signal

Table 2
Performance comparison.

	This Work**	ISCAS'12* [18]	ESSCIRC'13* [19]	CICC'14* [6]	ISSCC'13* [20]	ISSCC'13* [21]	TCASI'11* [22]	TCASI'15* [23]	ICECS'09** [24]	MEJ'15*** [25]	ISNE'13*** [26]
Architecture	IADC2	IADC2	IADC1 + 10 b SAR	IADC2 + IADC1	IADC2 + 6 b SAR	IADC2	IADC2 + 10 b cyclic	CT two-step IADC	CT MASH2 IADC	IADC2	IADC1 + 7b SAR
Process	90 nm	90 nm	0.6 µm	65 nm	0.16 µm	0.16 µm	0.18 µm	0.18 µm	0.18 µm	65 nm	0.18 µm
V_{DD} (V)	1	1.2	3.3	1.2	1.8	1	2	1.2/1.8	1.8	1	1.8
Number of Channels	20	2	8	1	1	1	1	16	1	1	1
Sampling Rate	5 MHz	1 MHz	5 MHz	96 kHz	25.6 kHz	750 kHz	115 MHz	320 kHz	9 MHz	10 MHz	128 kHz
OSR	128	256	256	192	1024	500	5	40	45	200	32
Diff. Input Range	0.9 V_{pp}	1 V_{pp}	2 V_{pp}	2.2 V_{pp}	1.8 V_{pp}	0.7 V_{pp}	3.6 V_{pp}	0.7 V_{pp}	–	–	–
Peak SNDR (dB)	85.3	74	70.07	90.8	119.8****	82	72	75.9	74	77.3	69.38
Bandwidth/channel	976 Hz	977 Hz	9.75 kHz	250 Hz	12.5 Hz	667 Hz	11.5 MHz	250 Hz	100 kHz	25 kHz	1.88 kHz
Power/Channel	8.6 µW	6.75 µW	145.25 µW	10.7 µW	6.3 µW	20 µW	48 mW	2.16 µW	1.3 mW	25 µW	23.07 µW
FOM_W (pJ/conv.)*****	0.29	0.84	2.9	0.76	0.32	1.48	1.02	0.85	1.59	0.083	2.55
FOM_S (dB)******	165.8	155.6	148.3	164.5	182.7	157.2	155.8	156.53	152.8	167.3	148.3

* Measurement results.
** Schematic simulation results.
*** Post-layout simulation results.
**** Since SNDR was not reported, SNRmax is used for FOM_W calculation, instead.
***** $FOM_W = Power/(2^{ENOB} * 2 * BW)$.
****** $FOM_S = SNDR + 10 * \log(BW/power)$.

bandwidth per channel. The oversampling ratio is 128, so the sampling frequency is determined 5 MHz. The maximum resultant SNDR for a 5.2 kHz sinusoidal input signal with −1 dBFS amplitude is 87.08 dB. Modulators' bitstreams are measured and then processed by Matlab through a cascaded integrator decimation filter. The power spectral density of the whole ADC is shown in Fig. 11 where the circuit noise has not been considered. By considering the circuit thermal noise in SNDR calculation, it becomes 85.3 dB corresponding to 13.87 ENOB. The simulated SNDR is illustrated over different input signal amplitudes in Fig. 12. Table 1 summarizes the performance of the simulated modulator in different process corner cases and temperatures variations. The average power dissipation of 8.6 µW per channel has been achieved excluding the decimation filter.

A comparison to some recent similar structures is provided in Table 2. It should be mentioned that the results of the proposed modulator is based on the circuit level simulations while the other modulators are reporting the measured results and this is not a fair comparison. Nonetheless, the achieved outstanding figure of merit (FoM) of the simulated modulator verifies the efficiency of the proposed incremental modulators, and hence, it is also expected a better FoM to be achieved from the measurement results.

5. Conclusions

In this paper, an NTF-enhanced incremental modulator is proposed which utilizes a SAR type quantizer. The error-feedback loop is realized using an OTA which buffers the quantization noise of the previous conversion and adds up the integrators' output simultaneously. Furthermore, the direct path of the input signal added in front of the quantizer is realized by utilizing the SAR sampling capacitors. According to the design prototype, just two OTAs with relaxed specifications are needed to achieve a second-order noise-shaping with an active summation. As a result of this structure, 20 channels within signal bandwidth of almost 1 kHz per channel are digitized with an effective resolution of 13.87-bit consuming only 172 uW. The proposed incremental modulator can be used in low power and high resolution applications.

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