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An LO architecture with novel wide locking range, quadrature output RILFDs and ILROs for cognitive radio applications

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Abstract In this paper, a wide locking range, quadrature output ring type injection locked frequency divider (ILFD) is presented for division ratios of 3 and 4. This ILFD proposes a novel injection scheme that shapes the injection signal to a proper form and provides a convenient situation for divider locking. Furthermore, two new wide locking range, low power consumption, injection locked ring oscillators (ILROs) are proposed for quadrature generation in local oscillator architectures. A novel cognitive radio quadrature local oscillator (LO) architecture is presented by utilizing the proposed ILFDs and ILROs to verify the effectiveness of the proposed circuits. Moreover, a new technique is implemented on the LO architecture to widen the frequency range without consuming any extra power. Because of using a single LC tank, this architecture is very compact. Also, it has the benefit of low power consumption and low output phase noise.

Keywords Class-C VCO · Cognitive radio · Injection locked frequency divider · Injection locked ring oscillator · Local oscillator

1 Introduction

Nowadays, the federal communication committee (FCC) imposes a lot of limitations in allocating frequency bands to new users, because the most of the spectrum is occupied. To solve this problem, the cognitive radio (CR) is introduced to transmit data by the secondary user until the main user does not utilize the channel. The FCC defines a CR as "a radio that can change its transmitter parameters based on interaction with the environment in which it operates" [1]. The desired frequency range for this purpose is from 50 MHz to 10 GHz [2]. It is clear that producing the local oscillator (LO) signal for this wide range with a single oscillator is not possible. Therefore, proposing a compact and low phase noise frequency extension circuit is one of the main challenges in these structures.

Using one LC-VCO that is followed by several dividers and multipliers is a proper solution to meet this concept. The subsequent frequency extension circuits help LC-VCO to have narrower tuning range, and thus, lower phase noise. Flip-flop based frequency dividers are the basic structures that are selected for this approach. They use simple structures and are broadband and robust over process variations. However, the maximum operating speed of these dividers is limited by the cut-off frequency (f_T) of the transistors and their power consumption increases with the frequency of operation [3]. Additionally, they cannot generate quadrature phased output signals with 50 % duty cycle when the division ratio involves an odd number.

Recently, injection locked frequency dividers (ILFDs) are taken into consideration. They alleviate the limitation of f_T, and thus, they can be used for applications at frequencies in tens of gigahertz. Moreover, the quadrature outputs depend on the circuit structure. There are two types of ILFDs: LC-type ILFDs [4–6] and ring-type ILFDs [7–9]. The problem with LC ILFDs is their narrowband characteristics due to the high quality Q factor of the LC-tank. In addition, they occupy large chip areas due to inductors. With their low Q nature, ring-type ILFDs have large locking range and small chip areas [10]. The problem of poor phase noise of the ring oscillators (ROs), does not appear in the ring ILFDs. In a divide-by-N ILFD, the phase

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noise of the output signal follows that of the input with a $20 \times \log N$ reduction. So, it is mainly determined by the phase noise of the input source [11].

In this paper, a wide locking range RILFD with a new method for shaping the injection signal to a proper form is proposed for division ratios of 3 and 4. Additionally, two novel wide locking range and low power consumption injection locked ring oscillators (ILROs) are presented for quadrature generation. The proposed circuits are used to generate a novel CR LO architecture which provides 1.75–10.5 GHz. The signals with frequencies lower than 1.75 GHz can be provided by cascading five flip-flop based divide-by-2 circuits.

The paper is organized as follows. Section 2 gives an overview of the proposed LO architecture. Section 3 presents the proposed ILFDs and gives a locking range formulation for them. Section 4 explains the structure of the proposed ILROs. The LO circuit implementation is described in Sect. 5. The simulation results of the proposed ILFDs, ILROs and LO architecture are presented in Sect. 6, and finally, Sect. 7 concludes the paper.

2 The proposed cognitive radio local oscillator architecture

In this section, an LO architecture is presented that provides the frequency range of 1.75–10.5 GHz by utilizing the ILFD and ILRO circuits which are proposed in the next sections of the paper. Figure 1 shows the proposed LO architecture and the frequency contribution of each block. This architecture is a single LC tank frequency extension circuit with a few RILFD and ILRO circuits. So, it is a very compact, low power consumption and low phase noise structure. The spur level of the proposed architecture is very low, because there is no mechanism to generate frequency components other than harmonics in the integer mode ILFDs and ILROs [2]. Except for the LC-VCO and divide-by-2 circuits, the rest of the circuits are proposed in this paper. Also, a novel method is presented in the LO architecture which provides a portion of desired frequency range without the need for additional circuitry by using the tail signals of the divide-by-3 differential pair. The description of the proposed RILFDs and ILROs and the LO circuit implementation are given in the following sections.

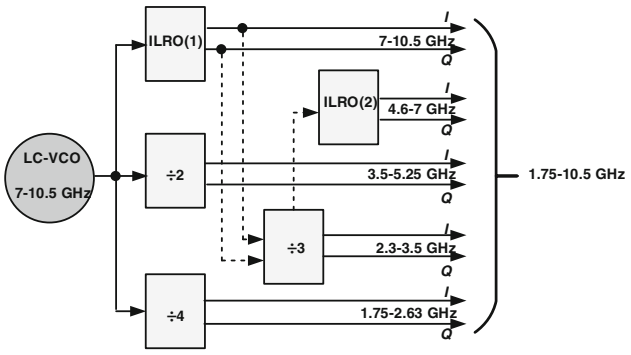

Fig. 1 Architecture of the proposed 1.75–10.5 GHz quadrature LO

3 Proposed ring type injection locked frequency dividers (RILFDs)

Providing a wide locking range is the main challenge in the ILFDs with high division ratios. Besides, the LO architecture must generate quadrature outputs. In order to satisfy these specifications, in this paper, an RILFD for division ratios of 3 and 4 with a wide locking range, quadrature output, low power consumption and without extra control mechanisms is presented. This ILFD proposes a novel injection scheme to shape the injection signal to a proper form and provides a convenient situation for locking the ILFD. The shape of the injected signal will be affected in two ways by this new technique. Firstly, the divide-by-3 and 4 cases will be converted to the divide-by-2. Therefore, the proposed ILFD will be locked in a convenient state because a two-stage RILFD (that is an intrinsic divide-by-2 circuit) is utilized as the base of the proposed ILFD. The second is the shaping of the injection signal to the pulses that is injected at the times which have the least effect on the natural operation of the ring oscillator. The new method is described below.

3.1 Proposed divide-by-3 circuit

Figure 2 shows the proposed divide-by-3 RILFD circuit. The circuit is based on a two-stage differential ring oscillator with the positive feedback load. The cross-coupled pMOS transistors create negative resistances to compensate the resistive losses and make the oscillation condition achievable at much lower power consumption [12]. Additionally, the positive feedback load generates outputs with sharp transitions and large amplitudes making high nonlinearity operation of the oscillator [10]. Therefore, it can provide strong harmonics, and hence, a wide locking range for the ILFD.

The direct injection topology is employed for the ILFD. The best time for injecting signals in this situation is at zero-crossings of the output signals. In a differential two-stage RILFD circuit, the output positive and negative peaks of one stage are synchronous with the output zero-crossings of the other stage. If the conventional direct injection is used for the divide-by-3 (injecting a single-phase input to one stage), the injections will be applied to the circuit in every positive peak of the injection signal. Therefore, by

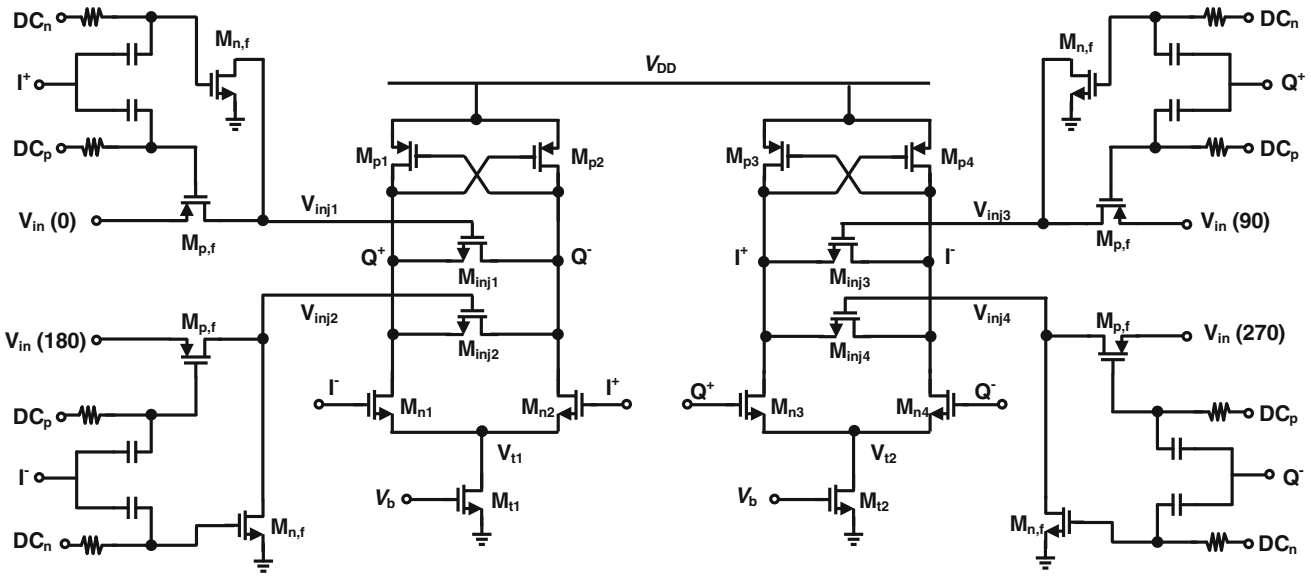

Fig. 2 Circuit schematic of the proposed divide-by-3 ILFD

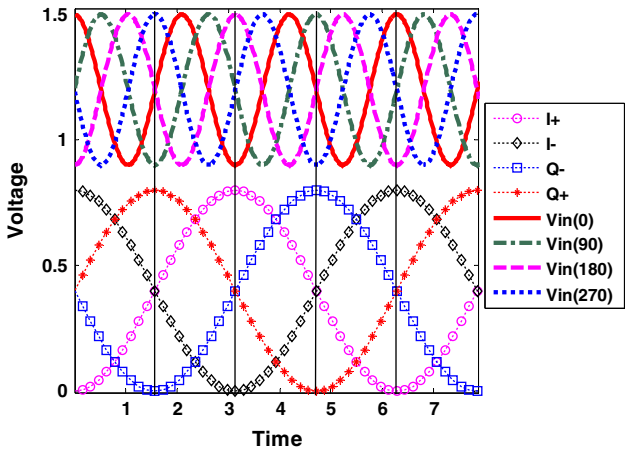

Fig. 3 Quadrature waveform of input signal at the frequency of $3f$ and output signal at the frequency of f in the ideal form

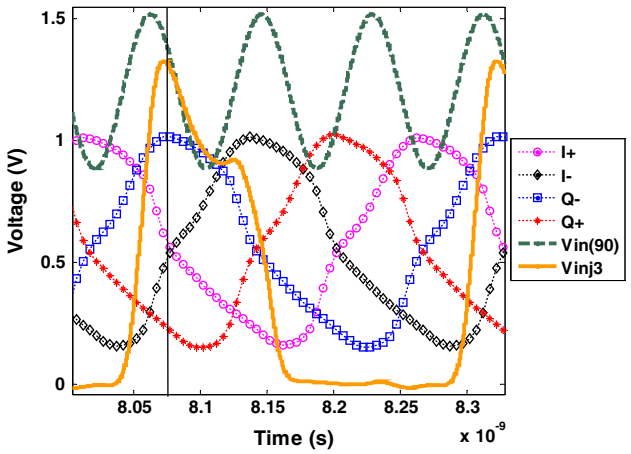

Fig. 4 Simulation waveforms of the proposed divide-by-3 circuit

considering one input signal, e.g. $V_{\text{in}}(0)$ in Fig. 3, this signal is injected three times during one output period that only one of them is synchronous with the output zero-crossings.

On the other hand, as depicted in Fig. 3, in the case of divide-by-3, the zero-crossings of four quadrature outputs (at the frequency of f) occur at positive (or negative) peaks of four quadrature inputs (at the frequency of $3f$). The proposed ILFD uses this property to eliminate the unwanted injections at the non-zero-crossing times by adding four feedback circuits to the conventional two-stage RILFD. In the feedback circuits, the output signals of the ILFD are compared with the quadrature input signals and the injection is only applied at the zero-crossings of the ILFD outputs which are the best instants for the injection.

For instance, according to Fig. 2, $V_{\text{in}}(90)$ is compared with Q^+ by the gate-source voltage of $\text{M}_{\text{p,f}}$. Whenever their difference is greater than the pMOS threshold voltage, $\text{M}_{\text{p,f}}$ will be ON and $\text{M}_{\text{n,f}}$ goes to the saturation region so the current will flow through $\text{M}_{\text{p,f}}$ and $\text{M}_{\text{n,f}}$ whereupon V_{inj3} will have a positive value. Otherwise, $\text{M}_{\text{p,f}}$ is OFF, $\text{M}_{\text{n,f}}$ is in the sub-threshold region and V_{inj3} goes to zero. So, the waveform of the injected signal (V_{inj3}) is different from the input signal [$V_{\text{in}}(90)$]. To inject the signal at the best time, the DC_p and DC_n bias voltages are chosen in such a way that only in the negative peaks of Q^+ (zero-crossings of I^+ and I^-), V_{GS} of $\text{M}_{\text{p,f}}$ is greater than its threshold voltage and the injection is done. Simulation results show the effectiveness of the proposed topology in Fig. 4. It is observed that V_{inj3} is produced one time in every three periods of $V_{\text{in}}(90)$, in the negative peaks of Q^+.

The proposed ILFD structure is based on the one introduced in [13], but with some innovations to improve the locking range and output waveform. In [13], one feedback circuit is used while the proposed circuit has four feedback circuits which eliminate more unwanted injections as explained before and increase the locking range. Additionally, in [13], using a single feedback circuit for injecting the signal to one stage causes the output signals of two stages to have different waveforms while this does not occur in our proposed circuit, since the injections are applied in two stages by quadrature phases. Furthermore, the bias voltages of $M_{p,f}$ and $M_{n,f}$ (DC_p and DC_n) in the proposed ILFD have been separated while [13] uses the same bias voltage for them. This separation is considered because of high output dc voltage of the LC-VCO which causes the selection of a high value for DC_p. However, using this dc voltage for DC_n drives $M_{n,f}$ out of the saturation region. Hence, by separating these voltage sources, the locking range is increased. Moreover, the presented ILFD in [13] uses the tail bias voltage to change the division ratios. In this case, the division ratio will be very sensitive to the bias voltage variations whereupon any small change in the bias voltage could shift the desired division ratio to the previous or the next ratio. For example, if a divide-by-3 circuit is required, with a few undesirable bias changes, we will have a division ratio of 2 or 4. In other words, no specific parameter is defined to separate the division ratios in the ILFD of [13]. While in the proposed ILFD, changing the input voltage phases determines the division ratio that is a reliable method.

A small size should be selected for M_{inj}, $M_{p,f}$ and $M_{n,f}$, because the ring oscillator works with the transistors' parasitic capacitances. So, adding a large capacitance to the output nodes by injection transistors has adverse effects on the locking range. Consequently, the values of the coupling capacitors should also be minimum. It forces a large value for the resistors to generate a high pass filter with low enough cut-off frequency, and so, appropriate signal transferring. The thermal noise of the resistors increases the internal noise of the ILFD, but it has a little impact on the output noise, based on the following equation [14]:

$$\pounds_{ILO}(\Delta\omega) = \pounds_{inj}(\Delta\omega) \cdot \frac{1}{N^2 1 + \left[(\Delta\omega/\omega_L)^2\right]} + \pounds_{osc}(\Delta\omega) \cdot \frac{(\Delta\omega/\omega_L)^2}{1 + (\Delta\omega/\omega_L)^2} \quad (1)$$

This equation gives the phase noise spectrum of an oscillator which receives an injection signal and produces an injection locked oscillator (ILO). $\pounds_{ILO}(\Delta\omega)$, $\pounds_{inj}(\Delta\omega)$ and $\pounds_{osc}(\Delta\omega)$ are the phase noise spectrums of the ILO, the injection signal, and the free-running oscillator, respectively. Also, ω_L and N denote the locking range and division ratio. When $N \geq 2$, the ILO will be an ILFD. This equation indicates that in an ILFD with a division ratio of N, in low offset frequencies, the phase noise of the output signal follows that of the input with a $20 \times \log(N)$ reduction. So, as the proposed ILFD has the large locking range, its output phase noise is mainly determined by the phase noise of the injection source and the internal circuit's noise is negligible at the output.

3.2 Proposed divide-by-4 circuit

The proposed injection method can also be used to widen the locking range in the case of divide-by-4. Figure 5 shows that the zero-crossings of four quadrature outputs (at the frequency of f) occur at the positive (or negative) peaks of a single input (at the frequency of $4f$). So, the circuit of Fig. 2 can be utilized for divide-by-4 by replacing all the

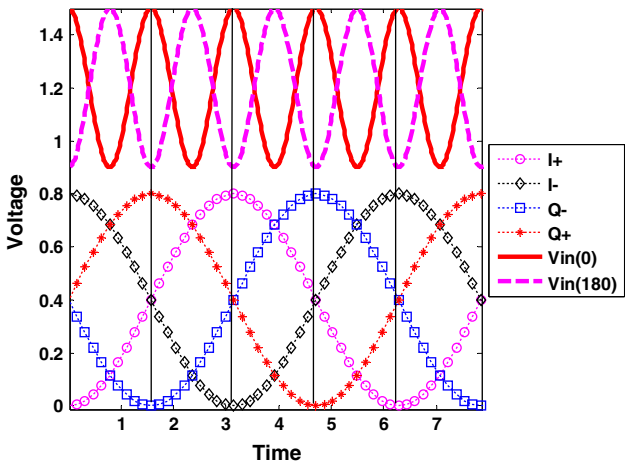

Fig. 5 Differential waveform of input signal at the frequency of $4f$ and quadrature output signal at the frequency of f in the ideal form

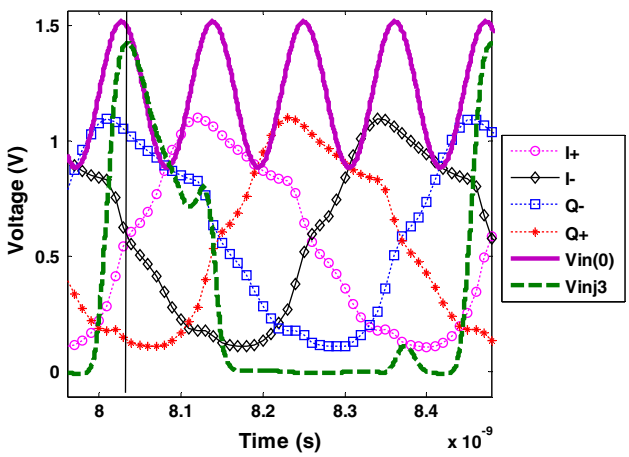

Fig. 6 Simulation waveforms of the proposed divide-by-4 circuit

input signals with a single-phase input. The waveforms from the simulation of the circuit in the case of division ratio of 4 are shown in Fig. 6. It demonstrates that the input signal is injected in expected times (zero-crossings of I^+ and I^-). Therefore, by injecting proper phases through four feedback parts, we have two separated wide locking range ILFDs for division ratios of 3 and 4.

3.3 Locking range formulation

As mentioned in Sect. 3.1, the proposed ILFD is based on a two-stage direct injection RILFD with a difference in the form of the injection signals. Therefore, we can utilize the analysis of the locking range of [15] by changing the injection signal from the sine wave to the new model of this paper.

The circuit implementation of a single delay cell and the corresponding behavioral model are shown in Fig. 7. The nMOS and pMOS differential pairs are described by the nonlinear elements K_1 and K_2, respectively. If we consider a low to high transition of $V_{\text{in}}(t)$ (from $-V_O$ to V_O), when the input signal crosses a threshold voltage, which is set to zero for convenience, K_1 changes V_x to $-V_O$ and the capacitance C is discharged. Simultaneously, $V_{out}(t)$ decreases in an exponential fashion until it reaches the threshold voltage of K_2, and then, K_2 instantaneously pulls the output voltage to the final value of $-V_{\text{O}}$. The injection current by M_{inj} is shown as $i_{inj}(t)$. The propagation time of the delay cell defined as the time it takes $V_{out}(t)$ reaches from $\pm V_O$ to the zero level, is described by:

$$t_p = \ln(2)RC \tag{2}$$

The free-running frequency of an N-stage ring oscillator is expressed by:

$$f_0 = \frac{1}{2Nt_p} = \frac{1}{2N\ln(2)RC} \tag{3}$$

To avoid ambiguity, it is considerable that there are four input signals $V_{in}(\text{t})$ and four injection signals $V_{inj}(\text{t})$ in the proposed circuit where the four $V_{in}(\text{t})$ are shown in Fig. 2 as $V_{in}(0)$, $V_{in}(90)$, $V_{in}(180)$ and $V_{in}(270)$ and the four $V_{inj}(\text{t})$ are shown as V_{inj1}, V_{inj2}, V_{inj3} and V_{inj4}. Therefore, we have $\omega_{inj} = \omega_{out}$ and $\omega_{in} = n\ \omega_{inj}$ (where n is the division ratio). In a conventional ILFD, V_{inj} has a sinusoidal function but in our proposed ILFD, it is formed by two narrow pulses in a period which are injected through two injection transistors for each stage. Every pulse that is shown in Figs. 4 and 6 as V_{inj3} can be approximated as a part of a sine wave with a large amplitude and a negative dc. Figure 8 shows this assumption. Two sine waves in this figure are the approximated voltages that is injected to one stage (e.g. V_{inj3} and V_{inj4}) which are $f(t) = A\cos(\omega_{inj}\,t) - B$ and $f'(t) = A\cos(\omega_{inj}\,t + \pi) - B$. In fact, only the upper segment of these waves is injected to the gate of the injection transistors (e.g. M_{inj3} and M_{inj4}). So, it can be assumed that V_{inj3} and V_{inj4} are added to create one injection signal $(V'_{inj}(t) = V_{inj3}(t) + V_{inj4}(t))$ which is injected to the gate of one injection transistor. Clearly, the frequency of $V'_{inj}(t)$ is twice that of the output frequency.

The Fourier series of two signals [$f(t)$ and $f'(t)$] are calculated in the desired time intervals and added to form $V'_{inj}(\text{t})$. Because of the output RC low pass filter, only the fundamental harmonic $(\omega_{inj} = \omega_{out})$ will remain at the output node. So, the desired harmonics of $V'_{inj}(\text{t})$ after mixing with $V_{out}(\text{t})$ are 0, ω_{inj} and $2\omega_{inj}$. The Fourier coefficients of these desired harmonics are provided in "Appendix". Therefore, the $V'_{inj}(\text{t})$ is expressed by:

$$\begin{aligned} V'_{inj}(t) &= a_0 + a_1\cos(\omega_{inj}t) + a_2\cos(2\omega_{inj}t) + a'_0 \\ &\quad + a'_1\cos(\omega_{inj}t) + a'_2\cos(2\omega_{inj}t) \\ &= 2a_0 + 2a_2\cos(2\omega_{inj}t) \end{aligned} \tag{4}$$

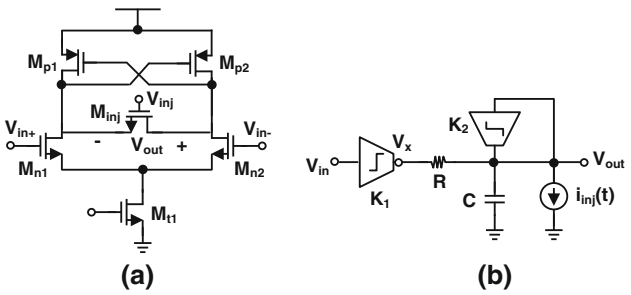

Fig. 7 **a** Circuit implementation of the delay cell, and **b** its behavioral model

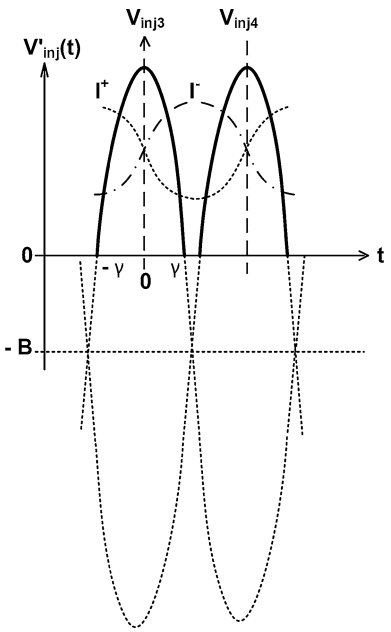

Fig. 8 Injection signal approximation

On the other hand, Fig. 8 shows the output voltage has a phase difference of $\pi/2$ with $f(t)$. So, the drain and source voltages of M_{inj} are equal to:

$$V_{Q+}(t) = V_{CM} + \frac{V_O}{2} sin(\omega_{inj} t) \tag{5}$$

$$V_{Q-}(t) = V_{CM} - \frac{V_O}{2} sin(\omega_{inj} t) \tag{6}$$

where V_{CM} is the dc value of $V_{Q+}(t)$ and $V_{Q-}(t)$. Due to the ac large-signal differential output voltage, the drain and source terminals of M_{inj} interchanges every half period. Therefore, the $V_{gs,inj}(t)$ and $V_{ds,inj}(t)$ are given by:

$$V_{gs,inj}(t) = 2a_0 + 2a_2 \cos(2\omega_{inj} t) - V_{CM} \pm \frac{V_O}{2} \sin(\omega_{inj} t) \tag{7}$$

$$V_{ds,inj}(t) = \pm V_O \sin(\omega_{inj} t) \tag{8}$$

The transistor M_{inj} is in the triode region at most of the times. Thus, the injection current is derived as follows:

$$i_{inj}^{+,-}(t) = \mu_n C_{ox} \left(\frac{W}{L}\right)_{inj} \left\{ 2a_0 + 2a_2 \cos(2\omega_{inj} t) - V_{CM} \pm \frac{V_O}{2} \sin(\omega_{inj} t) - V_{th} \right\} \times \left[\pm V_O \sin(\omega_{inj} t) \right] \tag{9}$$

The frequency of ω_{inj} remains at the output and the other harmonics are significantly attenuated with the cut-off frequency of the RC network. Therefore, the differential injection current is expressed by:

$$\begin{aligned} i_{inj,diff}(t) &= \eta \times [2a_0 - a_2 - (V_{CM} + V_{th})] \sin(\omega_{inj} t) \\ &= \eta \times \left[\frac{2}{\pi} \left(\frac{-A}{6} \sin(3\phi) + \frac{A}{2} \sin(\phi) + \frac{B}{2} \sin(2\phi) - B\phi \right) \right. \\ &\quad \left. - (V_{CM} + V_{th}) \right] \sin(\omega_{inj} t) \end{aligned} \tag{10}$$

where $\eta = 2V_O\ \mu_n C_{ox}(W/L)_{inj}$. We suppose that a low to high transition of the injection signal occurs at the time $t' = 0$. Under the locking condition, the propagation time of the delay cell changes to $t'_p = \pi/(N \cdot \omega_{inj}) = \pi/2\omega_{inj}$. So, we can write the following equation for the output voltage at t'_p:

$$V_{out}(t'_p) = V_O - 2V_O(1 - e^{-\frac{t'_p}{RC}}) - \eta\lambda \sin\left(\omega_{inj} t'_p - \angle Z\right) \times \frac{R}{\sqrt{1 + (\omega_{inj} RC)^2}} = 0 \tag{11}$$

where $\angle Z = \arctan(\omega_{inj} RC)$ and $\lambda = 2/\pi\ (-A/6 \sin(3\Phi) + A/2 \sin(\Phi) + B/2 \sin(2\Phi) - B\Phi) - (V_{CM} + V_{th})$. The argument of the arcsine function must be limited between -1 and 1. Therefore, the locking range formulation is expressed by:

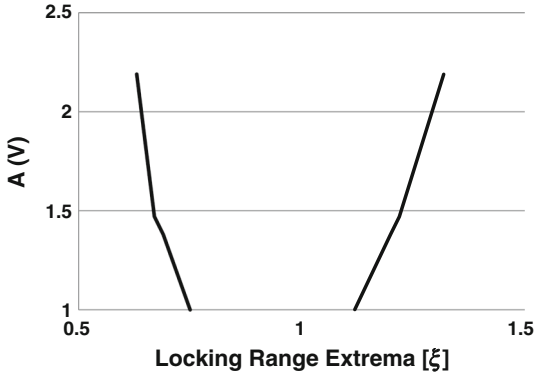

Fig. 9 Locking range extremes [ξ] versus A

$$\left| 2^{\frac{\xi - 1}{\xi}} - 1 \right| \sqrt{1 + \left(\frac{\pi}{2\ln(2)} \xi \right)^2} \leq \varepsilon |\lambda| \tag{12}$$

where $\xi = \omega_{inj}/\omega_0$ and $\varepsilon = \eta R/V_O = 2 \cdot \mu_n C_{ox}(W/L)_{inj} R$. Figure 9 shows the locking range extremes as a function of A by solving (12) numerically. It shows that by increasing the amplitude of the injection signal, A, the locking range is also increased. On the other hand, Figs. 4 and 6 show that the amplitude of the injection signal (V_{inj}) is much greater than the input signal (V_{in}). As a consequence, the locking range in the proposed ILFD is increased compared to the conventional ILFD.

In the proposed ILFD, as mentioned before, the frequency of $V'_{inj}(t)$ is twice the output frequency in both division ratios of 3 and 4. We know that a two-stage ring ILFD is a strong divide-by-2 circuit. So, our novel scheme by converting the divide-by-3 and divide-by-4 circuits to a divide-by-2 ring ILFD, provides wide locking ranges for 3 and 4 division ratios.

4 Proposed injection locked ring oscillators (ILROs)

One of the most critical features in an LO design is the generation of the quadrature signals. The image-reject and I/Q direct conversion receivers need quadrature LO inputs. Several structures have been suggested to meet this demand. Quadrature VCOs (QVCOs) need two inductors, and so, occupy large chip areas. Poly-phase filters are not suitable for wideband structures due to the signal attenuation. *RC-CR* filters create an amplitude error except for $f = 1/2\pi RC$. Divide-by-2 flip-flop circuits force the previous stages to work in the twice-higher frequency or need frequency doubler circuits before themselves, and hence, increase the power dissipation. The ILROs have the benefit of low power consumption, small chip area, and high phase accuracy. Therefore, in this section, two new ILRO circuits are proposed to provide a wide locking range for high frequency purposes with low power consumption.

4.1 Proposed ILRO (1)

In a two-stage differential ring oscillator, there is a 90° phase shift across each stage, and so, the outputs of the two stages are in the quadrature form. Therefore, we can use this circuit to produce the quadrature waveforms. An *RC-CR* filter followed by a two-stage ILRO is presented in [16] for quadrature generation. The proposed ILRO of this paper uses this topology with changing the structure of the ring oscillator delay cells. The proposed structure provides wider locking range and lower power consumption versus [16]. As it is seen from Fig. 10(a), the differential signal is fed to two *RC-CR* filters to create a low accuracy quadrature signal. Then, this signal is directly injected to a two-stage ring oscillator to increase the accuracy of the quadrature signal. Figure 10(b) shows the circuit schematic of the ILRO (1) delay cell. The injection signal is applied to the output nodes of the ring oscillator by using two differential pairs to convert the injection voltages into current and the load transistors add this current to the oscillator current, and hence, create the output signal.

The oscillator delay cell structure is obtained from [17]. In addition to the advantages of the circuit of [12], i.e. low power consumption and wide locking range, this structure has the benefit of increasing the operating frequency without any extra power consumption, by adding the diode-connected pMOS active loads. The oscillator loop-gain (without considering the injection circuit) can be expressed as:

$$H(s) = -\left[\frac{g_{mn1}}{(G_{ds} + g_{mp3} - g_{mp1}) + sC_L}\right]^2 \tag{13}$$

where $G_{ds} = g_{dsn1} + g_{dsp1} + g_{dsp3}$ is the transconductance due to the channel length modulation of transistors. Based on the *Barkhausen*'s phase condition, the value of $G_{ds} + g_{mp3} - g_{mp1}$ must be much lower than sC_L. The amplitude condition results in the free-running frequency given by:

$$f_{free-running} = \frac{1}{2\pi}\frac{\sqrt{g_{mn1}^2 - (G_{ds} + g_{mp3} - g_{mp1})^2}}{C_L} \tag{14}$$

This equation indicates that the maximum frequency occurs when $G_{ds} + g_{mp3} - g_{mp1}$ is close to the zero. The transistors M_{p1}–M_{p2} is used to cancel out the positive resistive load due to G_{ds}. But, usually their typical transconductance is much larger than G_{ds}. This is the reason of adding the diode-connected transistors (M_{p3}–M_{p4}) to get the maximum free-running frequency $g_{mn1}/(2\pi C_L)$ at the fixed power consumption [17]. The novelty of this paper is utilizing this structure in an ILRO circuit. Due to the highly nonlinear load block of the structure, its current gains a lot of harmonics that provides much wider locking range against [16] which it uses normal resistors as the load.

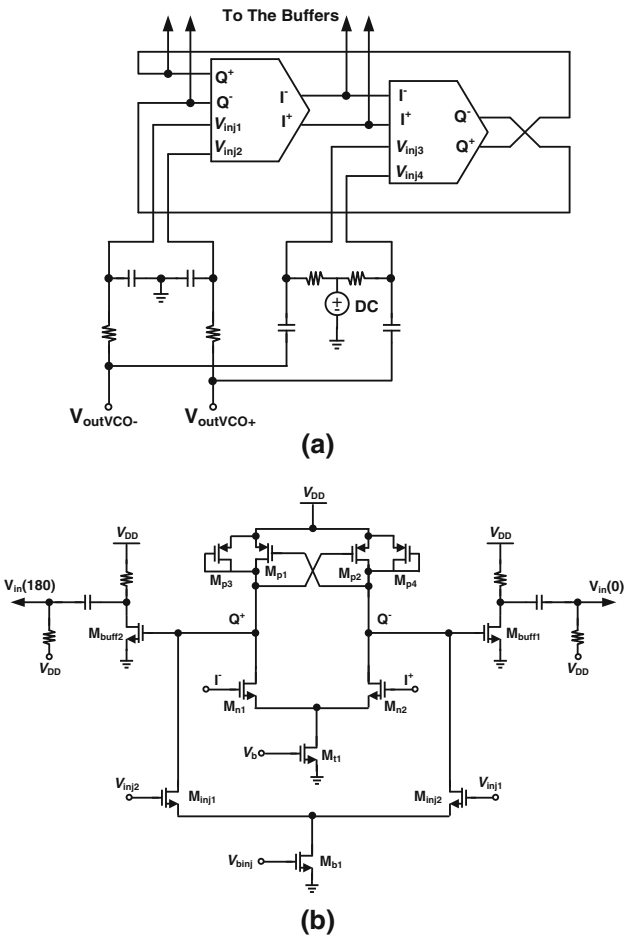

Fig. 10 Proposed ILRO for converting differential VCO outputs to the quadrature form: **a** The block diagram and **b** detailed schematic of one stage and the common-source stages for transferring output to the divide-by-3 circuit

4.2 Proposed ILRO (2)

As mentioned before, ILROs generate quadrature waveforms. Sometimes the injection signal does not have the phase accuracy or appropriate sinusoidal form. In this case, the proposed ILRO (1) is not a proper choice, because the signal is injected through a parallel differential pair directly to the oscillator output, it would adversely affect the output waveform and prevent the circuit to lock. This problem is solved by injecting the signal to the tail of the ILRO in the proposed ILRO (2).

As demonstrated in [2], the even order harmonics cause the duty cycle to deviate from the 50 % and also they are the main contributors of the quadrature phase mismatch. On the other hand, fundamental frequency and odd harmonics of the input signal are eliminated in the tail node of

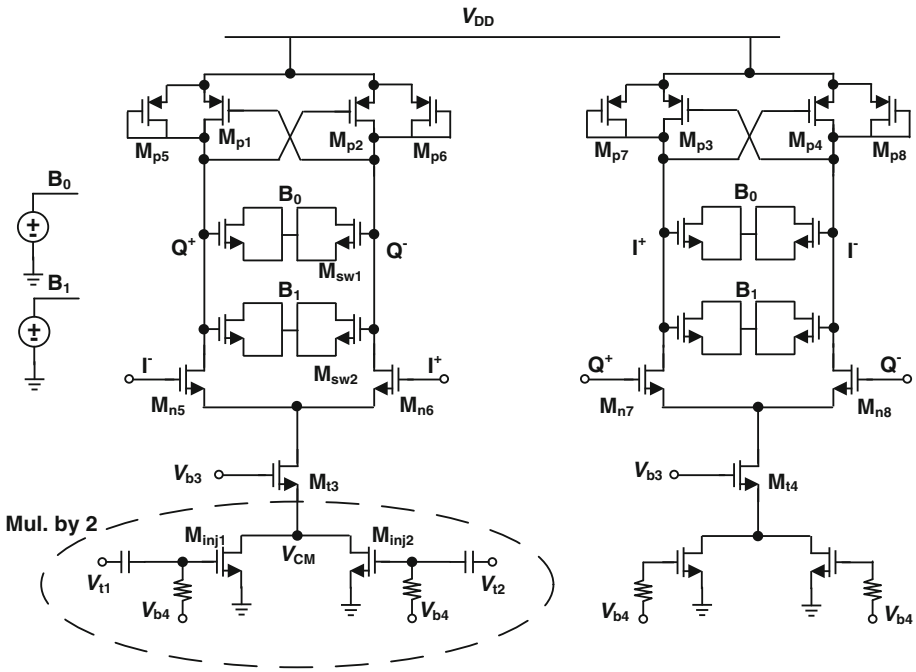

Fig. 11 Circuit schematic of the ILRO (2)

a differential pair, and so, the second order harmonic is amplified in this node [18, 19]. As a consequence, when the signal is injected to the tail, under the locking condition, the harmonics of the injection signal will be equal to the even order harmonics of the oscillation frequency. After mixing these harmonics with the output frequency by differential pair transistors, only the odd harmonics will remain at the output. Therefore, this will reduce the phase mismatch and the duty cycle deviations from 50 % [2].

The novel ILRO (2) consists of a frequency doubler and a divide-by-2 two-stage RILFD. This circuit is shown in Fig. 11. Two parallel transistors (M_{inj1} and M_{inj2}) are used to double the injection frequency. The resultant current from the frequency doubler is injected to a divide-by-2 RILFD via its tail transistor. So, the accurate quadrature form of the differential injected signal is generated at the ILRO (2) output. The delay cell structure and the number of ILROs stages are the novelties of ILRO (1) versus the ILRO which is proposed in [2]. The delay cell structure of the ILRO (2) is similar to the ILRO (1). So, it can produce higher frequencies with lower power consumption against the conventional delay cell structure used in [2]. Additionally, as mentioned in the previous section, the highly nonlinear load block of our ILROs delay cell will provide wide locking range versus the resistive load of [2]. Using a two-stage ring oscillator in the proposed ILRO (2) is another improvement of this circuit against the four-stage structure of [2] which causes to consume half power consumption.

Therefore, the ILRO (2) presents a wide locking range, low power consumption and high accuracy quadrature output circuit. The locking range of ILRO (2) is lower than ILRO (1), but it is a good choice for the injection signals with low phase accuracy and inappropriate sinusoidal form that ILRO (1) cannot support them.

5 LO circuit implementation

As shown in Fig. 1, a class-C LC VCO is utilized as the main core of the LO architecture to provide the frequency range of 7–10.5 GHz. The ILRO (1) converts the differential VCO output to the quadrature form and then the divide-by-3 circuit is employed to produce the frequency range of 2.3–3.5 GHz, by using the ILRO (1) output. The divide-by-2 and divide-by-4 circuits receive the output signal of the LC-VCO and cover the frequency range of 3.5–5.25 and 1.75–2.63 GHz, respectively. The tail signals of the divide-by-3 circuit which have twice the frequency of its outputs, are injected to the ILRO (2) circuit to provide the frequency range of 4.6–7 GHz in the quadrature form. The description of each building block is given below.

5.1 ILFDs

As mentioned before, the proposed LO architecture requires three dividers for division ratios of 2, 3 and 4. The proposed ILFDs of Sect. 3 are excellent choices for divide-by-3 and 4, because they have wide locking range, low power consumption and quadrature outputs. The required divide-by-2 circuit is replaced by a two-stage direct

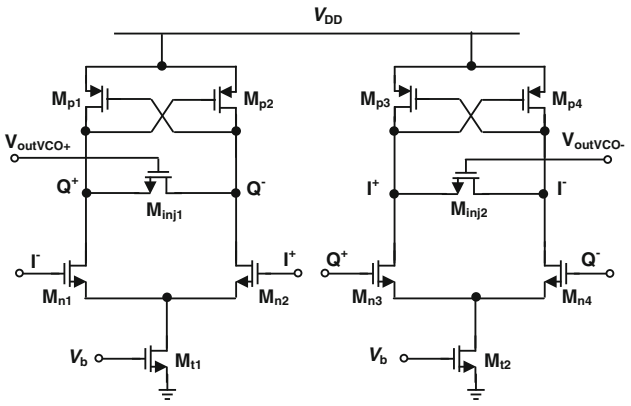

Fig. 12 Schematic of divide-by-2 circuit

injection RILFD which uses multi-phase injection to widen its locking range. This circuit is shown in Fig. 12.

5.2 ILRO (1)

The output signal of the LC VCO is differential, so the ILRO (1) is used to convert the differential signal to the quadrature form. Since the VCO provide a wide frequency range and also its output has an accurate sinusoidal waveform, using the ILRO (1) is a good choice for the quadrature generation.

5.3 ILRO (2)

The LO architecture presents a new method to provide the frequency range of 5.25–7 GHz in the frequency plan of Fig. 1. This range can be provided by doubling the divide-by-3 output frequency. Instead of using a frequency doubler to accomplish such purpose, the proposed architecture uses the signals at common-source nodes of the two stages of the divide-by-3 circuit to cover the desired frequency range. This technique reduces total power consumption and prevents the locking range reduction of the divide-by-3 circuit which is the result of loading effect of the frequency doubler on the divider.

However, the tail signals have low amplitude, inappropriate sinusoidal form, and they are in the differential form. So, we need a circuit to convert this signal to a proper quadrature form. As mentioned in Sect. 4.2, the ILRO (2) is appropriate to produce quadrature form of this type of signals. Therefore, the tails' signals of the divide-by-3 circuit are injected to ILRO (2) and an appropriate quadrature waveform with high phase accuracy is generated at the output.

In order to provide the desired frequency range in the different temperature variations and process corner cases, the circuit needs small varactors. Since this ILRO works with the parasitic capacitances, the technology varactors' sizes are large for this purpose. Thus, four nMOS transistors with small sizes are implemented as I-MOS varactors for each stage. This circuit can cover the desired frequency range with consuming low power.

5.4 LC-VCO

Figure 14 shows the schematic of the LC-VCO that is employed as the core of the proposed LO architecture. The class-C VCO that is proposed in [20] which has the benefit of low phase noise characteristic, is used in the LO architecture. The resonator of the VCO in Fig. 13, consists of a differential inductor (1 nH with $Q_{ind} = 14.1$), a pair of AC-coupled accumulation mode varactors (fine tuning) and a binary weighted switchable capacitor bank that contains four pairs of MIM capacitors (coarse tuning). To widen the tuning range, the differential tuning scheme of V_{tune} converter circuit which is proposed in [2], is used for varactors. In the coarse tuning part, in order to reduce the ohmic losses when the switch is ON, the size of the switches are chosen large enough. However, when the switch is OFF, it inserts large parasitic capacitances to the circuit. This problem has been solved by using two large resistors [21].

The amplitude of a wideband LC-VCO must be controlled, to avoid the waste of power [22] and the transition from the current-limited to the voltage-limited regimes by increasing the frequency [23]. Also, the proper activity of subsequent blocks depends on the amplitude stability. A digital automatic amplitude control circuit is proposed in [22]. The circuit presents a tail current source that uses the capacitor bank bits to send proper current to the VCO in any portion of the frequency range. The circuit is improved in [24] by changing the switches' places from the gate to the drain, and so, reducing the phase noise. This circuit approach is also utilized in this paper as shown in Fig. 13.

Two buffers are used to transfer the VCO output signal to the subsequent circuits. Since the required bias voltage for ILRO (1) and divide-by-2 circuits is different from the divide-by-4 circuit, two coupling capacitors are employed to transfer the signal with proper bias voltages (V_{b1} and V_{b2}).

6 Simulation results

The proposed circuits are designed and simulated in a 90-nm CMOS technology with a single 1.2 V power supply by using the Spectre RF simulator. In this section, firstly the simulation results for each block is presented and the proposed dividers are compared with some state-of-the-art ring ILFDs. Then, the simulation results of the proposed LO architecture are provided.

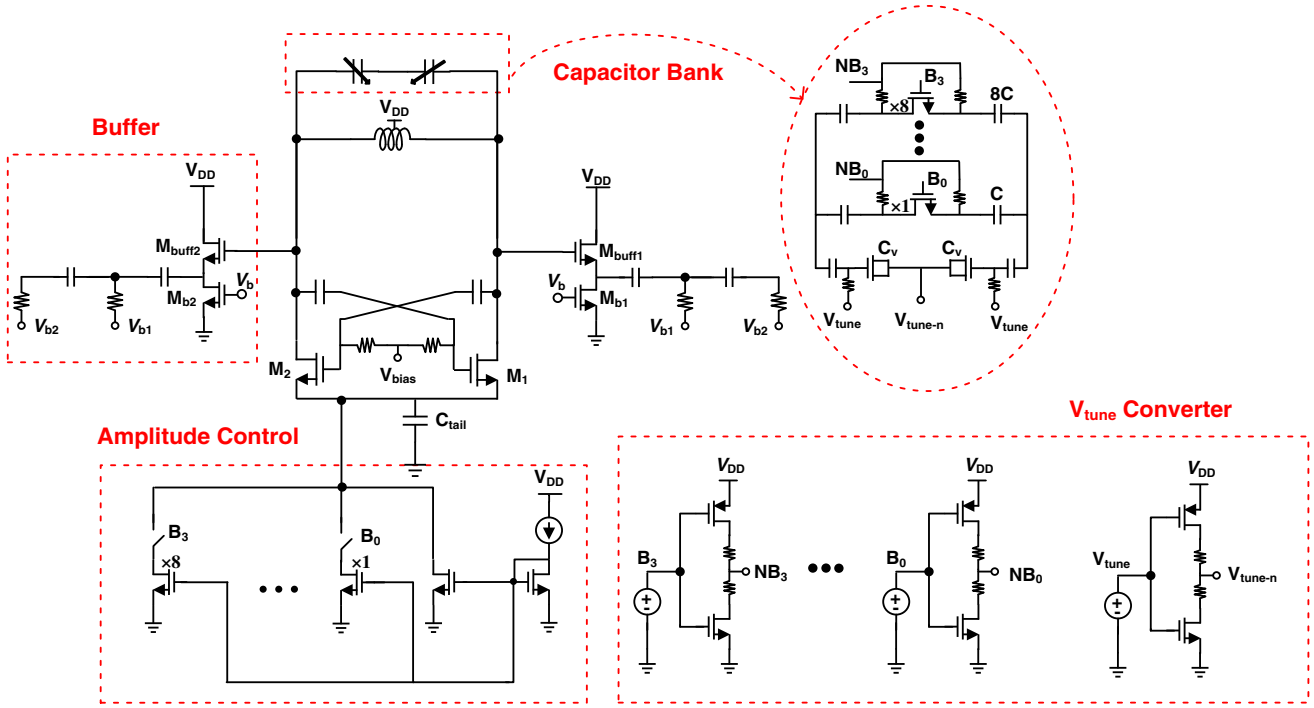

Fig. 13 Schematic of the LC-VCO and the buffers

The sensitivity curves of the proposed ILFD under different bias conditions for division ratios of 3 and 4 are shown in Fig. 14(a), (b), respectively. The input dc voltage for both circuits is considered 1.2 V which is equal to the LC-VCO output dc voltage in the LO structure. These results are achieved for $DC_p = 0.9$ V and $DC_n = 0.75$ V in the case of divider 3 and for $DC_p = 1$ V and $DC_n = 0.8$ V in the case of divider 4. The DC_p and DC_n bias voltages determine the width of the injection pulses. For a higher DC_p, the injection pulses are narrower, because the time interval where V_{SG} of $M_{p,f}$ is higher than the threshold voltage is less, and so, $M_{p,f}$ will be ON in less times. On the other hand, for a similar input frequency, the output period of the divide-by-4 circuit is larger than that of the divide-by-3 circuit. Therefore, for making narrower pulses for divide-by-4 circuit, a larger value of DC_p is needed. The figures show the best locking range of 4.5–12.8 GHz (95.95 %) at $V_b = 0.55$ V for divide-by-3 and locking range of 5.7–12.6 GHz (75.4 %) at $V_b = 0.53$ V for divide-by-4 at the injection voltage $V_{\text{inj,pp}} = 0.632$ V.

Table 1 summarizes the simulation results of the proposed ILFDs in different process corner cases and temperature variations. It indicates the ability of the proposed circuits to preserve their characteristics in the different conditions. Also, the simulation results of the divide-by-2 circuit are also given in this table for summarizing. A comparison between the proposed divide-by-3 circuit and the state-of-the-art ILFDs is given in Table 2. The results show a large locking range of the proposed ILFD compared

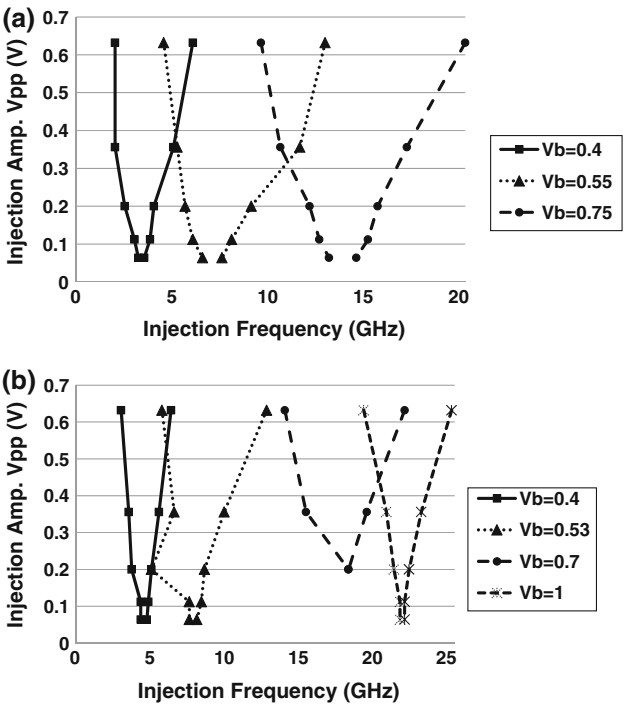

Fig. 14 **a** Sensitivity curves of the proposed ILFD, under different bias conditions, in the case of **a** divide-by-3 and **b** divide-by-4

with the others. The following figure of merit (FoM) is used for a more accurate comparison [29]:

$$FoM_T = \frac{[\text{Locking range}(\%) \times \text{Division number}]}{P_{dc}(\text{mW})} \quad (15)$$

Table 1 Simulation results of the proposed ILFDs in different process and temperature corner cases

	$V_{inj,pp}$ (V)	Div. num.	Freq. range (GHz)	Locking range (%)	P_{diss} (mW)
TT, 27 °C	0.632	4	5.7–12.6	75.4	1.35
SS, 85 °C			6–12.3	68.85	1.18
FF, −40 °C			5.5–13	81	1.48
TT, 27 °C	0.632	3	4.5–12.8	95.95	1.47
SS, 85 °C			4.3–12.6	94.7	1.22
FF, −40 °C			4–13	105.88	1.28
TT, 27 °C	0.632	2	3–18	142.9	0.9
SS, 85 °C			3.5–15	124.3	0.93
FF, −40 °C			3–24	155.5	1.12

where P_{dc} is the dc power dissipation and the locking range is calculated as:

$$LR = [2(f_{max} - f_{min})/(f_{max} + f_{min})] \times 100\% \quad (16)$$

Although the proposed divide-by-3 circuit does not show a very high FoM, but this circuit has the advantage of quadrature output where most of the divide-by-3 ILFDs do not have it. Especially some of these dividers with high FoM have single outputs, and so, they are not very operational.

A performance comparison between the proposed divide-by-4 circuit and some of the best state-of-the-art ILFDs is given in Table 3. The wide locking range and low power dissipation of our ILFD is distinguished among the others.

For the ILRO (1), the cut-off frequency of the *RC-CR* filter is chosen around the middle of the LC VCO tuning range (9 GHz), due to the less signal attenuation by filters at the ends of the frequency interval. The values of V_{binj} and *DC* should be set in such a way that differential pair's transistors operate in the saturation region. In this design, these values are set to 0.5 and 0.66 V, respectively.

The simulation results of two proposed ILROs in different process corner cases and temperature variations are summarized in Table 4. The locking range of 5–28 GHz (139.4 %) at the injection voltage of $V_{inj,pp} = 0.632$ V, with 4.797 mW power consumption for the ILRO (1) are achieved showing a circuit with excellent features. This locking range is achieved for the output voltage higher than 0.1 V.

Since the input signal of the ILRO (2) in the LO structure is taken from the tail node, it has a low amplitude. So, we simulate the circuit at the injection voltage $V_{inj,pp} = 0.2$ V. Table 4 shows the locking range of 5–8 GHz (46.2 %) that is sufficient for the proposed LO architecture. This table also indicates the stability of the ILROs in different conditions.

Figures 15, 16 and 17 show the output phase noise of each block in the LO architecture at the frequency of 9 GHz at different process corner cases including TT @ 27 °C, SS @ 85 °C and FF @ −40 °C, respectively. According to the Eq. (1), there is a $20 \times \log(N)$ phase noise reduction at the output of a divide-by-*N* ILFD. So, as it is seen from Fig. 15, there are 0, 6, 9.5, 12 and 3.5 dB phase noise reduction at the outputs of ILRO (1), divider 2, divider 3, divider 4, and ILRO (2), respectively. The input signal frequency of the ILRO (2) is twice the frequency of the divider 3. Thus, its output phase noise is obtained from a 9.5 dB reduction and 6 dB increment from the input phase noise. These figures show a little difference between the output phase noise in the PVT conditions.

Figure 18 plots the LO phase noise at 1 MHz offset frequency across the desired frequency range (1.75–10 GHz) in the PVT conditions. The phase noise changes are from −109.1 dBc/Hz (from LC-VCO) to −127.2 dBc/Hz (from divider 4) at TT @ 27 °C. The figure also shows a little change from these values in the PVT conditions. Figure 19 plots the simulated LO quadrature phase mismatch for the output of each circuit, in the case of $f_{VCO} = 9$ GHz for 100 Monte-Carlo iterations. It is clear that the injection locking technique corrects the phase noise of the oscillator. The output signal of the ILRO (2) has three phase correction steps in the chain of ILRO (1), divider 3 and ILRO (2). So it has the minimum I/Q imbalance among the others as it is seen from Fig. 19. The Monte-Carlo simulations show that the mismatch of devices has very low effect on the output phase mismatch.

Table 2 Performance comparison between the proposed divider 3 and state-of-the-art divide-by-3 ring ILFDs

	Tech. (nm) CMOS	V_{DD} (V)	$V_{inj,pp}$ (V)	Freq. range (GHz)	LR (%)	P_{diss} (mW)	Output type	FOM (%/mW)
This work	90	1.2	0.632	4.5–12.8	95.9	1.47[1]	Quad.	195.8
[13]	90	–	0.632	3.6–5.4	40	9.6[2]	Quad.	–
[25]	180	1	0.632	5.6–7.2	25	0.24	Single	312.5
[26]	180	1.8	0.651	8.28–11.48	32.4	1.67[3]	Quasi diff.	58.2
[27]	180	1	0.632	2.6–3.6	33	0.4	Single	247.5
[28]	180	1.8	0.4	1.2–4.9	121	0.74	Single	490.5

[1] Core P_{diss} only, [2] $P_{diss,min}$ for whole of the structure, [3] minimum P_{diss}

Table 3 Performance comparison between the proposed divider 4 and state-of-the-art divide-by-4 ring ILFDs

	Tech. (nm) CMOS	V_{DD}	$V_{inj,pp}$ (V)	Freq. range (GHz)	LR (%)	P_{diss} (mW)	FOM (%/mW)
This Work	90	1.2	0.632	5.7–12.6	75.4	1.35[1]	223.4
[7]	65	1.2	0.632	9.9–13.7	31.8	3.9	32.61
[8]	130	1.2	0.632	22.5–29	25.2	6	16.8
[13]	90	–	0.632	4.9–7.1	36.7	9.6[2]	–
[30]	180	1.8	0.632	1.6[3]	22.2	6.8	13.06
[31]	180	1.8	0.632	5.39–6.12	6.3	–	–
[32]	130	1.2	0.474	3.6–5.25	37.3	0.35[1]	426.3

[1] Core P_{diss} only, [2] $P_{diss,min}$ for whole of the structure, [3] centre frequency

Table 4 Simulation results of the proposed ILROs in different process and temperature corner cases

	Circuit	$V_{inj,pp}$ (V)	Freq. range (GHz)	Locking range (%)	P_{diss} (mW)
TT, 27 °C	ILRO (1)	0.632	5–28	139.4	4.797
SS, 85 °C			5–16.8	108.2	4.128
FF, −40 °C			7–36	134.9	5
TT, 27 °C	ILRO (2)	0.2	5–8	46.2	1.2
SS, 85 °C			5.2–7	29.5	1.16
FF, −40 °C			4.5–8.8	64.7	1.32

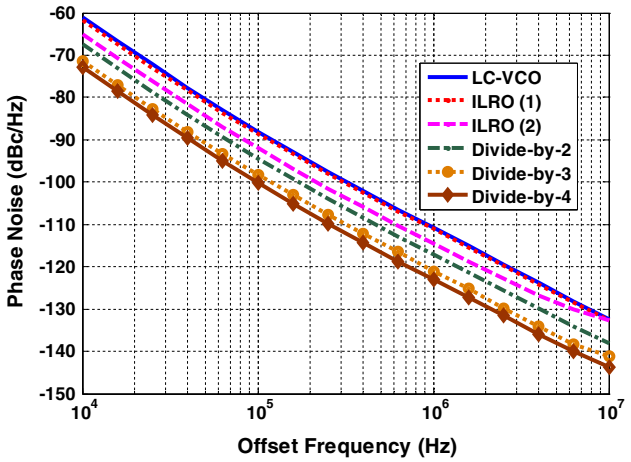

Fig. 15 Output phase noise of the LO architecture building blocks in TT, 27 °C @ $f_{VCO} = 9$ GHz

As mentioned in previous sections, two buffers are used at the LC-VCO output and four common-source stages at the ILRO (1) output to transfer the signal to the subsequent circuits. The simulated power dissipation of these two parts are 4.18 and 7.73 mW, respectively. So, the total power dissipation of the LO structure in the frequency range of 1.75–10 GHz is 23.196–26.84 mW at TT @ 27 °C, 20.412–23.38 mW at SS @ 85 °C and 26.2–30.25 mW at FF @ −40 °C.

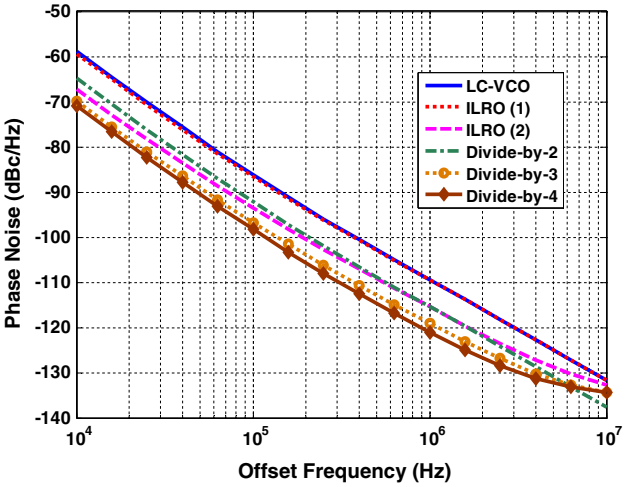

Fig. 16 Output phase noise of the LO architecture building blocks in SS, 85 °C @ $f_{VCO} = 9$ GHz

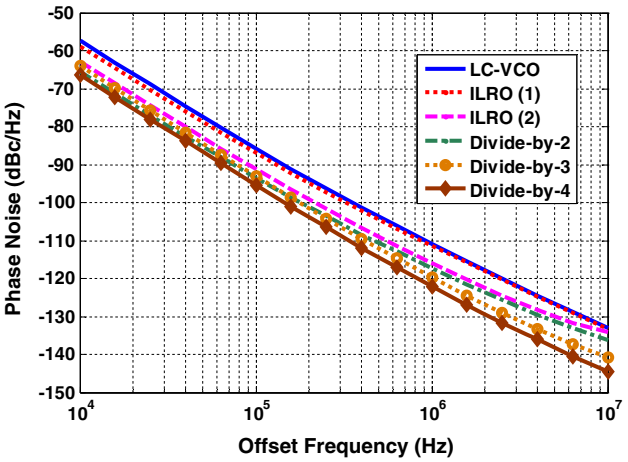

Fig. 17 Output phase noise of the LO architecture building blocks in FF, −40 °C @ $f_{VCO} = 9$ GHz

Table 5 compares this work with several other state-of-the-arts that produced wide tuning range with quadrature LOs. The difference between the frequency ranges makes

Table 5 Performance comparison between the proposed LO architecture and several state-of-the arts

	Tech. (nm)	Architecture	f_{VCO} (GHz)	FTR[1] (%)	f_{LO} (GHz)	Worst phase noise[2]	P_{diss} (mW)
This Work	90 CMOS	1 × LCVCO ILFD 2,3,4, 2 × ILRO	6.86–10.58	42.66	1.75–10	−109.1 @ f_{LO} = 10 GHz	23.196–26.84
2012, JSSC [2]	65 CMOS	1 × LCVCO Div.2,3, ILRO	14.6–22.2	41.3	4.9–11.1	−104 @ f_{LO} = 10 GHz	22
2011, ISSCC [33]	130 CMOS	1 × Q-LCVCO SSBM, Div.s	3–4.2 and 8.4–12	33.3 and 35.3	0.05–10[3]	−101@ f_{LO} = 10 GHz	33–83[4]
2010, JSSC [34]	90 CMOS	1 × Q-LCVCO SSBM, Div.2,3,5	7 and 8.75		1–10	−95@ f_{LO} = 8.75 GHz	31
2011, MWSCAS [13]	90 CMOS	1 × LCVCO 1 × ILFD, 7 × FF Div.s	7.8–10.5	29.5	0.01–7.8	−111.4@ f_{LO} = 8.15 GHz	9.6–15.6
2009, RFIC [35]	45 CMOS	2 × LCVCO Div.2 only	4–7.2 and 7–10	57.1 and 35.3	0.1–5	−111 @ f_{LO} = 7.2 GHz	19.8[5]
2005, JSSC [36]	130 CMOS	1 × Q-LCVCO SSBM, Div.s	2.6–3.9	40	0.87–2.6	−120 @ f_{LO} = 2.5 GHz	37.8
2011, JECE [37]	180 CMOS	1 × LCVCO SSBM, 2 × Div.2	2.2–3.3	40	0.98–6.64	−117@ f_{LO} = 5.12 GHz	4.41–26.9
2011, JSSC [38]	180 SiGe BiCMOS	1 × Fractional-N Synthesizer, 5 × Div.2, 2 × Mul.2	4–8[6]	66.67	0.125–32	−101 @ f_{LO} = 28 GHz	284–498[4]
2011, JSSC [39]	130 CMOS	1 × QVCO, HR-SSBM, Div. 2,4	3.42–5.45	45.77	1.8–6	−115 @ f_{LO} = 5.18 GHz	35.6–52.62[4]
2012, ASSCC [40]	65 CMOS	1 × LCVCO, 1 × Fractional-N ILFD, Div.s	7.2–10.3	35.4	0.01–6.6	−108 @ f_{LO} = 6.6 GHz	16–26

[1] FTR (%) = 100 % × 2 × $(f_{max} - f_{min})/(f_{max} + f_{min})$

[2] Unit: dBc/Hz @ 1 MHz Offset

[3] Other higher frequency band not listed

[4] Whole PLL

[5] VCO only

[6] Core synthesizer

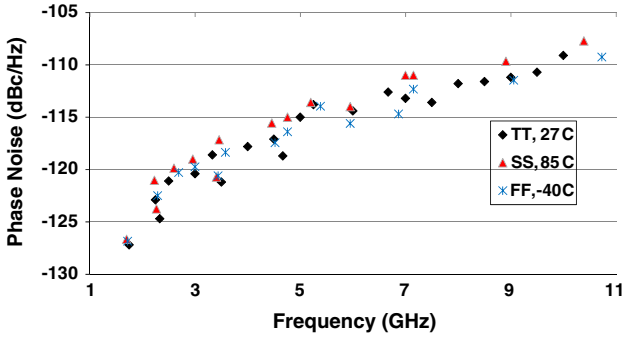

Fig. 18 Phase noise @ 1 MHz offset versus LO frequency in corner cases

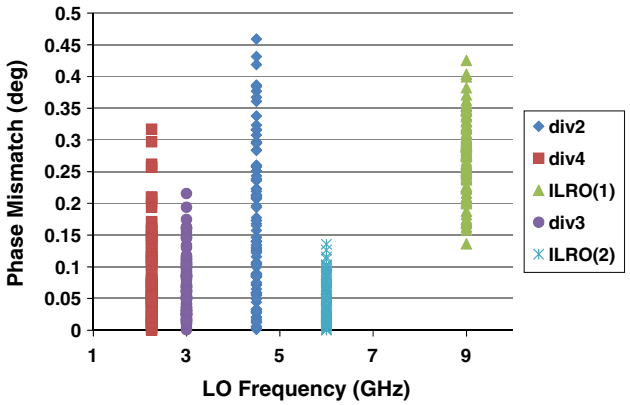

Fig. 19 Quadrature mismatches versus the LO frequency

the comparison difficult. But the results indicate that our architecture with wide frequency range, low phase noise, low power consumption and single LC-tank has a very good performance among the others. However, our results are achieved from the simulations while the other papers listed in the Tables 2, 3 and 5 present the measurement results and this is not a fair comparison. But, we have provided the simulation results for the different process corner cases, so it can be assert if this circuit is fabricated, it still will be one of the best LO architectures for CR applications. Moreover, the performance of the proposed LO architecture will be also comparable with the best alternative ones even some performance degradation is happen after the fabrication.

7 Conclusions

In this paper, novel RILFD and ILRO circuits are presented. The proposed ILFDs provide the division ratios of 3 and 4. They have the benefit of wide locking range, low power consumption, and quadrature output without needing extra control mechanisms. The wide locking range and low power consumption are the key advantages of the proposed ILROs that are used in the quadrature signal generation. These circuits have been utilized in a new CR LO architecture and their proper operation are asserted. The simulation results clearly demonstrated the wide locking range, low power consumption and low quadrature mismatch of the proposed ILFDs and ILROs and their potential for the design of a compact, low power and quadrature CR LO architecture.

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Appendix

The desired Fourier coefficients of $f(t) = A\cos(\omega_{inj}\, t) - B$ are as follows:

$$a_0 = \frac{2}{T_{inj}}\int_0^{\gamma}(A\cos(\omega_{inj}t) - B)dt = \frac{1}{\pi}\int_0^{\phi}(A\cos(\phi') - B)d\phi' = \frac{1}{\pi}[A\sin(\phi) - B\phi] \quad (17)$$

$$a_1 = \frac{2}{\pi}\int_0^{\phi}(A\cos(\phi') - B)cos(\phi')d\phi' = \frac{2}{\pi}\left[\frac{A}{4}\sin(2\phi) + \frac{A}{2}\phi - B\sin(\phi)\right] \quad (18)$$

$$a_2 = \frac{2}{\pi}\int_0^{\phi}(A\cos(\phi') - B)cos(2\phi')d\phi' = \frac{2}{\pi}\left[\frac{A}{6}\sin(3\phi) + \frac{A}{2}\sin(\phi) - \frac{B}{2}\sin(2\phi)\right] \quad (19)$$

where $\Phi = \omega_{inj}\cdot\gamma$. For $f'(t) = A\cos(\omega_{inj}\, t + \pi) - B$, the desired Fourier coefficients are given by:

$$a_0' = \frac{1}{\pi}\int_{\pi}^{\pi+\phi}(-A\cos(\phi') - B)d\phi' = \frac{1}{\pi}[A\sin(\phi) - B\phi] \quad (20)$$

$$a_1' = \frac{2}{\pi}\int_{\pi}^{\pi+\phi}(-A\cos(\phi') - B)cos(\phi')d\phi' = \frac{-2}{\pi}\left[\frac{A}{4}\sin(2\phi) + \frac{A}{2}\phi - B\sin(\phi)\right] \quad (21)$$

$$a_2' = \frac{2}{\pi}\int_{\pi}^{\pi+\phi}(-A\cos(\phi') - B)cos(2\phi')d\phi' = \frac{2}{\pi}\left[\frac{A}{6}\sin(3\phi) + \frac{A}{2}\sin(\phi) - \frac{B}{2}\sin(2\phi)\right] \quad (22)$$

These equations show that $a'_0 = a_0$, $a'_1 = -a_1$ and $a'_2 = a_2$.

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