Analog Integr Circ Sig Process (2014) 80:195–208
DOI 10.1007/s10470-014-0332-y

Design of CMOS three-stage amplifiers for fast-settling switched-capacitor circuits

Sajad Golabi · Mohammad Yavari

Received: 3 January 2014 / Revised: 8 May 2014 / Accepted: 9 May 2014 / Published online: 25 May 2014

Abstract In this paper, a time-domain design procedure for fast-settling three-stage amplifiers is presented. In the proposed design approach, the amplifier is designed to settle within a specific time with a given settling accuracy and circuit noise budget by optimizing both the power consumption and silicon die area. Both linear and nonlinear settling regions of three-stage amplifiers are considered and optimal values of the amplifier stages transconductance and compensation capacitors are obtained using the genetic algorithm optimization. Detailed design equations are provided and circuit level simulation results using a 90 nm CMOS technology are presented to evaluate the usefulness of the proposed design scheme respected to the previously reported design approaches.

Keywords Three-stage operational amplifiers · Nested Miller compensation · Small-signal and large-signal settling times · Circuit noise · Switched-capacitor circuits

1 Introduction

Three-stage amplifiers are recently used to achieve simultaneously high dc gain and large output signal swing in low-voltage nano-meter CMOS technologies [1–3]. To ensure their closed-loop stability, the nested Miller compensation (NMC) and reversed nested Miller compensation (RNMC) techniques are mainly utilized [4]. To overcome the inherent limits of three-stage amplifiers, several variants of the basic NMC and RNMC schemes have been proposed such as those reported in [5–13]. Most of these techniques have been optimized to drive large capacitive loads which are widely used in low-dropout (LDO) voltage regulators [9, 13]. On the other hand, in high-speed switched-capacitor circuits, the load capacitance is small and the amplifier is needed to settle within a specific time with a desired settling accuracy. Therefore, the transient settling performance is among the most critical aspects of high-speed amplifiers used in switched-capacitor circuits. This issue has not been extensively considered in literature. There are only a few publications considering the settling performance in the design optimization of multistage amplifiers [14–21].

In [14], the required value of gain bandwidth, slew rate, and noise budget are considered as the design parameters and then the device components are sized. Hence, this is not an optimized design scheme for settling purposes. It is worth mentioning that the design of a single-stage amplifier based on the unity-gain bandwidth and slew rate results in a fast-settling behavior, but, this is not true in multistage amplifiers where the settling performance can also be superior to the single-stage amplifiers as theoretically explored in [22].

In [15], a capacitor sizing rule based on the damping factor of the open-loop transfer function has been presented to realize a fast-settling three-stage amplifier. The value of compensation capacitors and small-signal settling time of a three-stage NMC amplifier are optimized in [16] for a given amplifier stages transconductance, and hence, for a given power dissipation budget. But, this is not a complete design procedure since it does not support the optimization of all device parameters including the amplifier stages transconductance for a given settling time and accuracy. This technique was also extended for other NMC-based three-stage amplifiers in [17]. In [18], the damping factor

S. Golabi · M. Yavari (✉)
Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran
e-mail: myavari@aut.ac.ir

of the non-dominant poles in the open-loop transfer function was considered as a single parameter to design fast-settling three-stage NMC amplifiers. This approach needs an initial design based on the heuristic choice of device sizes without considering the power consumption. The final design is refined through extensive Spice simulations. Therefore, in this paper, it is not reported any design optimization of the device parameters.

In [19], the closed-loop poles and zeros are optimized to minimize the required power consumption for a given settling time and accuracy. Nonetheless, the circuit noise and amplifier large-signal settling behavior is not considered in the design scheme. A complete design methodology is reported in [20], but it is presented for two-stage amplifiers with cascode compensation. The proposed design procedure in [21] minimizes the total integrated noise of a three-stage amplifier by constraining on power consumption and small-signal settling time. This design scheme is rather complicated and many design variables are utilized. Although an automated optimization program was employed to find the optimal solution, a good initial starting point based on the design heuristics is still needed.

In this paper, a new design scheme is presented for three-stage amplifiers by optimizing the closed-loop poles and zeros to minimize the required power consumption and silicon die area for a given settling time and accuracy and circuit noise budget. Both linear and nonlinear settling behaviors of three-stage amplifiers are considered here where in [14–19, 21] only the linear settling time has been considered. It is worth mentioning that although the slewing behavior of a class A amplifier is well understood, but it considerably affects the settling time in switched-capacitor circuits, and so, it should be included in the design procedure. The genetic algorithm is used in the optimization of device parameters. The genetic algorithm is a global optimization method, and hence, unlike the design scheme in [21], there is no need for an initial starting point to solve the optimization problem. By obtaining the related expressions for power consumption, settling time, and total integrated noise of a three-stage amplifier only as a function of the closed-loop pole and zero locations, the number of design variables is reduced resulting in a simplified design approach. Although the detailed design procedure and equations are presented for the basic three-stage NMC amplifier, but the proposed design scheme can also be employed in the other variations of three-stage amplifiers which are well described by a third-order transfer function with a straight forward extension. Hence, it is applicable to the most of three-stage amplifiers.

The paper is organized as follows. In Sect. 2, the basic block diagram and a typical fully-differential circuit implementation of the three-stage NMC amplifier are described. In Sect. 3, the proposed design procedure and the detailed design equations are presented. A design example and extensive circuit level simulation results are provided in Sect. 4. Finally, Sect. 5 concludes the paper.

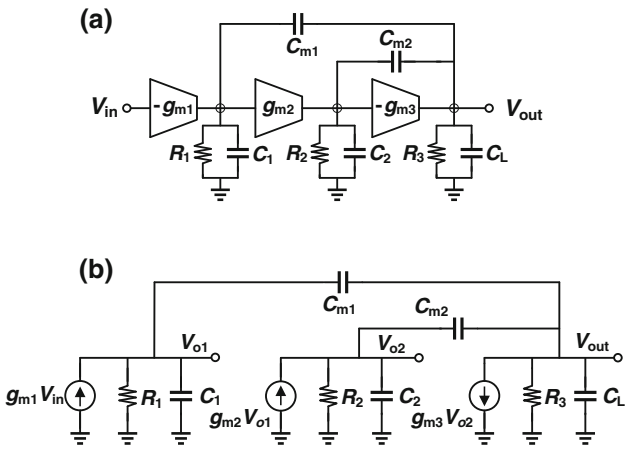

Fig. 1 **a** Block diagram and **b** small-signal model of the basic three-stage NMC amplifier

2 Three-stage NMC amplifier

The basic block diagram and the small-signal model of a three-stage NMC amplifier are shown in Fig. 1 where g_{mi}, C_i, and R_i represent the i^{th} stage transconductance, the equivalent parasitic capacitance, and the output resistance of the corresponding gain stages, respectively. C_L includes the load capacitor as well as the output parasitic capacitance of the amplifier's third stage. The capacitors C_{m1} and C_{m2} perform the nested Miller compensation in order to split the frequency poles and provide a dominant pole to ensure the closed-loop response stability [4, 5].

A typical fully-differential circuit implementation of a three-stage NMC amplifier is shown in Fig. 2 where three differential pairs with active loads are used to realize the amplifier stages. Using three identical gain stages similar to the first stage is another way to implement the NMC amplifier as presented in [2]. But, the implemented NMC amplifier in Fig. 2 has a large output voltage swing since the tail current-source transistor in the last stage is removed. Two independent switched-capacitor common-mode feedback (CMFB) circuits are used to define the output common-mode voltage of the amplifier stages. The first CMFB circuit determines the output common-mode voltage of the first stage and the second one fixes the output common-mode voltage of both second and third stages in the same CMFB loop. In the second CMFB circuit, the common-mode control signal is inverted to provide a negative feedback loop. The appropriate value of

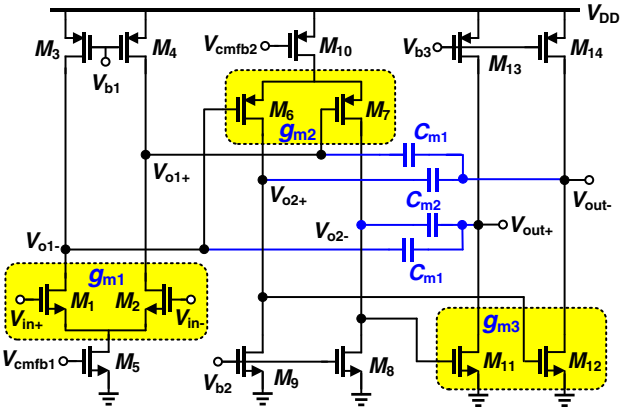

Fig. 2 A fully-differential circuit implementation of a three-stage NMC amplifier (bias and CMFB circuits are not shown for simplicity)

capacitors in switched-capacitor CMFB circuits is chosen based on the following design heuristics. Since they load the amplifier in the differential mode, the capacitors should not be too large. On the other hand, they should not be too small; otherwise the parasitic capacitances cannot be neglected and the CMFB loop gain will be reduced. The first CMFB circuit is a single-stage amplifier which is compensated by the total load capacitance of the first stage. The second CMFB circuit is a two-stage amplifier compensated by C_{m2}. In other words, C_{m2} also provides the Miller compensation to ensure the stability in the second CMFB circuit. A constant-g_m biasing circuit is used to make the transistors transconductance independent on the power supply voltage as well as the process and temperature variations [23]. It should be noted that the main amplifier and the bias circuit are not independent of each other. The transconductance and current of the biasing transistors are a small fraction of the main amplifier corresponding transistors. Therefore, by optimizing the main amplifier, the biasing circuit is also optimized.

By assuming high dc gain in amplifier stages and compensation and load capacitors are much greater than all circuit parasitic capacitances, i.e. $g_{mi}R_i \gg 1$ and C_L, C_{m1}, $C_{m2} \gg C_{1,2}$, and using the model shown in Fig. 1(b), the closed-loop small-signal transfer function of the three-stage NMC amplifier is obtained as:

$$A_v(s) \approx \frac{1}{\beta} \frac{1 - sC_{m2}/g_{m3} - s^2 C_{m1}C_{m2}/g_{m2}g_{m3}}{1 + s\left(\frac{C_{m1}}{\beta g_{m1}} - \frac{C_{m2}}{g_{m3}}\right) + s^2\left(\frac{g_{m3} - g_{m2} - \beta g_{m1}}{\beta g_{m1}} \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}\right) + s^3 \frac{C_{m1}C_{m2}C_L}{\beta g_{m1}g_{m2}g_{m3}}}, \quad (1)$$

where β is the feedback factor. The amplifier gain-bandwidth product (ω_{GBW}) is well approximated by the open-loop unity-gain frequency as $\omega_{GBW} = g_{m1}/C_{m1}$. As it is seen, the closed-loop transfer function has two zeros and three poles. The location of poles cannot be easily obtained as a function of the circuit parameters, but the location of zeros can be readily obtained as:

$$\omega_{z,LHP} = -\frac{g_{m2}}{2C_{m1}}\left(\sqrt{1 + \frac{4g_{m3}C_{m1}}{g_{m2}C_{m2}}} + 1\right), \quad (2)$$

$$\omega_{z,RHP} = \frac{g_{m2}}{2C_{m1}}\left(\sqrt{1 + \frac{4g_{m3}C_{m1}}{g_{m2}C_{m2}}} - 1\right). \quad (3)$$

One of the zeros is placed at the right half plane (RHP) and the other one is a left half plane (LHP) zero. The LHP zero is located at a higher frequency than the RHP zero. The RHP zero reduces the phase margin and can possibly degrade the stability of the closed-loop amplifier. The magnitude of the RHP zero should be equal or greater than that of the open-loop non-dominants poles [5]. To alleviate the RHP zero effect, different modifications of the basic three-stage NMC amplifier have been proposed such as [5, 24]. In [5], a nulling resistor is placed in series with the compensation capacitors and it is called the NMCNR amplifier. By this way, the location of RHP zero can be changed by properly choosing the value of the nulling resistor.

3 Proposed design procedure

In this section, firstly the small-signal and large-signal settling times, total integrated noise, and power consumption of the three-stage NMC amplifier are formulated. Then, an automated design procedure is presented to find the optimal solution of the design variables.

3.1 Small-signal settling

In order to investigate the small-signal settling behavior of a three-stage NMC amplifier, the amplifier accurate step response using the closed-loop transfer function should be obtained. But, using the small-signal closed-loop transfer function given in (1) to derive the amplifier step response is complicated since the location of poles are not known as a function of the circuit parameters. Therefore, the following standard transfer function is considered:

$$H(s) = H_0 \frac{(s + z_1\zeta\omega_n)(s + z_2\zeta\omega_n)}{(s + \alpha\zeta\omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)}. \quad (4)$$

This standard transfer function has three poles and two zeros. ω_n and ζ are called the natural frequency and damping factor of the complex poles, respectively. The frequency zeros and the real pole have been normalized with respect to the real part of complex poles with the normalization factors of z_1, z_2, and α respectively. z_1 and z_2

are considered to be the normalized LHP and RHP zeros, respectively. So, the value of z_1 is positive ($z_1 > 0$) and the value of z_2 is negative ($z_2 < 0$). According to (4), there are five different system parameters determining the small-signal settling performance of the system.

The system step response can be derived using the inverse Laplace transformation as:

$$s(t) = L^{-1}\left[\frac{A_0}{s}H(s)\right], \tag{5}$$

where A_0 is the amplitude of the input step. The dynamic settling error is defined as $\varepsilon_s(t) = (s(\infty)–s(t))/s(\infty)$, in which $s(t)$ and $s(\infty)$ are the step response and the steady state value of the step response, respectively. Thus, the dynamic settling error is obtained as:

$$\varepsilon_s(t) = a_1 e^{-\alpha\zeta\omega_n t} + a_2 e^{-\zeta\omega_n t}\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) + a_3 e^{-\zeta\omega_n t}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right), \tag{6}$$

where a_1, a_2, and a_3 are as follows:

$$a_1 = \frac{(z_1-\alpha)(z_2-\alpha)}{z_1 z_2\left(1-2\alpha\zeta^2+\alpha^2\zeta^2\right)},$$

$$a_2 = \frac{\alpha\left[(z_1+z_2)-\alpha+z_1 z_2\zeta^2(\alpha-2)\right]}{z_1 z_2\left(1-2\alpha\zeta^2+\alpha^2\zeta^2\right)},$$

$$a_3 = \frac{\alpha\left[\alpha\zeta^2+z_1 z_2\zeta^2(1-2\zeta^2+\alpha\zeta^2)-1+\zeta^2(1-\alpha)(z_1+z_2)\right]}{z_1 z_2\zeta\left(1-2\alpha\zeta^2+\alpha^2\zeta^2\right)\sqrt{1-\zeta^2}}.$$

The small-signal settling time depends on the five system parameters and the targeted settling accuracy level. An analytical expression for the small-signal settling time cannot be readily achieved, but it can be formulated for a given settling accuracy level, ψ, and settling time of t_{ss} as [16]:

$$t_{ss} = \min\{t: \quad |\varepsilon_s(t)| \le \psi, \quad \forall\, t \ge t_{ss}\}. \tag{7}$$

The small-signal settling behavior of a three-stage NMC amplifier can be described by means of the third-order transfer function given in (4). Therefore, the circuit parameters including the transconductance of the amplifier stages and the value of the compensation capacitors are obtained by equating relations (1) and (4) resulting in:

$$g_{m1} = \frac{\alpha\omega_n C_L}{\beta\zeta|z_1 z_2|}, \tag{8}$$

$$g_{m2} = \frac{\omega_n C_L\left(\alpha\left(z_1+z_2-2z_1 z_2\zeta^2\right)-z_1 z_2\right)(z_1+z_2)}{z_1^2 z_2^2\zeta}, \tag{9}$$

$$g_{m3} = \frac{\omega_n C_L B}{z_1^2 z_2^2\zeta}, \tag{10}$$

$$C_{m1} = \frac{C_L\left(\alpha\left(z_1+z_2-2z_1 z_2\zeta^2\right)-z_1 z_2\right)}{z_1^2 z_2^2\zeta^2}, \tag{11}$$

$$C_{m2} = \frac{C_L(z_1+z_2)B}{|z_1^3 z_2^3|\,\zeta^2}, \tag{12}$$

where $B = z_1 z_2\left[\alpha\zeta^2(z_1 z_2-2z_1-2z_2)+(\alpha-z_1-z_2)\right]+2z_1^2 z_2^2\zeta^2+\alpha\left(z_1^2+z_2^2\right)$.

Considering $z_1 z_2 < 0$ and $z_1 + z_2 > 0$, in accordance with the possible zeros locations in a three-stage NMC amplifier, all obtained expressions for circuit parameters in (8)–(12) will be positive, and so acceptable. The relations (8)–(10) reveal that the transconductance of the amplifier stages is proportional to the load capacitance (C_L) and the natural frequency (ω_n). The natural frequency is a representation of the amplifier speed and the above relations clearly indicate that a high speed amplifier needs more power. In addition, the total integrated noise of the amplifier is inversely proportional to the load capacitance, and consequently, to reduce the output noise, more power is also needed. The relations (11)–(12) demonstrate that the size of compensation capacitors increases proportionally by the load capacitance.

3.2 Large-signal settling

When a large input step is applied to the amplifier utilized in a closed-loop configuration, the output voltage firstly changes with a constant rate due to the limited slew rate of the amplifier and then it changes exponentially due to the amplifier's limited unity-gain bandwidth. These regions of settling are called the nonlinear or large-signal settling and small-signal settling, respectively. The effect of slewing behavior on the settling time of an amplifier is considerable especially in high speed switched-capacitor circuits. The authors in previously reported works point out this issue, but for the sake of simplicity, only consider the linear settling region in their proposed design procedures.

When a large input step is applied into the amplifier shown in Fig. 2, it can readily be shown that during slewing, the differential slew rates at the output of the amplifier stages are given by:

$$SR_1 = \frac{I_{D5}}{C_{m1}}, \quad SR_2 = \frac{I_{D10}}{C_{m2}}, \quad SR_3 = \frac{2I_{D13}-I_{D5}-I_{D10}}{C_L}, \tag{13}$$

where I_{D5}, I_{D10}, and I_{D13} are the drain current of M_5, M_{10}, and M_{13}, respectively. The minimum value of SR_1, SR_2, and SR_3 limits the slew rate of the amplifier, i.e. we have $SR = \min(SR_1, SR_2, SR_3)$ [14]. The relations in (13) describe the slew rate of amplifier stages in terms of their bias currents. To reduce the number of design variables, three slew rates can be expressed as a function of five system parameters. To do this, I_{D5}, I_{D10}, and I_{D13} are firstly related to the transconductance of the amplifier stages as follows:

$$I_{D5} = g_{m1}V_{eff1}, \quad I_{D10} = g_{m2}V_{eff2}, \quad I_{D13} = \frac{g_{m3}V_{eff3}}{2}, \quad (14)$$

where V_{eff1}, V_{eff2}, and V_{eff3} are the effective overdrive voltage of M_1, M_6, and M_{11} transistors in Fig. 2, respectively. Thus, using the relations (8), (11), and (14), we have:

$$SR_1 = \frac{g_{m1}}{C_{m1}}V_{eff1} = \frac{\alpha\zeta|z_1z_2|}{\beta\left(\alpha\left(z_1+z_2-2z_1z_2\zeta^2\right)-z_1z_2\right)} \times \omega_n V_{eff1} \quad (15)$$

Similar to (15), other expressions for SR_2 and SR_3 can be also obtained. The relation in (15) indicates that the slew rate is directly proportional to ω_n which means a fast-settling three-stage NMC amplifier must have a large slew rate. The amplifier limited slew rate determines the large-signal settling time and it can be approximated as:

$$t_{ls} = \frac{V_{FS}}{SR}, \quad (16)$$

where V_{FS} is the differential output signal change during slewing and t_{ls} is the large-signal settling time. After this time period, the amplifier enters into the linear region and the small-signal settling time corresponding to this region is given by (7). The total settling time of the amplifier is the sum of large and small signal settling times.

3.3 Noise analysis

In MOS transistors, the most significant noise source is the channel thermal noise. For MOS devices operating in the saturation region, the channel thermal noise can be modeled by a current source between the drain and source terminals [23]. The small-signal noise model of a three-stage NMC amplifier utilized in a closed-loop configuration is depicted in Fig. 3 where the noise of each amplifier stage is also modeled by a current source. The noise power spectral density (PSD) of the first stage amplifier is given by:

$$\overline{I_{n1}^2} = 4kT\gamma(g_{m1}+g_{m3,4}), \quad (17)$$

where k, T, and γ represent the Boltzmann's constant, absolute temperature, and excess noise coefficient of MOS transistors, respectively, and $g_{m3,4}$ is the transconductance of M_3 and M_4 transistors shown in Fig. 2. The noise of the first stage amplifier is appeared at the output by the following noise transfer function (NTF):

$$H_{n1}(s) = \frac{V_{n,out}}{I_{n1}} = \frac{1}{g_{m1}}A_v(s), \quad (18)$$

where $A_v(s)$ is the transfer function of the NMC amplifier which is expressed by (1). The noise contribution of first stage amplifier at the output is then found by integrating the product of the noise PSD with the squared NTF magnitude as follows:

$$S_{N,out,1} = 2\left[\overline{I_{n1}^2}\int_0^\infty |H_{n1}(f)|^2 df\right]. \quad (19)$$

The output noise power is multiplied by 2 due to the fully-differential circuit of the amplifier. Fortunately, there is an analytical expression for the above-mentioned integral [25]. Therefore, by using (19) and (8)–(12), the noise contribution of the first stage amplifier at the output is obtained in terms of the system parameters as:

$$S_{N,out,1} = \left[\frac{kT\gamma}{\beta C_L}\left(1+\frac{g_{m3,4}}{g_{m1}}\right)\right] \times \frac{\alpha+\alpha\zeta^2(z_1^2+z_2^2+2\alpha)+\zeta^4z_1^2z_2^2(\alpha+2)}{\zeta^2\left[1+2\alpha\zeta^2+\alpha^2\zeta^2\right]|z_1z_2|}. \quad (20)$$

The noise contribution of the second stage amplifier at the output can be also calculated similarly. The noise PSD of the second stage amplifier is given by:

$$\overline{I_{n2}^2} = 4kT\gamma(g_{m2}+g_{m8}), \quad (21)$$

where g_{m8} is the transconductance of M_8 and M_9 transistors in Fig. 2. The NTF of the second stage amplifier is expressed by:

$$H_{n2}(s) = \frac{V_{n,out}}{I_{n2}} = \frac{1}{\beta A_{v1}g_{m2}}\frac{\left(1-\frac{C_{m2}}{g_{m3}}s\right)(1+R_1C_{m1}s)}{D(s)}, \quad (22)$$

where $D(s) = 1 + s\left(\frac{C_{m1}}{\beta g_{m1}} - \frac{C_{m2}}{g_{m3}}\right) + s^2\left(\frac{g_{m3}-g_{m2}-\beta g_{m1}}{\beta g_{m1}}\frac{C_{m1}C_{m2}}{g_{m2}\,g_{m3}}\right) + s^3\frac{C_{m1}C_{m2}C_L}{\beta g_{m1}g_{m2}\,g_{m3}}$.

In (22), $D(s)$ is the characteristic equation of the system, and so, it is the same as the denominator of the transfer function of the three-stage NMC amplifier. The NTF of the second stage amplifier has a high frequency RHP zero and a low frequency LHP zero given by (23) and (24), respectively.

$$\omega_{z,RHP} = +\frac{g_{m3}}{C_{m2}}, \quad (23)$$

$$\omega_{z,LHP} = -\frac{1}{R_1C_{m1}} = -\frac{g_{m1}}{A_{v1}C_{m1}}, \quad (24)$$

where $A_{v1} = g_{m1}R_1$ is the dc gain of the first stage amplifier. Assuming that $g_{m3} \gg g_{m1}$, g_{m2}, the RHP zero is located at much higher frequencies, and hence, it can be neglected. By considering $A_{v1} \gg 1$, the low frequency LHP zero can be replaced by a zero in the origin, and consequently, $H_{n2}(s)$ can be approximated by:

$$H_{n2}(s) \approx \frac{C_{m1}}{\beta g_{m1}g_{m2}}\frac{s}{D(s)}. \quad (25)$$

Similar to the first stage amplifier, the noise contribution of the second stage amplifier at the output is obtained as:

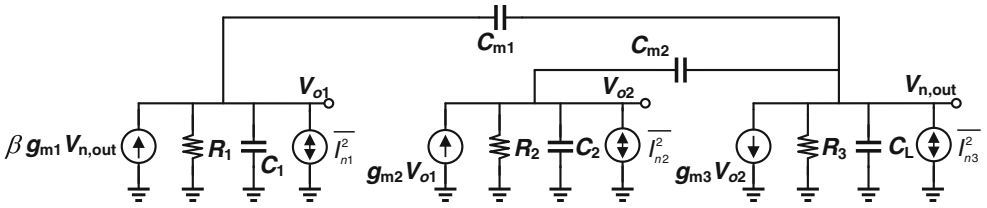

Fig. 3 Small-signal noise model of a three-stage NMC amplifier in the closed-loop configuration

$$S_{N,out,2} = \left[\frac{kT\gamma}{C_L}\left(1+\frac{g_{m8}}{g_{m2}}\right)\right] \times \frac{\alpha(z_1+z_2-2z_1z_2\zeta^2)-z_1z_2}{(1+2\alpha\zeta^2+\alpha^2\zeta^2)(z_1+z_2)}. \tag{26}$$

In (26), the value obtained for the noise contribution of the second stage amplifier must be positive. As mentioned already, we have $z_1 + z_2 > 0$ and $z_1 z_2 < 0$. So, considering these two conditions, the value of $S_{N,out,2}$ will be positive as expected.

It is worth mentioning that although the second stage NTF is divided by the dc gain of the first stage amplifier, the noise contribution of the second stage amplifier is still considerable. This is because the low frequency LHP zero raises the magnitude of this NTF and causes a peaking at high frequencies.

Finally, the noise contribution of the third stage amplifier is obtained. Its PSD is given by:

$$\overline{I_{n3}^2} = 4kT\gamma(g_{m3}+g_{m13}), \tag{27}$$

where g_{m13} is the transconductance of M_{13} and M_{14} transistors. The third stage amplifier's NTF is approximated given by:

$$H_{n3}(s) = \frac{V_{n,out}}{I_{n3}} = \frac{1}{\beta A_{v1}A_{v2}g_{m3}} \frac{(1+R_1C_{m1}s)(1+R_2C_{m2}s)}{D(s)} \approx \frac{C_{m1}\ C_{m2}}{\beta g_{m1}g_{m2}g_{m3}} \frac{s^2}{D(s)}, \tag{28}$$

where two low frequency LHP zeros of the NTF which are located at $1/R_1C_{m1}$ and $1/R_2C_{m2}$ are replaced by two zeros at the origin. This approximation is necessary to derive a simplified but yet accurate relation for the noise contribution of third stage amplifier as:

$$S_{N,out,3} = \left[\frac{kT\gamma}{C_L}\left(1+\frac{g_{m13}}{g_{m3}}\right)\right] \times \frac{B\ (1+2\alpha\zeta^2)}{\zeta^2 z_1^2 z_2^2 (1+2\alpha\zeta^2+\alpha^2\zeta^2)}, \tag{29}$$

where B has been previously defined in (12). In NTF of the third stage amplifier, the same peaking effect as the NTF of the second stage amplifier takes place, and hence, the noise contribution of the third stage amplifier is mainly due to the low frequency zeros. In the absence of these zeros and considering a high dc gain in the first and second stage amplifiers, it is expected that the noise contribution of third stage amplifier at the output will be negligible. The total integrated noise power of a three-stage NMC amplifier is simply the sum of its three stage noises:

$$S_{N,out} = S_{N,out,1} + S_{N,out,2} + S_{N,out,3}. \tag{30}$$

3.4 Power consumption

The power consumption of a three-stage NMC amplifier can be formulated in terms of five system parameters as:

$$\begin{aligned} P_{diss}\ (\alpha,\zeta,z_1,z_2,\omega_n) &= V_{DD}(I_{D5}+I_{D10}+2I_{D13}) \\ &= V_{DD}(g_{m1}V_{eff1}+g_{m2}V_{eff2} \\ &\quad + g_{m3}V_{eff3}), \end{aligned} \tag{31}$$

where the additional bias circuit power dissipation is neglected.

3.5 Proposed design procedure

The achieved relations to describe the performance of a three-stage NMC amplifier are very complicated to analytically obtain the system parameters, i.e. α, ζ, z_1, z_2, and ω_n optimally for a specific settling error in a definite time period and specific noise budget. Therefore, most of the previously reported works utilize the numerical simulations that are only able to minimize the small-signal settling time for a given power consumption and do not consider the other important specifications of three-stage amplifiers such as the large-signal settling time and total integrated noise in their design schemes. Therefore, to present a comprehensive design procedure that takes into account these important specifications, an automated design optimization scheme should be utilized.

In this approach, the amplifier design is formulated as a constrained optimization problem and a general purpose optimization program is applied to optimize the performance of the amplifier. As a first step, design equations are needed to evaluate the amplifier performance in the optimization routine and should be derived in advance. The second step is the identification of the independent variables that are varied by the optimization program in search of the optimum design solution. The relationships between dependent and independent design variables also need to be

minimize:

$P_{diss}(\alpha, \zeta, z_1, z_2, \omega_n)$ } Objective function

subject to:

$$\left.\begin{array}{l} \mathrm{I}: S_{N,out} < S_{N,out,desired} \\ \mathrm{II}: t_s < t_{s,desired} \ (\text{with } \psi \ accuracy), t_s = t_{ss} + t_{ls} \\ \mathrm{III}: z_2 < 0,\ z_1 + z_2 > 0 \end{array}\right\} \text{Constraints}$$

Fig. 4 Optimization problem

known. The performance of the amplifier can be specified as an objective or as a constraint. Performance objectives are minimized (or maximized) by the program, and therefore, are included in the objective function. The performance metrics that have to be satisfied are modeled as a constraint. The amplifier's performance is evaluated at each iteration for each set of independent design variables suggested by the optimization program. The resulting performance information is used by the optimization program to check the specification and to suggest new values for the independent design variables so as to optimize the objective function. Global or local optimization algorithms can be exploited to solve the optimization problem. In local optimization algorithms, it is necessary to provide a good initial starting point for the optimization routine while global optimization algorithms are able to find a global minimum (or maximum) of the objective function.

In the proposed design procedure, the design goal is minimizing the power consumption while meeting the settling time and noise requirements. So, here, the objective function is the power consumption while the total integrated output noise and settling time (considering both small and large signal settling regions) are included as a constrained performance. The five system parameters are considered as independent design variables. To have large output signal swing and sufficient linearity simultaneously, the overdrive voltage (V_{eff}) of all devices is set to a fixed value as a priori. To find optimal system parameters, the optimization problem shown in Fig. 4, is developed. In this optimization problem, the objective function is the amplifier power consumption that must be minimized and noise and settling time requirements are included in the form of first and second optimization constraints. The third constraint is related to the search space of the optimization problem since one of the system zeros is a RHP zero and the magnitude of the LHP zero is greater than that of the RHP zero. Then, the optimization problem is solved based on GA method and using MATLAB global optimization toolbox. The GA is a popular optimization method and was employed in several amplifier designs such as one reported in [26]. This method is suitable to solve both constrained and unconstrained optimization problems and it is based on the natural selection, the process that derives a biological evolution. The GA repeatedly modifies a population of individual solutions. At each step, the GA selects individuals randomly from the current population to be parents and uses them to produce the children for the next generation. Over successive generations, the population evolves toward an optimal solution.

The goal of the optimization is to find the global minimum of the objective function, a point where the function value is smaller than at any other point in the search space. However, optimization algorithms sometimes return a local minimum, a point where the function value is smaller than at nearby points but possibly greater than at a distant point in the search space. The GA can overcome this deficiency with the right settings such as the properly choosing of the population size, number of generations, etc. In the GA optimization, the population size is a useful option which can be used to guarantee the global optimization. The population size specifies how many individuals there are in each generation. With a large population size, the genetic algorithm searches the solution space more thoroughly, and hence, increasing the chance that the algorithm will return a global minimum of the optimization problem. However, a large population size also makes the algorithm to run slowly. So, there is a need to experiment with different population sizes to ensure that the global minimum is obtained. Figure 5 shows an implementation script of the GA optimization using the *ga* function provided in MATLAB global optimization toolbox.

Finally, it should be mentioned that it may be possible there is no feasible solution for the optimization problem in Fig. 4. The settling time constraint on the optimization problem can be always satisfied since the settling time is proportional to $1/\omega_n$, and therefore, large values of ω_n lead to small settling times. But, there is a minimum achievable total output noise power for a given capacitance load, and hence, the noise constraint in the optimization problem will not be met for any considered noise budget. Thus, if the GA did not reach to a feasible solution, it would be necessary to relax the noise specification or to increase the load capacitance of the amplifier if it is possible.

After obtaining optimal system parameters, the required transconductance value of amplifier stages and the size of compensation capacitors are calculated from relations (8)–(12). Once the transconductance and the overdrive voltage of transistors are determined, their aspect ratios and bias currents can be obtained. It is worth mentioning that the dc gain of amplifier stages are not used in the system level design since they also depend on the output resistance of MOS transistors that is not easily modeled and can only be predicted by simulations using the accurate transistor models. Nevertheless, the dc gain of amplifier stages highly depends on the channel length of transistors, and therefore,

Fig. 5 An implementation script of the GA optimization using MATLAB

```
%x=[x(1),x(2),x(3),x(4),x(5)]=[alfa,zeta,z1,z2,wn];
function      P=Power_Dissipation(x)
VDD=1.2,Veff1=0.15,Veff2=0.15,Veff3=0.15,Cl=2; beta=1; % Cl=2pF
gm1=-x(1).*x(5).*Cl./(beta.*x(2).*x(3).*x(4));
gm2=x(5).*Cl.*(x(1).*(x(3)+x(4))-2.*x(1).*x(3).*x(4).*x(2).^2-
x(3).*x(4)).*(x(3)+x(4))./(x(3).^2.*x(4).^2.*x(2));
B=x(3).*x(4).*(x(1).*x(2).^2.*(x(3).*x(4)-2.*x(3)-2.*x(4))+(x(1)-x(3)-
x(4)))+2.*x(3).^2.*x(4).^2.*x(2).^2+x(1).*(x(3).^2+x(4).^2);
gm3=x(5).*Cl.*B./(x(3).^2.*x(4).^2.*x(2));
P=(gm1*Veff1+gm2*Veff2+gm3*Veff3)*VDD;% The Power consumption is given in mW
end

function   [c,ceq]=Constraint(x)
VFS=1,Cl=2,beta=1;Veff=0.15;%Veff=Veff1=Veff2=Veff3 , Cl=2pF
ceq=[];
ts=10;st=0.0002; % ts=10ns
t=linspace(0,40,1000);
s=Step_Response(x(1),x(2),x(3),x(4),x(5),t);
d=stepinfo(s,t,'RiseTimeLimits',[0.05,0.95],'SettlingTimeThreshold',st);
gm1=-x(1).*x(5).*Cl./(beta.*x(2).*x(3).*x(4));
Cm1=Cl.*(x(1).*(x(3)+x(4))-2.*x(1).*x(3).*x(4).*x(2).^2-
x(3).*x(4)).*(x(3).^2.*x(4).^2.*x(2).^2);
gm2=x(5).*Cl.*(x(1).*(x(3)+x(4))-2.*x(1).*x(3).*x(4).*x(2).^2-
x(3).*x(4)).*(x(3)+x(4)).*(x(3).^2.*x(4).^2.*x(2));
B=x(3).*x(4).*(x(1).*x(2).^2.*(x(3).*x(4)-2.*x(3)-2.*x(4))+(x(1)-x(3)-
x(4)))+2.*x(3).^2.*x(4).^2.*x(2).^2+x(1).*(x(3).^2+x(4).^2);
gm3=x(5).*Cl.*B./(x(3).^2.*x(4).^2.*x(2));
Cm2=-Cl.*(x(3)+x(4)).*B./(x(3).^3.*x(4).^3.*x(2).^2);

SR1=gm1/Cm1*Veff;SR2=gm2/Cm2*Veff;SR3=(gm3-gm2-gm1)/Cl*Veff;SR=[SR1,SR2,SR3];
SR=min(SR);tls=VFS/SR;tss=d.SettlingTime;
c1=tls+tss-ts;
c2=Total_Output_Noise(x)-40;
c3=-x(3)-x(4);
c=[c1,c2,c3];
end
rng(1,'twister') % for reproducibility
options = gaoptimset('PopulationSize', 400,'Generations',100);
[x,fval]=ga(@Power_Dissipation,5,[],[],[],[],[0.1 0.1 0.1 -4 0.1],[4 0.95 4 -
0.1 6],@Constraint,options);
```

by selecting non-minimum channel lengths (2–4 times of L_{min}) especially for active load transistors, a high dc gain can be achieved. However, if the dc gain requirement of the amplifier will not be met by increasing the channel length of transistors, a folded-cascode amplifier instead of a simple differential pair can be used in the first stage amplifier and also possibly in the second stage amplifier to provide a very high dc gain. In other words, the required dc gain is mainly considered in the topology selection of the circuit implementation.

The proposed design procedure is summarized in Fig. 6 and its further details are explained in the design example presented in the next section.

4 Design example and simulation results

To evaluate the usefulness of the proposed design procedure, the three-stage NMC amplifier shown in Fig. 2 was designed and simulated using a standard 90 nm CMOS technology with HSPICE. The design is targeted to achieve 0.02 % settling accuracy within 10 ns while driving a 2 pF effective load capacitance from a single 1.2 V power supply in a fully-differential flip-around S/H configuration shown in Fig. 7. C_L is composed of the next stage (Multiply DAC) capacitance, the CMFB capacitance, the parasitic capacitances of output transistors, and the feedback capacitors. This S/H circuit is designed to be used in an 11-bit pipelined ADC with 2 V_{pp} differential input and 1 pF sampling capacitor to achieve an SNR due to the kT/C noise of the switches more than 11-bit accuracy. Besides, the amplifier total output thermal noise power is limited to 40 nV^2. The output noise of S/H circuit including the kT/C noise of the switches and output thermal noise of the amplifier must be chosen to satisfy 11-bit accuracy requirement of the targeted pipeline ADC.

To achieve large output signal swing and sufficient linearity, all devices are biased in strong inversion with an effective overdrive voltage (V_{eff}) about 150 mV. The system parameters using the proposed design procedure in Sect. 3 are obtained as $\alpha = 1.03$, $\zeta = 0.80$, $z_1 = 2.67$, $z_2 = -2.03$, and $\omega_n = 2.78$ Grad/s. Then, the relations (8)–(12) are used to find the optimal values of the amplifier stages transconductance and compensation capacitors as

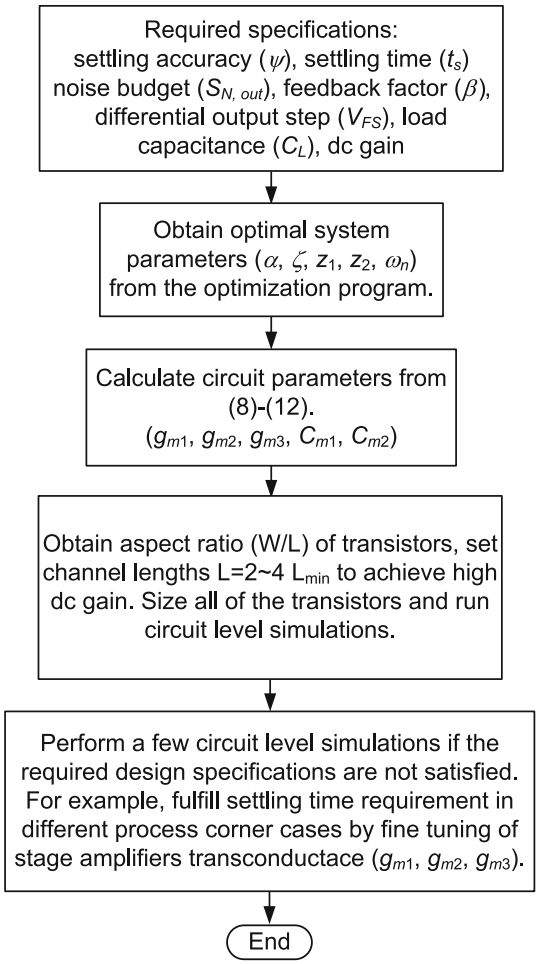

Fig. 6 Design flow summary

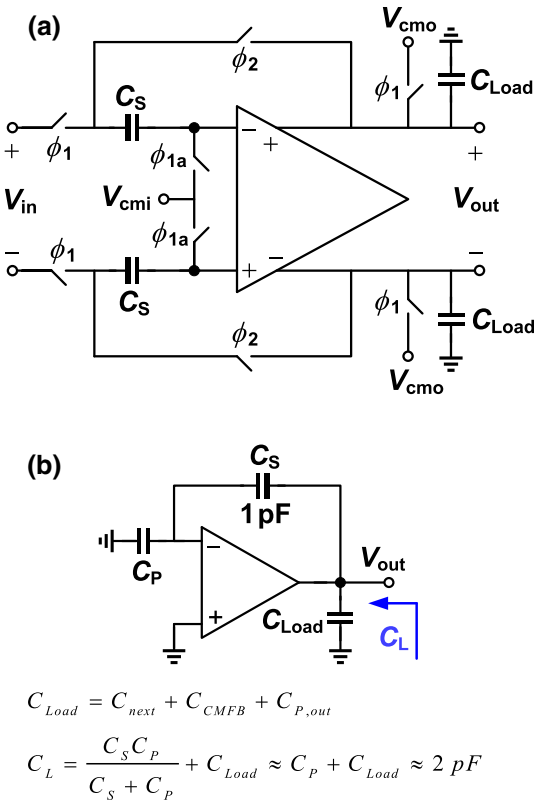

Fig. 7 **a** Fully-differential flip-around S/H and **b** the amplifier closed-loop configuration in the hold phase

Table 1 Simulated device sizes

Parameter	W/L	g_m (mA/V)	I_{DS} (mA)	V_{eff} (mV)
M_1, M_2	5 × 1/0.2 μm	**1.78** (g_{m1})	0.18	135
M_3, M_4	5 × 6/0.3 μm	2.03	0.18	137
M_5	10 × 1/0.2 μm	3.36	0.35	145
M_6, M_7	5 × 6/0.2 μm	**2.93** (g_{m2})	0.25	125
M_8, M_9	5 × 1.8/0.3 μm	2.41	0.25	152
M_{10}	10 × 6/0.2 μm	5.44	0.49	137
M_{11}, M_{12}	14 × 3.5/0.2 μm	**17.78** (g_{m3})	1.61	124
M_{13}, M_{14}	14 × 16/0.3 μm	17.06	1.61	155
C_{m1}, C_{m2}	1.4, 0.9 pF			
C_L	2 pF			

$g_{m1} = 1.3$ mA/V, $g_{m2} = 2.0$ mA/V, $g_{m3} = 16.8$ mA/V, $C_{m1} = 1.4$ pF, and $C_{m2} = 0.9$ pF. Hence, having known g_m and V_{eff} of all critical devices, their bias currents and aspect ratios are obtained. The non-minimum channel length is utilized in transistors to achieve high dc gain. The resulted device parameters are summarized in Table 1. The transconductance of amplifier stages was increased to achieve the targeted settling performance in different process corner cases through a few iterations in the circuit level simulations. This was necessary since the closed-loop transfer function given in relation (1) was obtained by assuming several simplifying assumptions. Therefore, in the proposed design scheme, a few circuit level simulations are needed to refine the settling performance by fine tuning of the amplifier stages transconductance.

Figure 8 shows the simulated amplifier settling response in different process corner cases and temperature variations when a ±1 V step is applied into the amplifier's input. The simulation results are summarized in Table 2. The proposed design procedure is completely done in the time-domain. As it is known, the step response of a dynamic system provides some information on the system stability. Hence, it is expected that the designed three-stage NMC amplifier should have a sufficient phase margin. The open-loop frequency response of the simulated amplifier is shown in Fig. 9. The achieved unity-gain frequency and phase margin are about 202.8 MHz and 63.2°, respectively.

To evaluate the optimal small-signal settling performance of the designed three-stage amplifier, the normalized settling time, $N = 2\pi \times f_{GBW} \times t_{ss}$, is utilized. In a first-order system, the minimum small-signal settling time

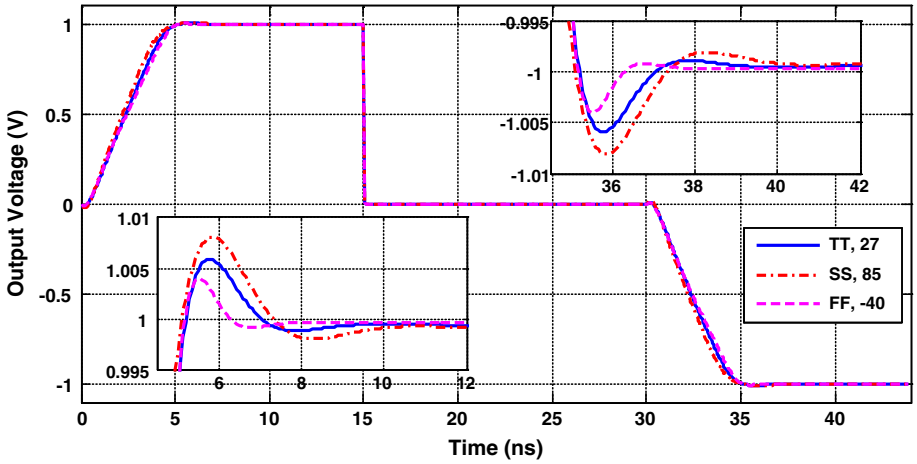

Fig. 8 Settling response to ±1 V differential input step

Table 2 Simulation results summary

Parameter	TT@ 27 °C	SS@ 85 °C	FF@ −40 °C
DC gain (dB)	72.1	69.5	74.6
f_{GBW} (MHz)	202.8	179.1	247.4
Phase margin	63.2°	64.2°	62.0°
0.02 % settling time, t_{s+}/t_{s-} (ns) @ ±1 V input step	8.7, 8.7	9.6, 9.6	7.3, 7.3
0.02 % small-signal settling time, t_{ss+}/t_{ss-} (ns) @ 100 mV input step	4.7, 4.7	4.8, 4.8	4.0, 4.0
$N = 2\pi \times f_{GBW} \times t_{ss}$	5.99	5.40	6.22
Power dissipation (mW)	5.2	5.4	4.8
V_{DD}	1.2 V		
Technology	90 nm CMOS		

with an accuracy level of ψ is given by $t_{ss} = -\ln(\psi) \times \tau$, where $\tau = 1/(\beta\ \omega_{\mathrm{GBW}})$ is the time-constant of the closed-loop single-pole amplifier and β is the feedback factor. In other words, $N = t_{ss}/\tau = -\ln(\psi)$ is defined as the number of required time constants for the amplifier to settle within a specific settling error. Similarly, in high-order systems, the parameter N can be defined as the normalized settling time. In a third-order system, the dependency of N on settling accuracy and other system parameters is complicated and deriving an analytical expression for N, similar to a first-order system, is almost impossible. However, the small value of N results in the reduction of the required value of GBW for a given settling time and accuracy making the designed amplifier more power efficient. Conclusion is that the value of N gives a good criterion to compare the different designed amplifiers and as well as to make sure from the small-signal settling optimization of a designed amplifier.

The value of N for the designed three-stage NMC amplifier is reported in Table 2. To calculate the value of N, only the small-signal settling time is considered to make a fair comparison between the simulated and theoretically obtained values of N. So, a 100 mV step is applied into the amplifier's input to guarantee the linear settling behavior in different process corner cases. In [22], the optimum value of $N = 6.5$ is theoretically calculated for a third-order system with 0.02 % settling accuracy. Comparing this value of N with the reported one in Table 2, obviously confirms the optimal small-signal settling performance of the designed amplifier even considering different process corner cases and temperature variations. It is worth mentioning that the simulated value of N is a little better than the theoretically value since in [22] the effect of zeros is neglected.

In order to further show the usefulness of the proposed design procedure, a comparison with the design scheme reported in [16] is performed. The presented design in [16] finds the optimal value of compensation capacitors for a given amplifier stages transconductance such that the settling time is minimized. We obtained the value of C_{m1} and C_{m2} using the same procedure presented in [16] with the assumption that the amplifier stages transconductance be the same as the achieved values here. The value of compensation capacitors are found as $C_{m1} = 1.4$ pF and $C_{m2} = 0.9$ pF which are exactly the same as the obtained values here. The result of this comparison clearly

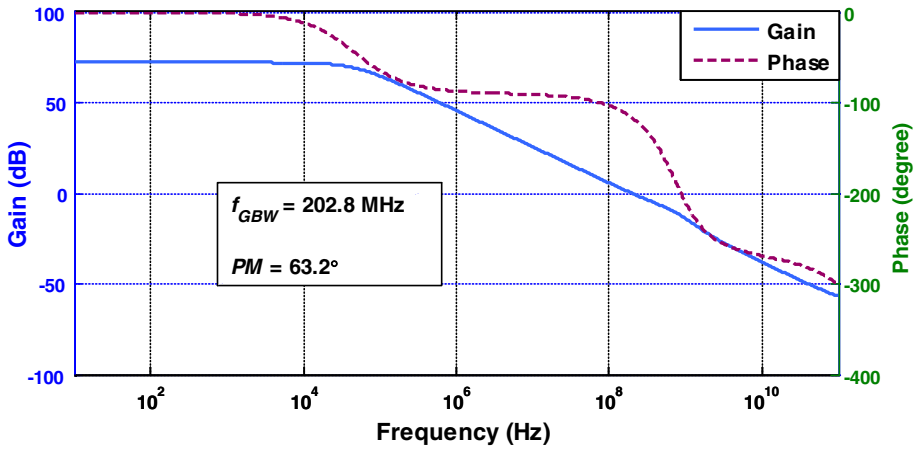

Fig. 9 Open-loop frequency response of the simulated three-stage NMC amplifier

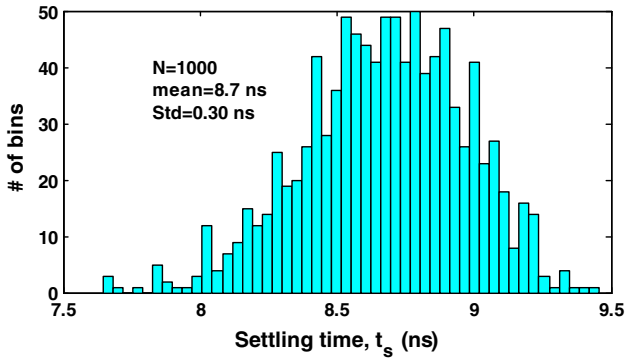

Fig. 10 Monte Carlo simulation results of the settling time

Table 3 Settling time and phase margin versus the variation of compensation and load capacitors

Parameter	−10 %	Nominal	+10 %
C_{m1} (pF)	1.26	1.4	1.54
C_{m2} (pF)	0.81	0.9	0.99
C_L (pF)	1.8	2	2.2
Phase margin	62.9°	63.2°	63.4°
t_s (ns)	8.4	8.7	9.5

demonstrates that the proposed design scheme achieves the best settling performance and finds the optimal circuit parameters for a three-stage NMC amplifier. It should be noted that the proposed design method in this paper is superior to that in [16] since it provides the transconductance of amplifier stages and the value of compensation capacitors optimally while the design procedure in [16] only finds the value of compensation capacitors for a given value of amplifier stages transconductance.

The robustness of the proposed design procedure against process and mismatch variations were evaluated through extensive circuit level Monte Carlo simulations. The results

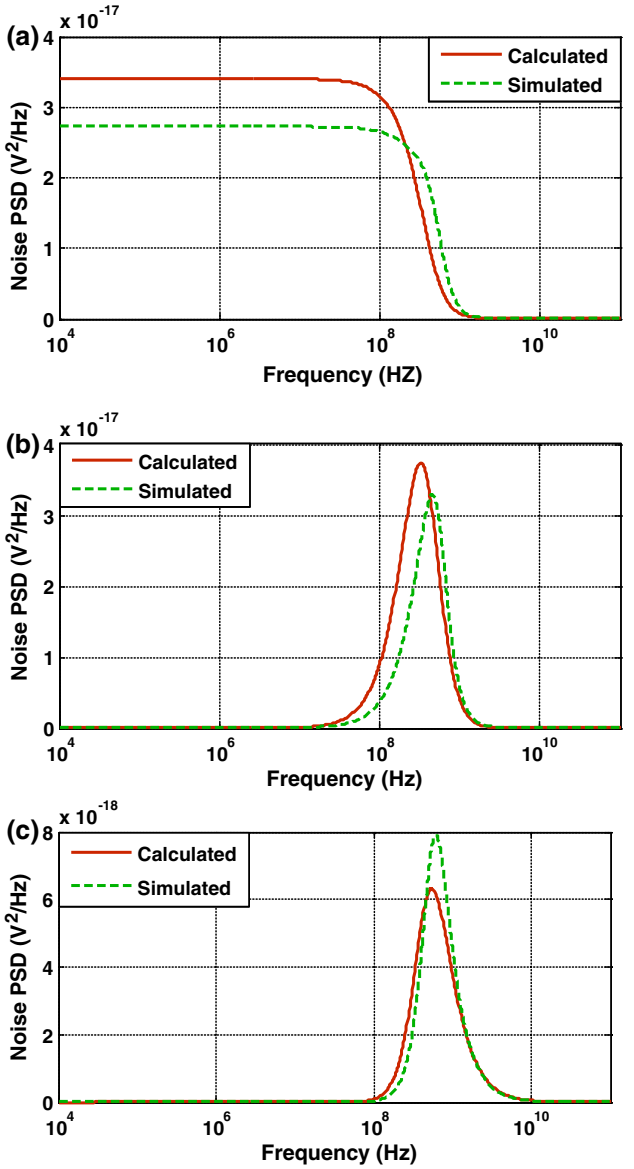

Fig. 11 PSD at the total amplifier output due to the **a** first stage, **b** second stage, and **c** third stage noises

are shown in Fig. 10 where the settling time of the designed amplifier for 0.02 % dynamic settling error is illustrated for 1,000 iterations. As it is seen, the designed amplifier is more tolerant to the process and device variations and shows negligible performance degradation.

Sensitivity of the settling time with respect to compensation capacitors is also investigated. As an example, a typical capacitance tolerance of ±10 % is considered. Simulation results summarized in Table 3 indicate that the settling time requirement is also satisfied in the case of these variations.

To support noise analysis carried out in Sect. 3 with simulation results, Fig. 11 and Table 4 are presented. In Fig. 11, the simulated and calculated noise PSD's at the output are a little different since we increased the transconductance of amplifier stages in the circuit level simulations, but the simulated and calculated total output noise power given in Table 4 match better because according to the relations (20), (26), and (29), the total output noise power of an NMC amplifier depends on the load capacitance and relative pole-zero locations not the absolute value of amplifier stages transconductance. In Table 4, the relative noise contribution of each stage amplifier at the total output noise power is also shown. As it is seen, the noise contribution of the third stage amplifier is less than the other stages since the noise PSD of each stage amplifier at the output is inversely proportional to its stage transconductance (g_{mi}) and g_{m3} is greater than both g_{m1} and g_{m2}.

The noise analysis in this paper gives further insight into the design of three-stage NMC amplifiers. As reported in Table 4, the second stage amplifier has the largest contribution at the total output noise power. So, in order to reduce the total amplifier output noise, g_{m2} cannot be selected smaller than g_{m1}. This important matter has not been considered already. For example, in design procedure presented in [16] where the value of the amplifier stages transconductance are chosen based on design heuristics, a small value is considered for g_{m2} since a lower value for g_{m2} results in a lower size in C_{m2}. Although this design choice leads to the reduced silicon die area, but it increases the total output noise power of a three-stage NMC amplifier.

In order to compare the proposed design procedure with respect to previously reported design approaches, Table 5 is presented. The different design procedures are compared using the following figure-of-merit (FoM) defined in [27]:

$$FoM = \frac{GBW \times C_L}{g_{m,\text{total}}}, \tag{32}$$

where $g_{m,total}$ is the total transconductance used in amplifier stages. It is worth mentioning that this FoM is independent of the amplifier topology, utilized process, and other design choices, thus providing an accurate and fair comparison among different design procedures. On the other hand, it considers only the small-signal performance using the GBW as a representative for the speed of the amplifier. Therefore, considering the noise performance and also the

Table 4 Noise contribution of each amplifier stage in the total output noise

Parameter	Calculated	Simulated
First stage amplifier noise	12.5 nV^2 (31.25 %)	15.4 nV^2 (35.3 %)
Second stage amplifier noise	19.3 nV^2 (48.25 %)	19.4 nV^2 (44.5 %)
Third stage amplifier noise	8.2 nV^2 (20.5 %)	8.8 nV^2 (20.2 %)
Total output noise power	40 nV^2	43.6 nV^2

Table 5 Comparison of the different design procedures

Topology	NMC [16]	NMCNR [18]	NMC [19]	NMCNR [21]	NMC [Proposed]
Supply (V)	±1	3	1.8	1	1.2
Power consumption (mW)	0.05	5.4	0.54	5.2	5.2
DC gain (dB)	115	–	85.7	–	72.1
GBW (MHz)	0.247	55	21.3	449	202.8
Phase margin	62.8°	66°	62.0°	–	63.2°
C_L (pF)	10	3	2	1.86	2
Total transconductance, $g_{m,\ total}$ (mA/V)	0.11	12.42	2.64	37.83	22.49
C_{m1}, C_{m2} (pF)	7.98, 2.16	2.3, 3.5	1.8, 0.4	1.89, 1.26	1.4, 0.9
Implementation	Single-ended	Fully-differential	Single-ended	Fully-differential	Fully-differential
Small-signal settling time t_{ss+}/t_{ss-} (ns)	1220, 1660	13.7	13.1, 20.9	2.53	4.7
$N = 2\pi \times f_{GBW} \times t_{ss+}$ (t_{ss-})	1.89, 2.58	4.7	1.74/2.6	7.14	5.99
Settling accuracy	1 %	0.1 %	0.1 %	0.1 %	0.02 %
FoM = $GBW.C_L/g_{m,\ total}$ (MHz pF V/mA)	21.80	13.29	16.14	22.07	18.03
Technology	0.35 µm	0.35 µm	0.35 µm	90 nm	90 nm

normalized settling time, the overall performance of the amplifier using the proposed design procedure outperforms the previously reported works.

The presented design procedure is applicable to third order systems described by relation (4), and hence, it can be extended to other three-stage amplifiers as well. It can help circuit designers to design three-stage amplifiers optimally as well as it can be used in the computer aided circuit design tools.

5 Conclusions

In this paper, a novel systematic time-domain design procedure is presented for fast-settling three-stage amplifiers. The value of amplifier stages transconductance and compensation capacitors are optimized for a given circuit noise budget and settling accuracy within a specific time by considering both small-signal and large-signal settling regions to achieve a low-power and robust design. The proposed design approach can be used in the design of three-stage amplifiers to realize fast-settling switched-capacitor circuits.

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Sajad Golabi received the B.Sc. degree in electrical engineering from the K. N. Toosi University of Technology, Tehran, Iran, in 2011. He is currently a Research Assistant with the Integrated Circuits Design Laboratory, Amirkabir University of Technology, since 2011, where he is pursuing the M.Sc. degree in electrical engineering. His current research interests include analog and mixed-signal integrated circuits and systems, data converters, and CMOS RFIC design.

Mohammad Yavari received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, 2001, and 2006, respectively. He has been an Assistant Professor with the Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran, since 2006, where he founded the Integrated Circuits Design Laboratory, in 2007. He spent several research periods with the Institute of Microelectronics of Seville (IMSE-CNM), Seville, Spain. He was with Niktek, from May 2004 to April 2005 and October 2006 to May 2007, as a Principal Design Engineer, where he was involved in the design of high-resolution A/D and D/A converters for professional digital audio applications. He is the author or co-author of more than 100 peer-reviewed papers in international and national journals and conference proceedings on analog integrated circuits. His current research interests include analog and mixed-signal integrated circuits and signal processing, data converters, and CMOS RFIC design for wireless communications. Dr. Yavari was a recipient of the Best Student Research Award of the University of Tehran in 2004. He has been an Associate Editor of the *International Journal of Circuit Theory and Applications* since 2014.