# Transactions Briefs

## A Single Channel Split ADC Structure for Digital Background Calibration in Pipelined ADCs

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***Abstract*— A digital background calibration technique based on the concept of split analog-to-digital converter (ADC) structure is proposed for pipelined ADCs to correct the gain error induced by the capacitors mismatch and finite dc gain of the residue amplifiers and nonlinearity of the residue amplifiers. In the proposed technique, one of the channels in split ADC structure is virtually implemented by using two extra comparators in each ADC's stage and an interpolation filter to eliminate the mismatch between channels. Several circuit-level simulation results in the context of a 12-bit 100-MS/s pipelined ADC are provided to verify the usefulness of the proposed calibration technique. The simulation results show 51-dB signal-to-noise and distortion ratio and 65-dB spurious free dynamic range improvement, respectively, in comparison with the noncalibrated ADC.**

***Index Terms*— CMOS integrated circuits, digital background calibration, interpolation filter, least mean square (LMS) algorithm, pipelined analog-to-digital converters (ADCs).**

### I. Introduction

The scaling of CMOS technology deteriorates the performance of analog circuits, and hence, digital calibration techniques are utilized in high performance analog-to-digital converters (ADCs) to mitigate the imperfections of analog circuits [1].

Several digital calibration methods have been presented in the literature. In [2], the correlation of the ADC's digital output with a pseudorandom sequence, which acts like an offset in the ADC, is calculated to correct the gain error and nonlinearity of the amplifier. In [3], the histogram of the ADC around the decision points of the sub-ADC is investigated to address the gain error. The main problem of the pseudorandom and histogram-based methods is that they require a long time to converge or lots of digital processing. To avoid these problems, equalization-based techniques have been presented in the literature. A slow but accurate ADC is used in [4] to calibrate the pipelined ADC and a reference digital-to-analog converter (DAC) along with the least mean square (LMS) algorithm is utilized in [5]. Equalization-based techniques benefit from the fast convergence time unlike the pseudorandom-based schemes. However, they need an accurate reference resulting in the analog design complexity and more power consumption. In [6], a semiequalization-based technique is used to reduce the convergence time of split ADC structures. Regarding this method, an unknown gain is added in the path of input signal to make a replica path for the pipelined ADC. This replica path and an interpolation filter are used to extract the gain error and nonlinearity of the amplifier. However, this increases the analog design complexity and also the calibration coefficients.

In this brief, a calibration technique based on the split ADC structure is proposed by using a single ADC and some extra comparators with an interpolation filter as the virtual ADC.

Manuscript received October 7, 2016; accepted December 14, 2016. Date of publication January 9, 2017; date of current version March 20, 2017.

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Digital Object Identifier 10.1109/TVLSI.2016.2641259

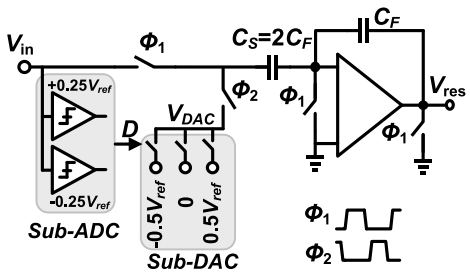



Fig. 1. Circuit implementation of a 1.5-bit stage.

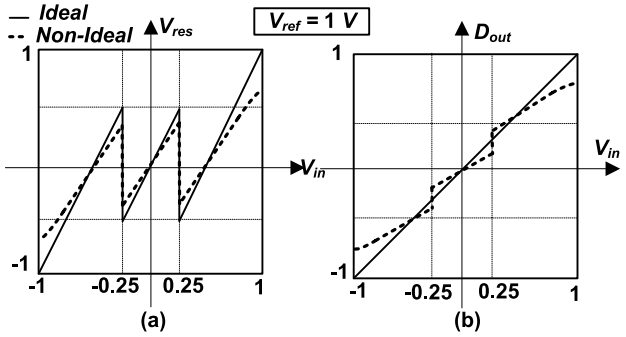



Fig. 2. Effect of circuit nonidealities in the (a) MDAC transfer function and (b) ADC output.

This brief is organized as follows. In Section II, the ADC structure and error modeling are presented. The proposed calibration technique is described in Section III. Section IV is allocated to the circuit design details. Simulation results are presented in Section V. Finally, the conclusion is given in Section VI.

### II. ADC Structure and Error Modeling

A circuit implementation of commonly used 1.5-bit stage is shown in Fig. 1 [7]. This scheme offers the same gain property for the input signal and the DAC path. Hence, the capacitor mismatch and the amplifier gain error can be considered at the same way [7]. In the rest of this brief, all signal voltages are normalized by $V_{\text{ref}}$ for simplicity.

Fig. 2(a) shows the stage transfer function that has two discontinuities at the decision points, $\pm 0.25$. Due to the circuit nonidealities, the transfer function deviates from the ideal case and some missing codes appear at the ADC output around the decision points. Fig. 2(b) shows the ADC transfer function with a nonideal first stage and an ideal backend ADC. Owing to the circuit nonidealities in the first stage, some missing codes appear around $\pm 0.25$.

In order to perform the calibration, a digital domain third-order inverse model is considered by using [7] as

$$V_{\text{in}} = V_{DAC} + \beta_1 V_{\text{res}} + \beta_3 V_{\text{res}}^3$$
$$\beta_1 = 1/\alpha_1, \quad \beta_3 = -\alpha_3/\alpha_1^4. \tag{1}$$

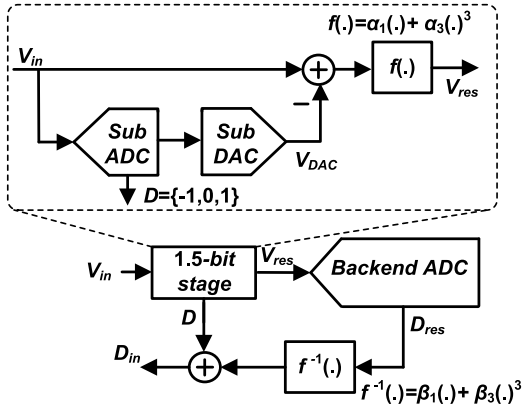



Fig. 3. Stage and its digital calibration model.

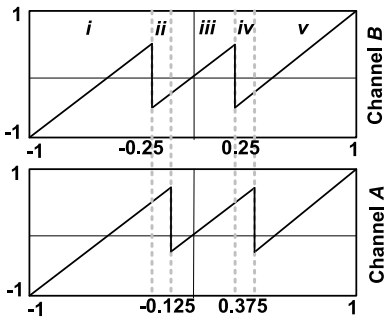



Fig. 4. Stage's transfer function of channels $A$ and $B$ in the split structure.

Here, $\alpha_1$ models the capacitor mismatch and the finite dc gain of the amplifier and $\alpha_3$ denotes the nonlinearity of the amplifier. In practice, higher order terms have a negligible effect on the performance of the ADC, and so, they can be neglected [5], [7].

The digital domain equivalent of (1) will be as [7]

$$D_{\text{in}} = D + \beta_1 D_{\text{res}} + \beta_3 D_{\text{res}}^3 \tag{2}$$

where $D_{\text{in}}$ and $D_{\text{res}}$ are the digital equivalents of $V_{\text{in}}$ and $V_{\text{res}}$, respectively. Therefore, for the calibration of each stage, it is enough that the algorithm extracts $\beta_1$ and $\beta_3$. The first stage and its digital domain calibration model are shown in Fig. 3. It should be mentioned that the ADC calibration starts from the last stage and ends in the first stage. Therefore, in the calibration of $i$th stage, the latter stages have been calibrated already and they are used as an ideal backend ADC to produce the digital equivalent of this stage's output, $D_{\text{res}}$.

## III. Proposed Digital Background Calibration Technique

### A. Split ADC-Based Calibration Technique

In the split ADC structure, two same-pipelined ADCs work simultaneously. The final digital output is achieved by averaging the digital output of two channels. Besides, their subtraction can be used in the calibration process.

The method in [8] shifts the decision points of ADC in one of the channels, called channel $A$, in comparison with their counterparts in channel $B$. Thus, the transfer functions shown in Fig. 4 are produced. The channel $B$ uses the original decision points of a 1.5-bit sub-ADC, i.e., $\pm 0.25$, while the other channel uses $-0.125$ and 0.375 decision points. With these two transfer functions, five different regions are created. In the regions $i$, $iii$, and $v$, these two transfer functions are the same. Whereas, the regions $ii$ and $iv$ are the ones that can be used to extract the calibration coefficients with the LMS algorithm as follows:

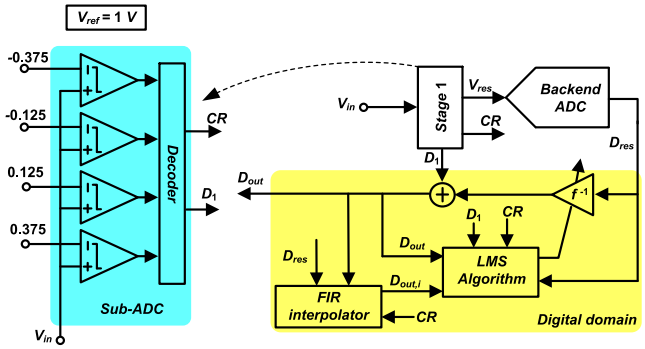



Fig. 5. Structure of the proposed calibration technique.

$$\begin{aligned}\beta_1(n+1) &= \beta_1(n) + \mu_1 e(n)(D_{\text{res},B} - D_{\text{res},A}) \\ \beta_3(n+1) &= \beta_3(n) + \mu_3 e(n)\left(D_{\text{res},B}^3 - D_{\text{res},A}^3\right)\end{aligned} \tag{3}$$

where $e(n) = D_{\text{out},A} - D_{\text{out},B}$ and $\mu_1$ and $\mu_3$ are the update step sizes of the first- and third-order coefficients, respectively. Moreover, $D_{\text{res},A}$ and $D_{\text{res},B}$ denote the digital outputs of backend ADCs for the stage under the calibration in channels $A$ and $B$, respectively.

### B. Proposed Calibration Technique

In order to perform the digital background calibration, the structure of the proposed pipelined ADC has been improved to implement a single channel split ADC. As depicted in Fig. 5, two extra comparators along with an interpolation filter are utilized to implement the dual-mode transfer function of the split pipelined ADC.

Here, unlike the conventional structure, the stage decision points are placed at $-0.375$ and 0.125, respectively. Two extra comparators with decision points at $-0.125$ and 0.375 are added to the stage in order to perform the dual-mode transfer function. The main transfer curve relates to decision points of $-0.375$ and 0.125, while the auxiliary transfer curve is related to $-0.125$ and 0.375.

In the proposed calibration scheme, the difference between the main and auxiliary transfer curves in calibration regions, $-0.375 < V_{\text{in}} < -0.125$ and $0.125 < V_{\text{in}} < 0.375$, are used to estimate the calibration coefficients. This choice for decision points results in twice wider calibration regions in comparison with [8]. Thus, the convergence time of the proposed calibration technique is decreased. The main drawback of this choice is the limited offset voltage tolerance in the comparators.

The main transfer curve is considered for the normal operation of the pipelined ADC, while the auxiliary transfer curve is used in the calibration process. The single channel split ADC structure for the calibration is shown in Fig. 5. When the stage input sample is located in one of the calibration regions, a calibration cycle is done. In each calibration cycle, the stage is configured with the auxiliary transfer curve, while the main transfer curve is estimated with a $2L$ taps finite-impulse response (FIR) interpolator. Indeed, the interpolator and two extra comparators act like a virtual ADC to implement the proposed single channel split pipelined ADC.

The proposed calibration technique is performed adaptively and updates the coefficients at each calibration cycle, which consists of $N$ input samples. Timing diagram of the calibration process is shown in Fig. 6. In each calibration cycle, the ADC produces one sample based on the auxiliary transfer curve, i.e., the desired sample in Fig. 6. When the desired sample is located in the one of calibration regions,

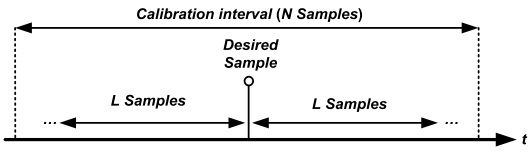



Fig. 6. Timing diagram of the proposed calibration scheme.

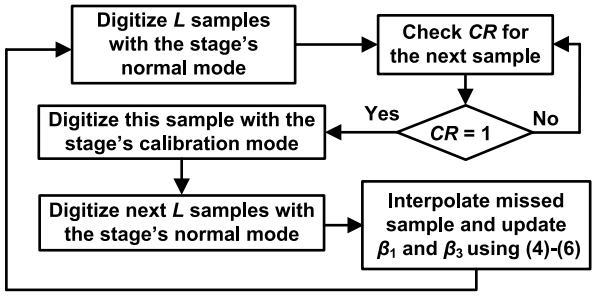



Fig. 7. Flowchart of the proposed calibration technique.

a calibration cycle is done. $L$ samples before and $L$ samples after the desired sample are used in the interpolator to produce the ADC's output based on the main transfer curve. Here, $N$ should be greater than $2L + 1$. In the presented method, $L$ is set to 64, and $N$ is set to 512. Then, the subtraction of the interpolator and ADC's outputs drives an LMS machine to estimate the calibration coefficients as

$$\begin{aligned}\beta_1(n+1) &= \beta_1(n) + \mu_1 e(n)(D_{\text{res}}(n) - D_{\text{res},i}(n)) \\ \beta_3(n+1) &= \beta_3(n) + \mu_3 e(n)\big(D_{\text{res}}^3(n) - D_{\text{res},i}^3(n)\big)\end{aligned} \tag{4}$$

where $D_{\text{res}}$ is the digital equivalent of the first stage output. Moreover, the error signal $e(n)$ is given by

$$e(n) = CR(n) \times (D_{\text{out}}(n) - D_{\text{out},i}(n)) \tag{5}$$

where $D_{\text{out}}$ and $D_{\text{out},i}$ are the digital output of the ADC and the FIR interpolator, respectively. Besides, the control signal $CR(n)$ is high when the input sample is located in the calibration regions. Moreover, $D_{\text{res},i}$ is approximated by using $D_{\text{out},i}$ as

$$\begin{aligned}D_{\text{res},i}(n) = &\frac{1}{\beta_1(n)}[D_{\text{out},i}(n) - D_1(n)] \\ &- \frac{\beta_3(n)}{\beta_1^4(n)}[D_{\text{out},i}(n) - D_1(n)]^3.\end{aligned} \tag{6}$$

The calibration converges when the difference of the ADC and interpolator outputs $e(n)$ is minimized enough. In each calibration cycle, if the input sample does not locate at the calibration regions, i.e., $CR = 0$, the proposed algorithm waits until the next sample to occur in the calibration region.

The flowchart of the presented digital calibration scheme is illustrated in Fig. 7. In each calibration cycle, $L$ samples are digitized with the normal mode transfer function and $(L + 1)$th sample is checked whether to be placed in the calibration regions or not. For a sample in the calibration region, it is digitized with the calibration mode transfer function, and the next $L$ samples are digitized with the normal mode transfer function and then the results are used to update the calibration coefficients. If $(L + 1)$th sample does not place in the calibration regions, the next sample will be checked to see whether it is placed in the calibration regions or not.

The main drawback of the proposed calibration technique is that the interpolator limits the input bandwidth of the ADC. To alleviate this issue, the number of interpolation taps should be considered as large as possible at the cost of increased area and power consumption in the calibration circuitry [9].

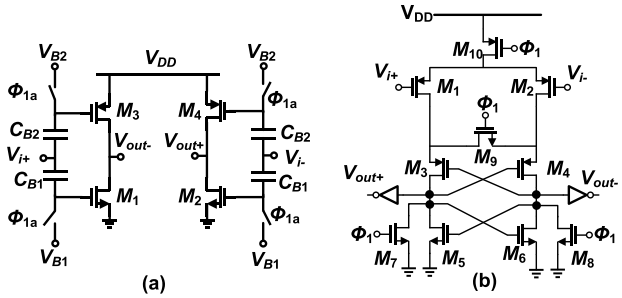



Fig. 8. (a) Topology of the amplifier utilized in the first five gain stages. (b) Topology of the comparators.

## IV. Circuit Design Example

In order to examine the effectiveness of the proposed digital background calibration scheme, a 12-bit, 100 MS/s pipelined ADC is implemented in a standard 90-nm CMOS technology with 1 V power supply. Moreover, by matching the time constant between the signal paths of the first stage [10], the front-end S/H circuit is eliminated to reduce the power consumption. Like [7], due to the thermal noise consideration, the sampling capacitor of the first stage is set to 4 pF. In other stages, the sampling capacitors are scaled down to the fifth stages. All of the sampling capacitors of the backend ADC are set to 0.2 pF. The implemented pipelined ADC is composed of 12 1.5-bit stages followed by a 2-bit flash quantizer. Only the first five stages, which drive larger capacitors, are calibrated rather than the last seven stages. Simple amplifiers with low dc gain and high speed are utilized in the first five stages. The last seven stages along with the 2-bit flash quantizer act as an ideal backend ADC in the calibration. The same technique used in [11] is utilized to implement high dc gain amplifiers to achieve an ideal backend ADC. Simulation results show that the backend ADC has 9.5-bit effective number of bits. Like [5] and [7], in the first and second stages, the first- and third-order errors are compensated, while only the first-order errors are compensated in the third to fifth stages.

### A. Amplifiers and Comparators

For the first five stages, a simple inverter-based amplifier is utilized as shown in Fig. 8(a). It acts as a class AB amplifier with a very low static power. Minimum channel length transistors are used in order to achieve high speed, which limit the dc gain to about 24 dB. As mentioned in [11], an equivalent common-mode feedback circuit can be created in the stage structure to control the output common-mode voltage of the pseudodifferential amplifier. Moreover, because of redundancy in the 1.5-bit sub-ADC, a simple dynamic latch [12] shown in Fig. 8(b) is used to realize the comparators.

### B. Digital Section

The digital section of the proposed calibration technique has been implemented with fixed-point blocks in MATLAB. The calibration process is started from the fifth stage and goes back to the first stage.

In the proposed calibration scheme, the first step is to determine the position of the input signal to see whether the input sample is placed in the calibration regions or not. As illustrated in Fig. 9, the position of the input signal is determined by using two XOR gates followed by an OR gate. In the calibration regions, the digital output of the comparators differs from their counterparts and $CR = 1$.

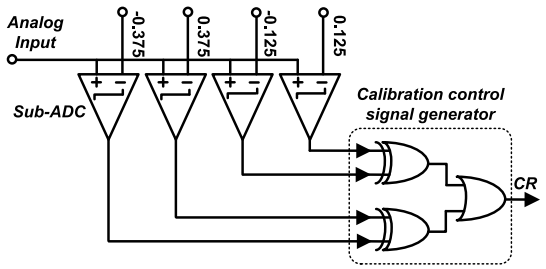



Fig. 9. Calibration control signal generator.

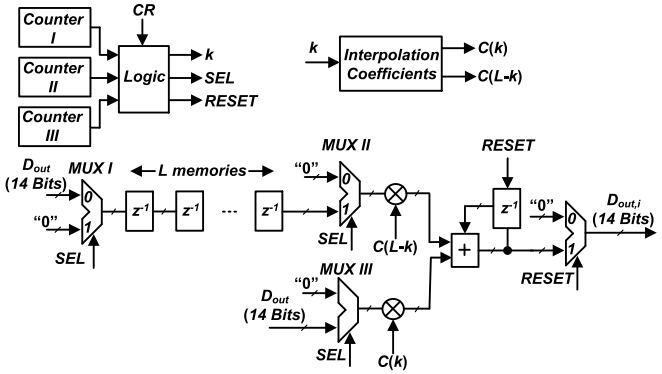



Fig. 10. FIR interpolator and its control signals.

In order to produce the control signals for the FIR interpolator and calibration process, three counters shown in Fig. 10 are utilized. A counter (counter $I$) with the range of $N$ is needed to control the calibration cycles in Fig. 6. A digital comparator is used to compare the output of the counter $I$ and number $N$ in order to generate a RESET signal. Moreover, a counter (counter $II$) with the range of $L$ is needed to control the digital outputs of the pipelined ADC before the desired sample. Besides, the last counter (counter $III$) with the range of $L$ is required for the digital outputs of the pipelined ADC after the desired sample in Fig. 6. Additionally, the calibration coefficients are chosen based on the output of counter $III$. The counter $I$ is the master in producing the controlling signals and the two others are its followers. This counter is utilized to restart the calibration cycles every $N$ samples, and so the calibration procedure updates the calibration coefficients continuously.

As illustrated in Fig. 10, in order to implement the FIR interpolator, $L$ memories are utilized to store the $L$ samples before the desired sample. In every clock cycle before the desired sample, the values of these memories are updated by the digital output of the ADC. After the desired sample, the digital word "0" starts to shift from the first memory to the last one. After $L$ clock cycles, all of the memories have been reset and they are prepared for the next calibration cycle. Also, two multiplexers, the multiplexers $I$ and $II$, are used with the memories. The multiplexer $I$ is utilized in order to store the $L$ samples before the desired sample and to shift the digits "0" after the desired sample. After the desired sample, the stored digital outputs are shifted through the multiplexer $II$ to a multiplier. The output of counter $III$, $k$, controls the interpolation coefficients that are multiplied to the stored digital output of the ADC. Note that the interpolation coefficients $C(k)$ have been calculated in [9] and are utilized here in the interpolator filter.

The multiplexer $III$ is utilized to control the $L$ samples after the desired sample to the input of multiplier. However, the coefficients that are multiplied to the output of multiplexer $III$ differ from the coefficients that are multiplied to the output of multiplexer $II$. The output of the counter $III$, $k$, is utilized to choose the proper coefficient to be multiplied to the output of each multiplexer. Hence, $C(k)$ is multiplied to the outputs of the ADC after the desired signal. Moreover, $C(L-k)$ is multiplied to the stored output. The output of multipliers is added and then stored in an integrator to form the final output of the FIR interpolator. After the desired sample, $L$ clock cycles are needed for the FIR interpolator to produce $D_{\text{out},i}$ which is used in (6) to update $\beta_1$ and $\beta_3$ coefficients.

TABLE I
DIFFERENT STEP SIZES OF THE CALIBRATED STAGES

| Stage number | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| $\mu_1$ | 1/512 | 1/128 | 1/64 | 1/32 | 1/16 |
| $\mu_3$ | 1/8192 | 1/512 | 0 | 0 | 0 |

TABLE II
COMPARISON WITH SEVERAL OTHER CALIBRATION TECHNIQUES

| Ref. | Digital circuit complexity | Convergence time | Additional analog circuit | Calibration coefficients |
|---|---|---|---|---|
| [4] | Low | Short | Reference ADC | $\beta_1$ and DAC error |
| [5] | Medium | Short | 7-bit reference DAC | $\beta_1$ and $\beta_3$ |
| [6] | Low | Medium | Unknown gain in each calibrated stage | $\beta_1$, $\beta_3$, and unknown gain |
| [8] | Low | Short | Replica path | $\beta_1$, DAC error and gain error |
| This Work | Medium | Medium | Two extra comparators in each calibrated stage | $\beta_1$ and $\beta_3$ |

## V. SIMULATION RESULTS

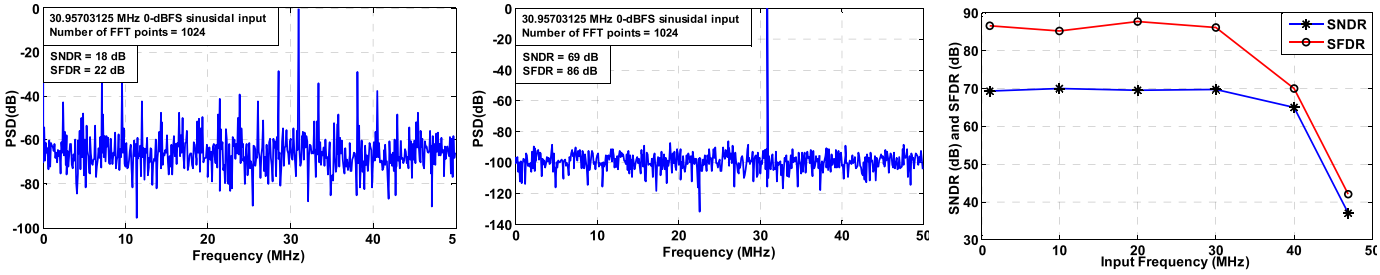
The described 12-bit 100 MS/s pipelined ADC is simulated and its digital calibration is implemented using fixed-point blocks with $N = 512$ and $L = 64$. The output PSD of the simulated ADC before and after the calibration is depicted in Fig. 11(a) and (b), respectively. As it is seen, before the calibration, the spurious free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are about 22 and 18 dB, respectively. However, after the calibration, SFDR and SNDR are improved to 86 and 69 dB, respectively.

For further investigation of the proposed digital background calibration technique, both SNDR and SFDR of the simulated ADC versus the input signal frequency are plotted in Fig. 11(c). As it is clear, the SFDR and SNDR are almost constant in the 0.4 of Nyquist band. As it is evident, the interpolation filter limits the bandwidth of the input signal. The bandwidth of the input signal is limited to 0.4 of Nyquist band. The simulated ADC consumes only 6.7 mW from a single 1 V power supply.

Like [1], the calibration coefficients have been performed on all the stages concurrently. However, the calibration update size decreases from the fifth stage to the first stage. The update size of different stages is listed in Table I. In Fig. 12, the convergence of the SNDR is plotted versus the calibration intervals. As it is evident, the proposed calibration technique takes about $4 \times 10^4$ calibration intervals to converge.

Monte Carlo simulations are done to investigate the sensitivity of the proposed calibration technique to the change in dc gain variation of amplifier and capacitor mismatch. For 5% dc gain variation in amplifier and 0.1% capacitor, the standard variation of SNDR is about 2 dB.

The proposed calibration technique is compared with several other schemes in Table II. Indeed, it is a semiequalization-based technique




(a) (b) (c)

Fig. 11. Output spectrum (a) before calibration and (b) after calibration. (c) Simulated SNDR and SFDR versus the input signal frequency.

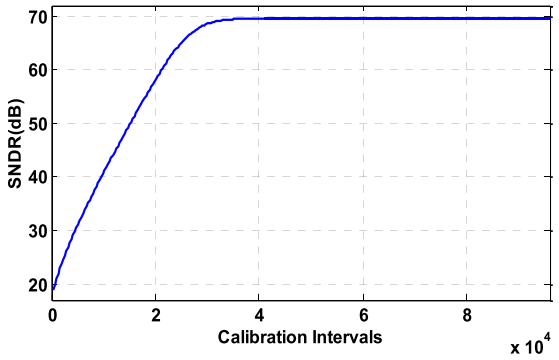



Fig. 12. Convergence of the SNDR versus the calibration intervals.

that benefits from the short convergence time of the equalization-based techniques without any replica path or reference ADC. On the other hand, it limits the bandwidth of the analog input signal and it converges when the input signal is busy enough around the calibration regions.

## VI. Conclusion

In this brief, a new digital background calibration method has been presented. It uses an interpolation filter and two extra comparators to create an auxiliary transfer function for the ADC, and so to extract the inverse coefficients. The presented algorithm is able to estimate and correct the gain error and the nonlinearity of the amplifier. The only overheads of the proposed technique are two extra comparators in each stage and some digital circuits that consume negligible power. This technique improves both the ADC's SNDR and SFDR considerably.

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