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# A power conversion chain with an internally-set voltage reference and reusing the power receiver coil for wireless bio-implants

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ABSTRACT

In this paper, a power conversion chain (PCC) with an internally-set voltage reference is presented. It is comprised of a power receiver coil, an active rectifier and a novel buck-boost converter. The output voltage of the PCC is set by using the parameters of a new buck-boost converter control unit in order to avoid utilizing an extra voltage reference circuit. Furthermore, the proposed PCC reuses the power receiver coil to facilitate the realization of the buck-boost converter. This way, the efficiency of the proposed PCC gets almost independent of the receiving coil voltage amplitude. In addition, the proposed buck-boost converter significantly reduces the size of the PCC and makes it suitable for wireless power transfer via inductive links in bio-implant applications. It should be noted that employing an active rectifier followed by the proposed buck-boost converter enhances the PCC end-to-end efficiency. The proposed PCC is simulated for the input received signal with a frequency of 10 MHz and an amplitude variation within 3–7 V. The simulation results show that the efficiency variation is less than 2.6% and the achieved maximum efficiency is 80.4% and 63.4% for the proposed converter and PCC, respectively. For further verification of the proposed idea, a proof-of-concept prototype is implemented and experimental results are provided.

## 1. Introduction

Nowadays, power transmission via inductive links for implantable medical devices (IMDs) considerably becomes important and pervasive. The reason is that it is an alternative option for the battery-powered cases that can decrease the total size of the IMD and reduce the probability of infection. Power transmission via inductive links can be used for applications such as cochlear implants [1], visual prosthesis [2] and invasive wireless neural recording [3]. Significant challenges in today's IMD design are related to the size of IMD and the power consumption [3,4].

Fig. 1 shows a typical power conversion chain (PCC) which is used in IMDs. The PCC converts the input AC voltage to a DC output voltage. After rectification, there should be a voltage regulator to maintain the output voltage at a certain level, by comparing it to a voltage reference. Thus, this voltage can be used as a supply voltage for other parts of the implant. The conventional structure used in bio-implants is the linear regulators [5,6]. In power transfer via inductive links, the amplitude of the received voltage may vary a lot due to the variation in the distance or the angle between the power transmitting and receiving coils. Moreover, the other parameters such as the moisture of the path between these two coils would be able to have influence on the received voltage amplitude.

In linear voltage regulators, the output voltage level is constant. As a result, the variation in the input level can increase voltage drop across the regulator. This can significantly decrease the regulator efficiency. The considered problem would be diminished using two methods. The first method reduces the power loss by controlling the power transmitter gain in the driver of the outer coil [7]. Using this method, when the received voltage level is decreased, the power transmitter gain increases and the transmitter coil transmits higher power to compensate for the received voltage. In return, when the received voltage level is increased, the power transmitter gain is decreased to compensate. This method needs a variable gain power transmitter in the primary side of the coil. In addition, an analog-to-digital converter, and also, a data transmitter in the implant side are needed to gather the received voltage level information and send them for the power transmitter. Besides, imposing an additional reverse path to send the received voltage level information for the power transmitter from the implant can significantly increase the size of the implant, which is critical in the bio-implant applications.

The second method in order to get rid of the efficiency degradation by input voltage variation is the use of nonlinear voltage converter as introduced by the previous work of the authors in Ref. [8]. In the mentioned reference, by employing a buck-boost converter instead of a

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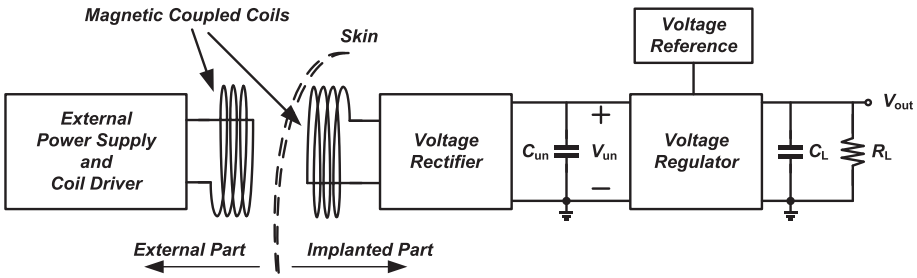


**Fig. 1.** Power conversion chain structure in bio-implant systems.

linear regulator, the efficiency variation is decreased from 35% to less than 8% for input amplitude voltage variation of 3–6 V [8]. The designed converter achieves an output current range of 10 μA to 4 mA without the problem of instability. Moreover, the output DC voltage level could be higher or lower than the amplitude of the received input voltage. The main problem in the nonlinear converters is the existence of a large bulky inductor that is inevitably off-chip and considerably increases the size of the implant. Reusing the inductor of the power receiver coil not only resolves the problem of the large off-chip coil but also gives a very small converter by adding just four power switches and a control circuit as well. This is the main idea of the previous work of the authors [8].

Voltage reference is an essential block in both linear and nonlinear converters. The bandgap reference is mostly employed for this purpose. The quiescent current of the bandgap voltage reference degrades the total power efficiency of the PCC. Recently, many researches have been done to solve this drawback [9,10]. Nowadays, many efforts have been done to replace the bandgap circuit by a completely CMOS reference [9,11]. However, CMOS references most often could not be a suitable alternative since they would bring up various problems causing different challenges for designers. For example, the CMOS reference which is introduced in Ref. [11] and is used in Ref. [8], begins to oscillate with a little change in the value of its elements. Furthermore, two off-chip resistors have been used in order to compensate for the variations in different process corner cases resulting in enlarged size of IMD [8].

Drawbacks of using a bandgap voltage reference encouraged the authors to have more attention to the voltage reference matter in PCC. Therefore, a new structure has been suggested that completely removes the voltage reference from the PCC. The proposed structure is according to the matter in which there is a control circuit similar to the feedback in nonlinear converters. Thanks to the feedback circuit, the output voltage of the converter can be regulated due to the loop parameters. Thus, this method provides a situation in which no voltage reference block is required. Removing the voltage reference not only enhances the efficiency of PCC by omitting its quiescent current but also improves the circuit behavior against the process corner cases, temperature variations and device mismatches in comparison with the other CMOS voltage references.

Therefore, the effect of temperature and process variations on the output voltage is negligible. In this way, the quiescent current of the voltage reference is removed and the converter output voltage could be regulated at any desirable value provided by the converter. Furthermore, by eliminating the voltage reference, the size of the IMD is further decreased.

The proposed power receiver chain introduced in Ref. [8] has been implemented by a passive rectifier. Although this converter has a high efficiency that is almost independent of the input voltage, the total PCC efficiency is low due to the passive rectifier. In this paper, an active rectifier is employed in the PCC structure to remedy this issue. The new structure not only improves the total efficiency significantly, but also shows a very better consistency of the converter efficiency against the variations of the input voltage. Using this structure, the efficiency variation is decreased from 8% for the input voltage range of 3–6 V to less than 2.6% for an input range of 3–7 V.

To validate the simulation results, the suggested PCC structure has

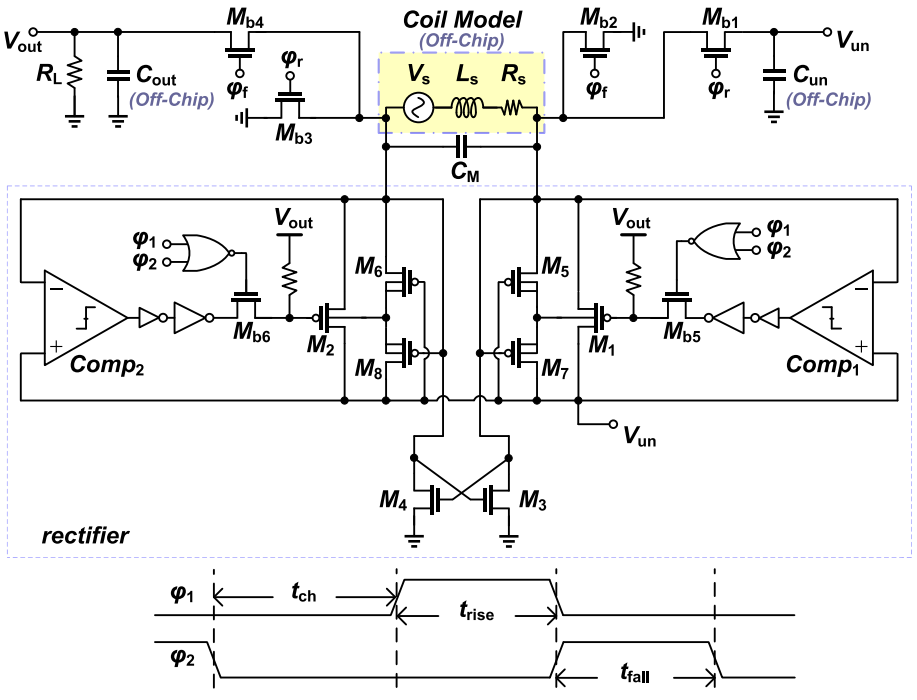


**Fig. 2.** Proposed inductor-reused buck-boost converter with an active rectifier.

been designed and implemented using off-chip components. It demonstrates the possibility of reusing the power receiver coil in the structure of the nonlinear voltage converter, and also, the adjustment of the output voltage with voltage converter's control circuit in absence of the voltage reference.

This paper describes the design, analysis and simulation of the proposed coil inductor reused PCC with an internally-set voltage reference. It also focuses in detail on the design of the output voltage setting by feedback loop parameters. Besides, the measurement results of a proof-of-concept prototype are provided. The rest of the paper has been organized as follows. In Section 2, the concept of the proposed buck-boost converter by reusing the power receiver coil with an active rectifier is described. Section 3 illustrates the proposed converter with an internally-set voltage reference. Simulation results are presented in Section 4, and Section 5 concludes the paper.

## 2. The concept of the inductor reusing in a buck-boost converter

Fig. 2 shows the proposed inductor-reused buck-boost converter. In this figure, the power receiver coil is modeled by $L_s$, $R_s$ and $V_s$ [12], which stand for self-inductance, series resistance and sinusoidal received voltage, respectively. As $L_s$ is a large off-chip inductor, it can be reused as a proper alternative to realize a buck-boost converter. To do this, the operation of this coil is divided into two time intervals. In the first time interval, the power receiver coil in IMD receives the power that is transmitted by the outer coil. Fig. 3 represents the circuit in this phase. This power is stored in the output capacitor of the rectifier, which is shown by $C_{un}$ in the figure. At the second time interval, the coil is working in the structure of the buck-boost converter to transfer the received power in $C_{un}$ to desirable DC voltage level at the output capacitor. In this interval, the only difference between the proposed converter and common buck-boost converters is that instead of a DC voltage source at the input of the converter, the initial voltage of $C_{un}$ is applied as an input voltage source. In Fig. 2, $\varphi_1$ and $\varphi_2$ are connected to $\varphi_r$ and $\varphi_f$ terminals, respectively. In the next section, it would be seen that $\varphi_1$ and $\varphi_2$ will be the input of the control unit and $\varphi_r$ and $\varphi_f$ will be connected to the output of the control unit. According to $\varphi_1$ and $\varphi_2$, there are three phases of operation: power receiving phase where both of $\varphi_1$ and $\varphi_2$ are low, inductor charging phase that $\varphi_1$ is high and $\varphi_2$ is low and inductor discharging phase that $\varphi_2$ is high and $\varphi_1$ is low. These three phases are explained in details in the following section.

### 2.1. Power receiving phase

In Fig. 2, the circuits inside the dashed line, labeled by the rectifier, work as a full-wave active rectifier [13]. In the power receiving phase, the rectifier conducts the received sinusoidal power to $C_{un}$. This power is stored in this capacitor in order to apply in the next phase to the input of the buck-boost converter. The operation of the circuit in this phase is represented in Fig. 3. Switches $M_{b1}$-$M_{b4}$ are open during power receiving phase and switches $M_{b5}$ and $M_{b6}$ are closed. $C_M$ is utilized as input matching capacitor. This capacitor should be resonated with the self-inductance of the power receiving coil at the power receiving frequency. The capacitor $C_M$ is obtained from the resonance frequency as:

$$C_M = \frac{L_s}{L_s^2\omega_0^2 + R_s^2} \tag{1}$$

where $\omega_0$ is the resonance frequency of $L_s$ and $C_M$. In Fig. 3, once the power signal is received via the coil, when $V_{in1}$ is positive, the voltage at $V_{in2}$ is negative and vice versa. For the case in which $V_{in1}$ is positive, the output of the $COMP_1$ becomes low. Since during this phase $M_{b5}$ is on, the gate of switch $M_1$ goes to low and makes it on. Just at this moment, the output of the comparator $COMP_2$ is high since its negative input is smaller than its positive one. This causes $M_2$ to be turned off. On the other hand, in this condition, $M_4$ is turned on while $M_3$ is turned off and as a result $V_{in2}$ is connected to the ground. Therefore, in the first cycle of the received signal, $C_{un}$ is charged through $M_1$. In the next cycle, the negative input of comparator $COMP_1$ is lower than its positive input, $M_1$ is off, $M_2$ and $M_3$ are on and $C_{un}$ is charged through $M_2$. In the next phases (i.e.; $\varphi_r$ and $\varphi_f$) that $M_{b5}$ and $M_{b6}$ are open, $M_1$ and $M_2$ are off due to the pull-up resistors that are connected to their gate terminal. Dynamic body biasing technique has been used for $M_1$ and $M_2$ by adding auxiliary PMOS transistors, $M_5$ to $M_8$. These transistors automatically connect the bulk voltage of $M_1$ and $M_2$ to the highest potential among the input and output voltages of the rectifier, i.e. max ($V_{in1}$, $V_{un}$) and max ($V_{in2}$, $V_{un}$) in Fig. 3, respectively.

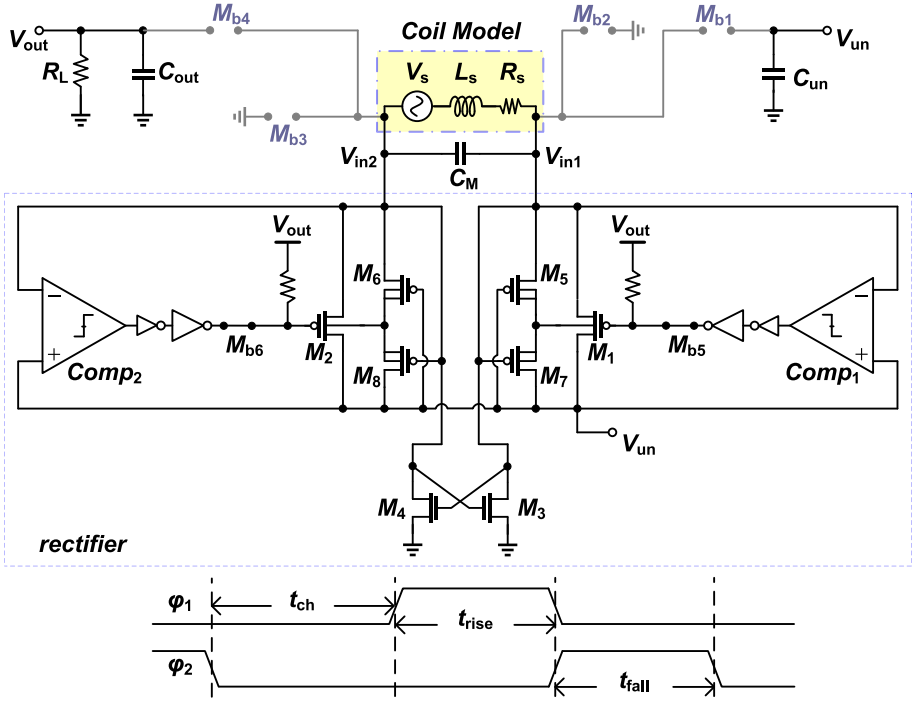


**Fig. 3.** Proposed inductor-reused buck-boost converter in power receiving phase.

The duration of this time interval should be much larger than the period of the sinusoidal received voltage to give enough time to $V_s$ to charge $C_{un}$ to its maximum value. In other words, it takes several periods for $V_s$ to charge $C_{un}$ to its maximum value, depending on the value of $C_{un}$ and the amplitude of $V_s$. Therefore, $t_{ch}$ should be larger than the period of $V_s$. $C_{un}$ is charged to the maximum amplitude of $V_s$ during this phase and this voltage is used as an initial condition of this capacitor at the start of the next phase. As $C_{un}$ is charged to its maximum value at the end of the power receiving phase, it pulls no more current and the current inductor is zero. It means that at the start of the next phase, the initial condition of the inductor is zero.

### 2.2. Inductor charging phase

During the inductor charging phase, $M_{b1}$ and $M_{b3}$ switches are closed and $L_s$ is charged by the energy that stored in $C_{un}$. This is equal to the charging phase in the conventional buck-boost converters. Fig. 4 shows the converter in this phase in which $M_{b5}$ and $M_{b6}$ are open and this way the rectifier is excluded from the converter. In addition, $C_M$ is paralleled with $C_{un}$ and since it is very smaller than $C_{un}$, it can be ignored. Here, $V_{o1}$ notates the initial condition of $C_{un}$ at the start of this phase, which is equal to the amplitude of $V_s$. Initial condition of the inductor is zero because $C_{un}$ is charged to its maximum value at the end of the previous phase and drains no more current. Therefore, there is a simple series RLC circuit in which the current of the inductor starts to increase by $V_{o1}$. The time that the total energy of $C_{un}$ is discharged to $L_s$, determines the duration of the inductor charging phase.

Two separate voltage sources, specified as $V_{o1}$ and $V_s$, should be taking into account to analyze the RLC loop. As $V_{o1}$ is a DC voltage and $V_s$ is a sinusoidal voltage reference, transient analysis and steady-state analysis should be utilized, respectively, to determine the current of the inductor at the end of this phase. This current is used as the initial condition of the inductor at the beginning of the next phase. The transient current of the inductor has been analyzed and calculated in Ref. [8]. By adding the effect of $C_M$ it is obtained as:

$$i_{t,r}(t) = A_0 e^{-\alpha t} \sin\left(\sqrt{\omega_0^2 - \alpha^2}\, t\right) \tag{2}$$

where $i_{t,r}(t)$ is the transient response of the inductor current accounts for $V_{o1}$. $\alpha = R_s/2L_s$ is the damping coefficient, $\omega_0 = 1/\sqrt{L_s(C_{un}+C_M)}$ is the resonance frequency and $A_0 = V_{o1}/L_s\sqrt{\omega_0^2 - \alpha^2}$ (A). The current $i_{t,r}(t)$ reaches to its maximum value within $t_{rise}$ which determines the time period of inductor charging phase and it is obtained as:

$$t_{rise} = \frac{\arctan\left(\frac{-\alpha}{\sqrt{\omega_0^2-\alpha^2}}\right) + \frac{\pi}{2}}{\sqrt{\omega_0^2 - \alpha^2}} \tag{3}$$

The current magnitude of the inductor, $I_{s,r}(j\omega)$, owing to the voltage source $V_s$ is given by:

$$\left|I_{s,r}(j\omega)\right| = |V_s(j\omega)| \times \left|\frac{(C_{un}+C_M)\sqrt{L_sC_M - R_s^2C_M^2}}{R_s(C_{un}+C_M)\sqrt{L_sC_M - R_s^2C_M^2} + j\left(C_{un}L_s - R_s^2C_M(C_{un}+C_M)\right)}\right| \tag{4}$$

The minimum total current of the inductor at the end of this phase can be expressed as:

$$i_{L,r(min)}(t_{rise}) = |i_{t,r}(t_{rise})| - |I_{s,r}(j\omega)| \tag{5}$$

where $I_{s,r}(j\omega)$ is the current amplitude of the inductor owing to the voltage source $V_s$. $i_{L,r(min)}(t_{rise})$ is the minimum initial condition of the inductor at the start of the next phase. As the energy of $C_{un}$ and $C_M$ at the end of this time interval is completely discharged to $L_s$, the initial condition of $C_M$ at the start of the next phase is zero.

### 2.3. Inductor discharging phase

During the inductor discharging phase, $M_{b1,3,5,6}$ switches are open and $M_{b2,4}$ switches are closed. Therefore, the energy of $L_s$ is delivered to $C_{out}$ in order to drive the load. $C_M$ is paralleled with $C_{out}$ as $M_{b2}$ is closed and because it is very smaller than $C_{out}$, it can be ignored. Fig. 5 shows that this phase is completely like the discharge phase in conventional buck-boost converters. The initial current of the inductor is defined as $I_0$ and the DC voltage of the output is assumed as $V_{o2}$. It could be obviously

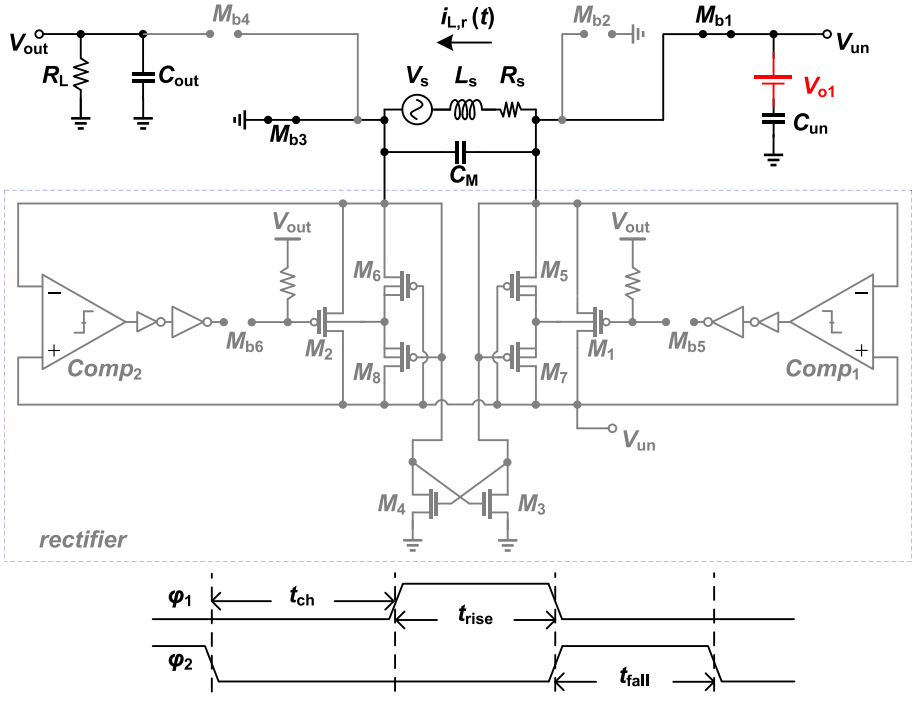


**Fig. 4.** Proposed inductor-reused buck-boost converter in inductor charging phase.

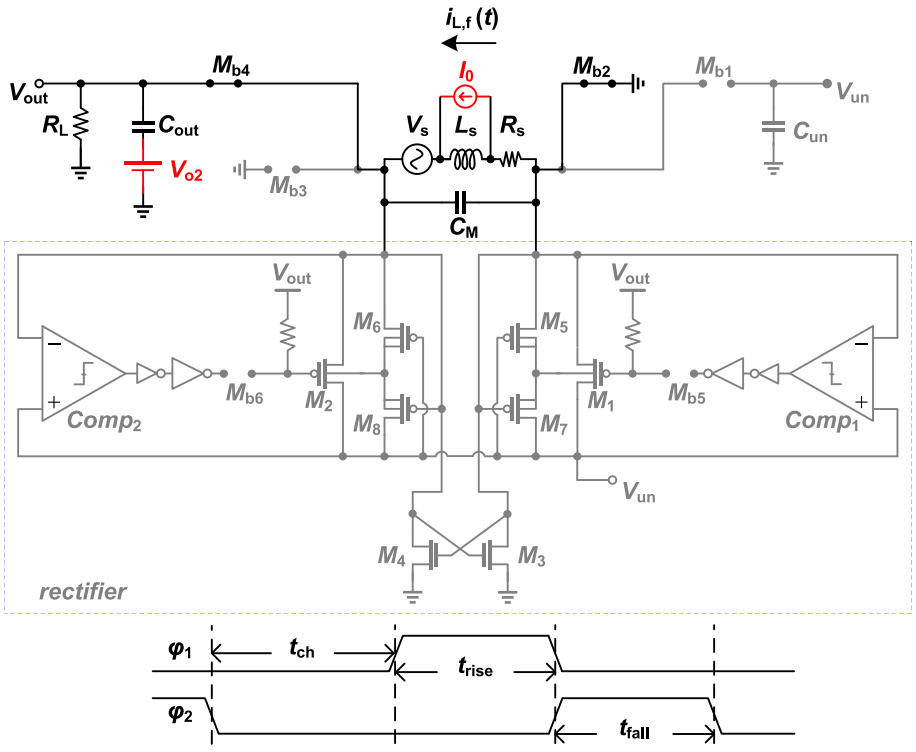


**Fig. 5.** Proposed inductor-reused buck-boost converter in inductor discharging phase.

seen that the rectifier is excluded from the converter during the inductor discharging phase and the equivalent circuit can be considered as a mere RLC loop.

The time in which $i_{L,f}(t)$ reaches to zero, determines the time duration of this phase and is notated as $t_{fall}$. To obtain $t_{fall}$, the effect of three different voltage sources on the $i_{L,f}(t)$ should be considered: $V_{o2}$ and $I_0$ as initial conditions of $C_{out}$ and $L_s$, respectively, and $v_s(t)$. It should be noted that $V_{o2}$ is the same as the output DC voltage of the converter. The response of the circuit to $V_{o2}$ and $I_0$ is determined by solving the following equation:

$$\frac{d^2\left(i_{t,f}(t)\right)}{dt^2}+\left(\frac{R_s}{L_s}+\frac{1}{(C_L+C_M)R_L}\right)\frac{d\left(i_{t,f}(t)\right)}{dt}+\frac{1}{L_s(C_L+C_M)}\left(1+\frac{R_s}{R_L}\right)i_{t,f}(t)=\frac{-1}{L_s(C_L+C_M)}\left(1+\frac{R_s}{R_L}\right)I_0 \tag{6}$$

where $i_{t,f}(t)$ is the transient current response of the inductor to $I_0$ and $V_{o2}$. If the effect of $v_s(t)$ on the total inductor current, $i_{L,f}(t)$, is represented by $i_{s,f}(t)$, then the amplitude of this current can be given by:

$$|I_{s,f}(j\omega_0)|=\frac{\sqrt{1+(R_L(C_{out}+C_M)\omega_0)^2}\times|V_s(j\omega_0)|}{\sqrt{(R_L+R_s-R_LL_s(C_{out}+C_M)\omega_0^2)^2+(R_sR_L(C_{out}+C_M)+L_s)^2\omega_0^2}} \tag{7}$$

where $|I_{s,f}(j\omega)|$ is the Fourier transform of $i_{s,f}(t)$ and $\omega_0$ is obtained from equation (1).

During this phase, $i_{L,f}(t)$ should be positive. A negative current significantly diminishes the efficiency. Relation (8) guarantees the positivity of $i_{L,f}(t)$.

$$i_{t,f}(t)\geq\left(i_{s,f}(t)\right)_{p-p} \tag{8}$$

where $i_{s,f}(t)$ is the effect of $v_s(t)$ on the total inductor current and $(i_{s,f}(t))_{p\text{-}p}$ is its peak-to-peak amplitude. The pulse width of $\varphi_2$, notated as $t_{fall}$, can be calculated as:

$$i_{t,f}\left(t_{fall}\right)=\left(i_{s,f}\left(t_{fall}\right)\right)_{p-p} \tag{9}$$

## 3. The proposed inductor-reused converter with an internally-set voltage reference

To regulate the output voltage of a nonlinear converter, a control circuit unit is required to adjust the timing of the converter switches. Traditionally this control unit regulates the converter output voltage by comparing it with a voltage reference. If it was smaller than the voltage reference, the converter would have its ordinary operation and the control unit allows the energy to transfer from the input to the output. However, if the converter output voltage were higher than the voltage reference, the control unit would not allow the energy transfer to the output by opening the switches. As a result, the converter output voltage does not increase and this way, the control unit works as a feedback to regulate the converter output voltage. The importance of the voltage reference is that any change in its voltage level, directly changes the converter output voltage. Accordingly, its operation in different process corner cases is very crucial.

A structure is presented here to simplify the PCC by removing the voltage reference and it still has a noticeable output voltage consistency against the temperature, process and received voltage amplitude variations. In addition, the quiescent current of the voltage reference is eliminated as this block is removed, and consequently, the total efficiency of PCC is improved. The basis of the proposed structure is to make two different linear ratios of the converter output voltage and compare them with each other. Since these two paths have different slopes, they become equal for a special value of the output voltage. Exactly at this time, the output of the comparator switches from 1 to 0. If at the transition time of the comparator, switches of the converter become open, the output voltage will be regulated at the same value. This value of the output voltage can be set to the desirable values by changing the slope of these two paths. The proposed control circuit has been represented in Fig. 6(a). As it is seen, one ratio of $V_{out}$ is made by the resistors ratio and the other path is provided by nMOS transistors ratio. The output of these two paths would be compared by a comparator. The internal circuit of the

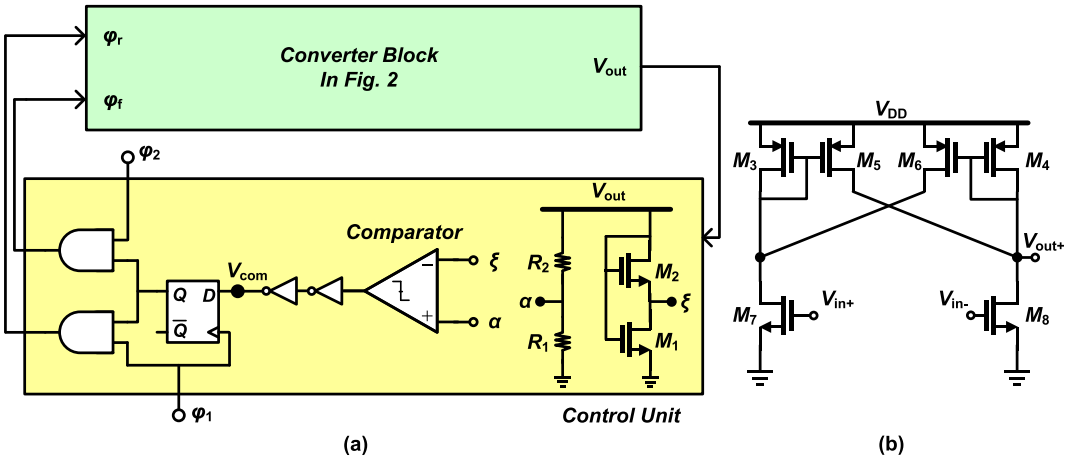


**Fig. 6.** (a) Control unit circuit of the proposed inductor-reused buck-boost converter with an internally-set voltage reference and (b) Utilized comparator in Fig. 6(a).

comparator in Fig. 6(a) has been shown in Fig. 6(b). In Fig. 6(a), when the converter starts to operate for the first time, $V_{out}$ gradually increases from zero. For the small values of $V_{out}$, $\alpha$ starts to increase, since it is a resistive ratio of $V_{out}$. From Fig. 6(a), the value of $\alpha$ can be expressed as:

$$\alpha = \frac{R_1}{R_1 + R_2} V_{out} = \frac{1}{1 + \rho_R} V_{out} \tag{10}$$

where $\rho_R = R_2/R_1$.

However, $\xi$ remains zero, so long as $V_{out}$ is less than $V_{TH}$ of nMOS transistors. Therefore, the output of the comparator and D-flip flop would be high since $\alpha$ is larger than $\xi$. Thus, $\varphi_1$ and $\varphi_2$ are applied to $\varphi_r$ and $\varphi_f$, respectively, which results in ordinary operation of the converter. It results in increment of $V_{out}$ until it reaches to $V_{TH}$ of nMOS transistors to turn these transistors on. In Fig. 6(a), $M_1$ is always in triode region since its drain-source voltage is equal to its gate-source voltage minus $V_{GS}$ of $M_2$. In contrast, $M_2$ is always in saturation region since it has a diode-connected structure. $I_{D1} = I_{D2}$ results in the following equation:

$$\mu_n C_{ox} \left(\frac{W}{L}\right)_1 \left[ (V_{GS1} - V_{TH1}) V_{DS1} - \frac{1}{2} V_{DS1}^2 \right] = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2 \tag{11}$$

where $\mu_n$, $C_{ox}$, $V_{TH}$, $(W/L)_1$ and $(W/L)_2$ are electron mobility, gate capacitance per unit area, threshold voltage, and aspect ratio of $M_1$ and $M_2$, respectively. $\xi$ would be obtained with solving the following second-order equation by substitution of $V_{DS1}$, $V_{GS1}$ and $V_{GS2}$ with $\xi$, $V_{out}$ and $(V_{out} - \xi)$, respectively.

$$\xi^2 - 2\left[ V_{out} - \frac{\gamma_W V_{TH1} + V_{TH2}}{1 + \gamma_W} \right] \xi + \frac{(V_{out} - V_{TH2})^2}{1 + \gamma_W} = 0 \tag{12}$$

where $\gamma_W = (W/L)_1/(W/L)_2$ which has a constant value. By solving (12), the acceptable value of $\xi$, for which $M_1$ remains in the triode region, is obtained as:

$$\xi = \left(1 - \sqrt{\frac{\gamma_W}{1 + \gamma_W}}\right) V_{out} - \frac{V_{TH2} - \left(\sqrt{\gamma_W(\gamma_W + 1)} - \gamma_W\right) V_{TH1}}{1 + \gamma_W} \tag{13}$$

$V_{out}$ is set in a certain value in which $\alpha$ and $\xi$ become equal. So its desired value can be obtained as:

$$V_{out} = \frac{V_{TH2} - \left(\sqrt{\gamma_W(\gamma_W + 1)} - \gamma_W\right) V_{TH1}}{(\gamma_W + 1)\left(\frac{\rho_R}{\rho_R + 1} - \sqrt{\frac{\gamma_W}{\gamma_W + 1}}\right)} \tag{14}$$

For values of $V_{out}$ that are smaller than equation (14), $\varphi_1$ and $\varphi_2$ are applied to $\varphi_r$ and $\varphi_f$, respectively. However, as the value of $V_{out}$ become higher than the value of equation (14), output of the comparator in Fig. 6(a) will switch to zero. Accordingly, with the next positive edge of $\varphi_1$, the output of D-flip flop becomes zero to open all of the converter switches. In this way, any excess energy cannot transfer to the output of the converter and $V_{out}$ would remain at the same desired value. So, as long as $V_{out}$ is higher than the value of equation (14), the switches are open. However, as $V_{out}$ becomes lower than this value, $\varphi_1$ and $\varphi_2$ are applied to the converter again at the next positive edge of $\varphi_1$. In this way, the output of the converter will be regulated at the desired value without the need for a voltage reference.

The role of D-flip flop is to prevent from the power circulate when $V_{out}$ reaches to its desired value. In this regard, assume in phase $\varphi_2$, $V_{out}$ increases until $\xi$ goes higher than $\alpha$ and the output of the comparator goes low to open the converter switches. If the output of the comparator is applied to the converter switches exactly at this time, the excess energy in the inductor cannot be transferred to the output. Therefore, this energy will return to $C_{un}$ through the rectifier. Current circulation in the circuit causes the waste of energy and as a result, the efficiency is reduced. The D-flip flop in return allows the energy of the inductor to flow to the output capacitance completely. It will open the switches at the next positive edge of $\varphi_1$. Therefore, there would be no current circulation in the circuit.

It is known that the coefficients composed of the ratio of two analogous constants (e.g.; $\gamma_W = (W/L)_1/(W/L)_2$ and $\rho_R = R_2/R_1$) show better robustness against the process variations. Furthermore, $M_1$ has no body effect since $V_{SB\ (M1)} = 0$, and thus, a negligible variation for $V_{TH1}$ is also expected. On the other hand, as shown in Fig. 6(a), $M_1$ is biased in the triode region and it can be conceived as a degenerated resistor providing a series-series negative feedback path for $M_2$. This way, the variation of $V_{TH2}$ is significantly compensated. Thus, it is concluded that the voltage at $V_{out}$ calculated in (14) remains almost the same in different corner cases of process, temperature variations and device mismatches. In addition, the aspect ratio of $M_1$ and $M_2$ and the values of $R_1$ and $R_2$ can be chosen in order to significantly reduce their currents in contrast to the converter output current. Therefore, the robustness of the proposed converter output voltage is even better than most of the converters equipped with the conventional voltage reference.

## 4. Simulation results

To evaluate the functionality of the proposed PCC, a design example of the proposed inductor-reused buck-boost converter with an internally-set voltage reference is presented. In addition, the circuit-level simulation results are provided in this section. These simulations are performed in

Cadence environment using TSMC 0.18 μm CMOS technology. The values of $L_s$ and $R_s$ are considered to be 2 μH and 0.5 Ω, respectively, which are according to the experimental results [4]. The received power frequency is considered to be 10 MHz because the frequencies in this range have minimum losses for in-body wireless power transfer [14]. As illustrated in Ref. [8], $C_{un} = 200$ nF gives a fast response in inductor charging phase. The (W/L) of power switches are selected according to the maximum load current. However, if they are chosen so large, their parasitic capacitors will affect the time constants of buck-boost operation phases of the converter. Furthermore, it is possible that PCC to receive power signals with voltage amplitude more than 2–3 V. Hence, the thick oxide transistors of TSMC 0.18 μm CMOS process are utilized. The aspect ratio of all power switches is $(W/L) = 50 \times 64$ μm/0.35 μm.

The transient simulations of the circuit shown in Fig. 6(a) are performed. Here, the values of $R_1$ and $R_2$ are designed to have $V_{out} = 1$ V with 200 kHz switching frequency. Simulation results of this circuit are shown in Fig. 7. As it is seen, when $V_{out}$ starts to increase from zero, $\xi$ is smaller than $\alpha$. However, as $V_{out}$ reaches more than 1 V, $\xi$ becomes larger than $\alpha$ and the output of the comparator, which is notated by $V_{com}$, is reversed. So, at the next phases of $\varphi_1$ and $\varphi_2$, the signals $\varphi_r$ and $\varphi_f$ shown in Fig. 6(a) remain at low state and thus no energy would transfer to the buck-boost converter output. As a result, the voltage $V_{out}$ remains at the same value of 1 V. So, it can be concluded that when $V_{out}$ reaches to 1 V (or any desired value), the frequency of the switching signals applied to the converter, $\varphi_r$ and $\varphi_f$, is reduced. Fig. 8 shows the power spectral density (PSD) of $V_{out}$. To better show the frequency components up to the maximum frequency of the circuit, Fig. 8 is divided into two sections by attributing linear X-axis for low frequencies and logarithmic X-axis for high frequencies. As it is clear, the frequency components at 3.32 kHz and its harmonics are the dominant frequencies appeared at the converter output. From transient response of $V_{out}$ in Fig. 7, it is obvious that 3.32 kHz is the same switching frequency, $\varphi_r$ and $\varphi_f$, when $V_{out}$ reaches to its desired value. According to Fig. 8, the largest spurious component in the spectrum of $V_{out}$ has been suppressed more than 45 dB in accordance with the DC component (i.e.; 0 dB). This shows that the negligible amount of ripple voltage can be expected as shown in Fig. 7. As represented in the figure, the output ripple is less than ±10 mV.

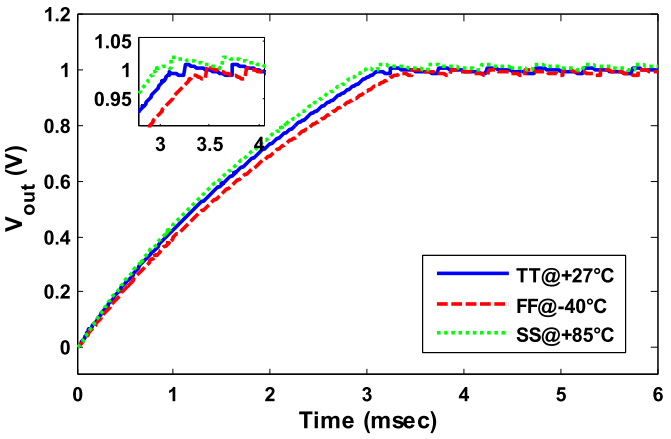


**Fig. 9.** Output voltage of the circuit in Fig. 6(a) in different process corner cases for $V_{out} = 1$ V.

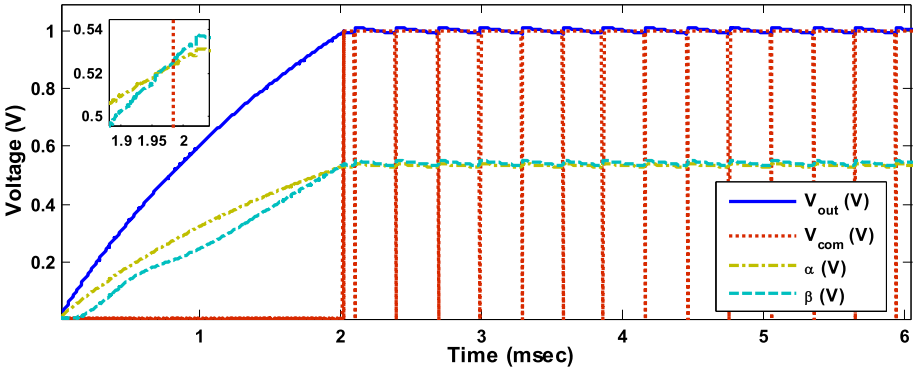


**Fig. 7.** Simulated output voltage of the proposed converter with an internally-set voltage reference in Fig. 6(a).

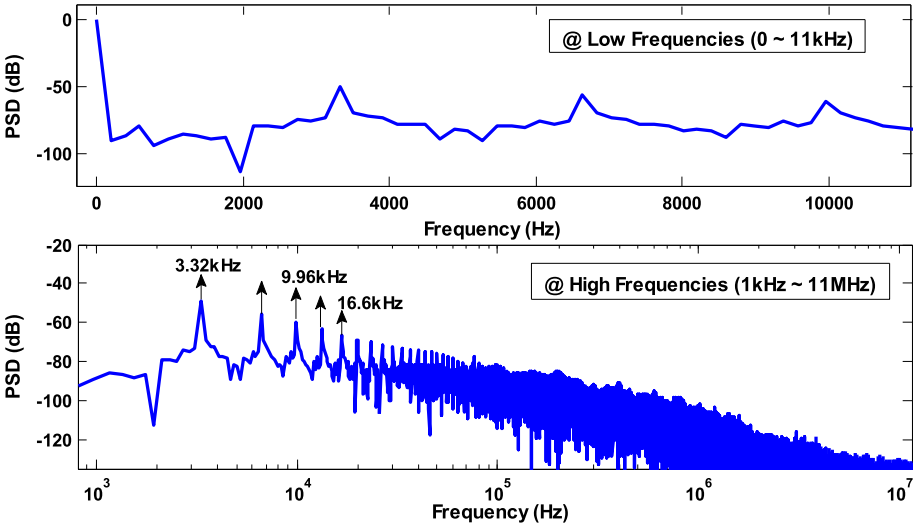


**Fig. 8.** Power spectral density of the output voltage in the proposed PCC.

The simulated output in different process corner cases and temperature variations is illustrated in Fig. 9. The maximum output voltage error is less than 18 mV in the worst case. Although the voltage reference is removed from PCC, the proposed converter with an internally-set voltage reference has a very good consistency against the process and temperature variations.

The simulated transient current of the inductor in $\varphi_r$ and $\varphi_f$ is shown in Fig. 10. The current in $\varphi_r$ follows equation (5) where a sinusoidal steady state current is summed with a transient current. In addition, as it is seen, the current of the inductor is discharged to $C_{out}$ in $\varphi_f$ and it reaches to zero at the end of this phase. The output voltage of the active rectifier ($V_{un}$) in different phases of operation is shown in Fig. 11. It could be seen that in $\varphi_r$, $V_{un}$ is decreased since $C_{un}$ is discharged to $L_s$. In this phase, $V_{un}$ reaches to its minimum value which is equal to the voltage drop over $V_{DS}$ of $M_{b1}$ and $M_{b3}$. In $\varphi_f$, $M_{b1}$, $M_{b5}$ and $M_{b6}$ are open and $V_{un}$ remains at the last value from the previous phase. When both of $\varphi_r$ and $\varphi_f$ are low, $C_{un}$ is charged through the rectifier and $V_{un}$ starts to increase.

A Monte-Carlo simulation is employed to evaluate the output voltage consistency of the proposed converter against the process variations and device mismatch. This simulation is performed in Cadence Spectre-RF environment using the mismatch models of TSMC 0.18 μm CMOS technology with 100 iterations. As seen in Fig. 12, the mean of the output voltage is 0.998 V. In addition, the standard deviation ($\sigma$) is about 3.34 mV, which confirms the robustness of the proposed converter against process variations and devices mismatch.

According to the measurement results in Ref. [15], here, it is assumed that the voltage amplitude of the received AC signal across the coil varies in the range of 3–7 V. The proposed PCC is simulated with different amplitudes of the input voltage level and the related efficiency is plotted in Fig. 13. The simulation results confirm a suitable degree of the efficiency robustness against the variations of the received voltage amplitude. For the input voltage in the range of 3–7 V, the maximum PCC efficiency variation is less than 2.6%, while the maximum power efficiency is 63.4%.

In order to verify the functionality of the proposed PCC, a proof-of-concept prototype was developed using off-chip components. To test the implemented PCC, some requirements including a power amplifier, power transmitter coil, and power receiver coil should be provided. Therefore, two single layer printed spiral coils (PSCs) as the power transmitter and receiver coils [16], and also a common class-E power amplifier [17] are implemented. In order to make the timing of the implemented PCC like the simulations in this section, the secondary coil is designed in a way that has self-inductance and series resistance equal to 2 μH and 0.5 Ω, respectively.

Fig. 14 shows the implemented prototype circuit. The primary and secondary coils are spaced and fixed in 1 cm distance from each other. In the test bench, the power transmitter is designed to deliver about 2 W power into the primary coil with 10 MHz frequency. This condition results in a 5 V peak-to-peak received voltage at the output of the secondary coil, which is the input of the rectifier. For simplicity, a passive rectifier is used in the implemented circuit to test the ideas. The required pulses for $\varphi_1$ and $\varphi_2$ are provided using an FPGA evaluation board with a 50 MHz on-board clock oscillator. Fig. 15 shows an oscilloscope screen shot of the output voltage of the PCC. Using a potentiometer, the resistors ratio in the control loop is set to provide 1 V output voltage.

The performance summary of the proposed buck-boost converter with an internally-set voltage reference in comparison with several other works is given in Table 1. It should be noted that the utilized rectifier in the proposed converter is taken from Ref. [13] and its efficiency is not included in Table 1. This is because in the other similar works, only the converter results have been reported. Thus in order to have a fair comparison, we have also investigated the efficiency of this part and the efficiency of the rectifier is excluded. Furthermore, it is worth mentioning that the proposed converter structure does not depend on the rectifier structure and it could be simply applied to the other active or passive rectifier topologies [8]. Although, the voltage reference block is removed

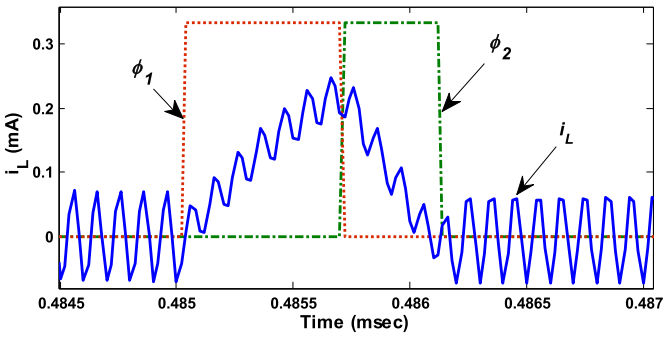


**Fig. 10.** Inductor current of the proposed converter in Fig. 2, in $\varphi_1$ and $\varphi_2$ phases.

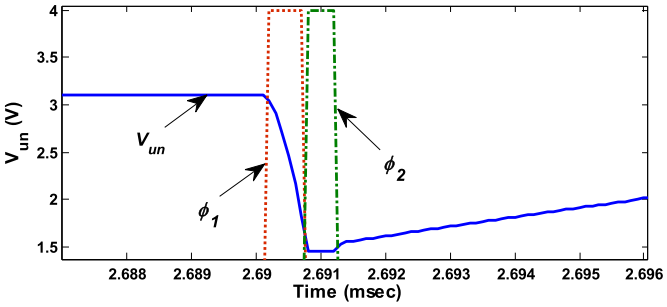


**Fig. 11.** Output voltage of the rectifier in Fig. 2, in $\varphi_1$ and $\varphi_2$ phases.

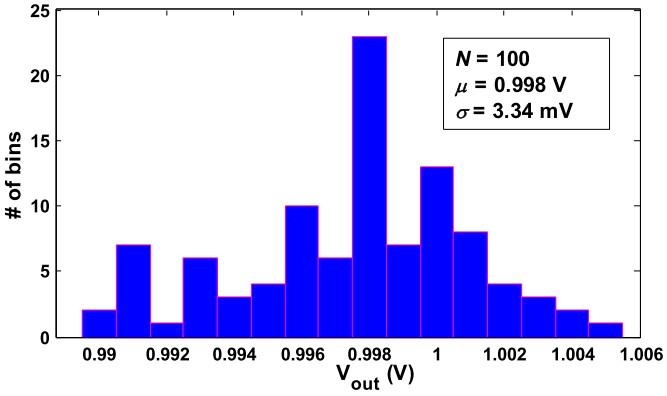


**Fig. 12.** Output voltage histogram of the circuit in Fig. 6(a) against process variations and mismatch of the switches.

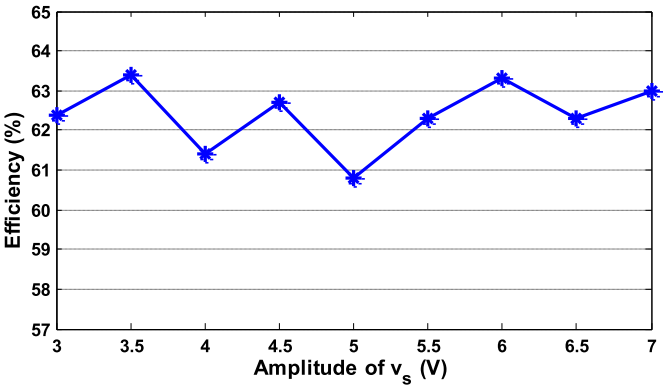


**Fig. 13.** Maximum power efficiency of the proposed PCC versus different input voltage amplitudes.

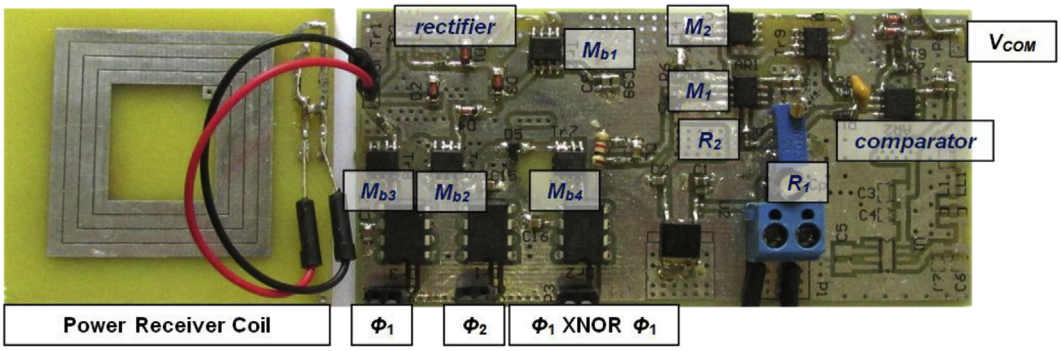


**Fig. 14.** The proof-of-concept prototype developed for experiments.

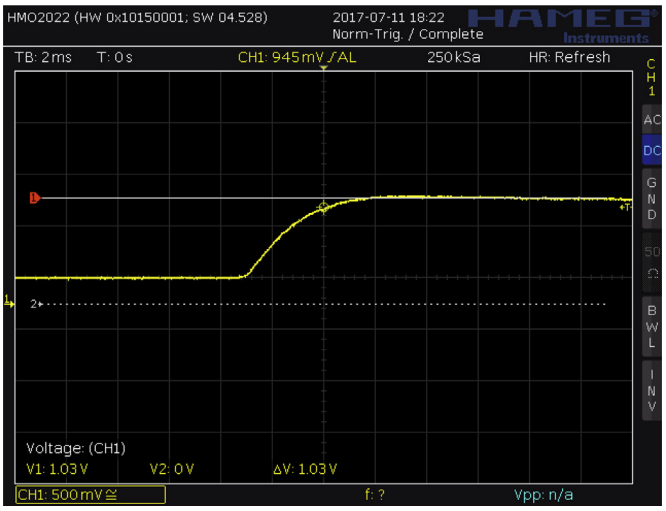


**Fig. 15.** Oscilloscope screen shot of the proof-of-concept prototype output voltage.

**Table 1**
Performance summary and comparison.

| Parameter | JSSC'15 [18] | TPE'13 [19] | NORCAS'15 [20] | This work[c] |
|---|---|---|---|---|
| CMOS process | 0.18 µm | 0.35 µm | 0.18 µm | 0.18 µm |
| Architecture | Buck-Boost | Buck-Boost | Buck-Boost | Buck-Boost |
| Voltage Reference | External | External | External | Self-Referenced |
| Input DC voltage[a] | 3 V | 2.5 V–5 V | 0.9 V–2.2 V | 1.5 V–4.5 V |
| Output DC voltage | 1 V, 1.8 V, 3 V | 3.3 V | 0.9 V–2.2 V | 0.6 V–2.5 V |
| Output current | 1 mW–10 mW[b] | 300 mA | 200 mA | 10 µA–2 mA |
| Inductor | 10 µH | 18 µH | 4.7 µH | 2 µH |
| Output capacitor | 10 µF | 47 µF | 10 µF | 10 µF |
| Switching frequency | 312.5 Hz | 500 kHz | 0.7 MHz–1.3 MHz | 200 kHz |
| Maximum efficiency | 83% | 65% | 75.6% | 80.4% |
| Line regulation | – | – | 0.05 V/V | 0.048 V/V |
| Load regulation | – | – | – | 0.027 V/V |
| Maximum ripple | – | – | ±5 mV | ±10 mV |

[a] After rectification.
[b] The output power is reported.
[c] Simulation results.

in the proposed inductor-reused buck-boost converter, its output voltage consistency against the temperature and process variations is comparable with other works. In addition, the proposed converter efficiency is almost independent of the input voltage amplitude making it suitable for inductively powered bio-implants.

## 5. Conclusions

In this paper, a new power conversion chain (PCC) comprised of a power receiver coil, a novel buck-boost converter and an active rectifier is presented. It is applicable for wireless power transferring through the inductive links. Avoiding the need for an extra circuitry to set the required voltage reference, the proposed PCC is benefited from an internally-set voltage reference. In addition, reusing the self-inductance of the coil resolves the need for a large off-chip inductor in the proposed buck-boost converter. Consequently, the power consumption, and also, the size of the implant are significantly reduced. Furthermore, to enhance the total efficiency, an active rectifier has been employed in the proposed PCC. According to the simulation results, the output voltage of PCC shows a good consistency against temperature and process variations and device mismatches. Besides, the efficiency of the proposed converter is almost independent of the received voltage amplitude. The simulation results and the experimental results of a proof-of-concept prototype demonstrate that the suggested PCC could be a proper alternative for the conventional PCCs in low-power wireless bio-implant applications.

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