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RESEARCH ARTICLE

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An adaptive continuous-time incremental ΣΔ ADC for neural recording implants

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Summary

In this paper, an analog-to-digital converter (ADC) with adaptive resolution is presented for wireless neural recording implants. The resolution of the ADC is changed according to the neural signal content, and for this purpose, a continuous-time (CT) incremental sigma-delta (IΣΔ) modulator is employed. The ADC digitizes the action potential (AP) and background noise (B-noise) with 8-bit and 3-bit resolutions, respectively. An automatic AP detector is used to separate the APs from the B-noise in order to select one of the two proportional resolutions. The power dissipation and output data rate of the ADC are reduced by using this technique. Analytical calculations and behavioral simulation results are provided to evaluate the performance of the proposed ADC. To further confirm its efficiency, the circuit-level implementation of the CT IΣΔ ADC is presented in Taiwan Semiconductor Manufacturing Company (TSMC) 90-nm complementary metal-oxide semiconductor (CMOS) process. According to the simulation results, the proposed ADC achieves 8-bit or 3-bit resolution adaptively with 10 kHz bandwidth while the average power consumption is less than 1.89 μW from a single 1-V power supply.

KEYWORDS

action potential detection, adaptive resolution, analog-to-digital converters, continuous-time incremental ΣΔ modulators, neural recording systems, root mean square, threshold level

1 | INTRODUCTION

Recently, wireless neural recording implants have been widely used to observe the simultaneous activity of many neurons in the brain.[1,2] These structures have multielectrode arrays, which are inserted into the cerebral cortex to observe the electrical activity of nearby nerve cells. The electrical activity of the neurons is named as the neural spike and/or the neural action potential (AP).[3] Nowadays, there is growing interest in the development of these systems especially increasing the number of recording channels. For neural recording systems with large number of channels, both low-power consumption and small-chip area are needed.[2] The analog-to-digital converter (ADC) is one of the key components at the front-end that its performance considerably affects the efficiency of the entire system. Typically, successive approximation register (SAR) ADCs with 8 to 10-bit resolution and 20 kS/s sampling rate are used in the wireless neural recording systems. The number of the utilized ADCs is equal to the number of recording channels[1] or several ADCs are shared between all channels to minimize the chip area.[3,4] However, the SAR ADC has stringent requirements in the reference buffer and front-end circuits resulting in more power consumption.[5]

Recently, the incremental sigma-delta (IΣΔ) ADC is utilized in the neural recording implants.[6,7] There is a one-to-one mapping between the input and output samples in IΣΔ ADCS because of the resetting in the modulator and decimation filter. Accordingly, IΣΔ ADCs can be well multiplexed between different channels without any memory effect. In addition, the distinct sample-and-hold (S/H) circuit can be removed by the modified IΣΔ ADC,[8] and therefore, a power hungry block is eliminated. Although most IΣΔ ADCs have been implemented as discrete-time (DT) circuits, continuous-time (CT) IΣΔ ADCs have been considered in recent years.[6,9] In CT ΣΔ ADCs, the required gain-bandwidth (GBW) of the operational amplifiers is less than the DT counterpart resulting in lower-power consumption. In addition, the DT IΣΔ ADC employs switched-capacitor integrators, and the linear realization of the switches is more difficult at low-supply voltage.

ADCs with a fixed resolution have been usually used in neural recording systems similar to the ADCs, which are mainly utilized in mixed-signal applications. The signal specification can be used to optimize the performance of the ADC in specific applications. Accordingly, so far, two methods have been proposed. In the first method, the nonuniform sampling is utilized in time domain where more information exists than elsewhere.[10,11] In the second method, a nonlinear quantizer is employed for signals that more information exists in the amplitude domain.[12]

As shown in Figure 1, the extracted neural signal of the electrode includes the background noise (B-noise) and APs. APs are used in the communication between different neurons. The number of the generated APs per second is named as the neural firing rate and the most information of the brain is encoded in neural communication, which is performed by APs. The neural recording implants record neural signals from many channels (electrodes). Each electrode typically senses the signal of multiple neurons (up to six neurons).[13] The subsequent signal processing must be able to differentiate the action potentials of different neurons. The waveform of action potentials is used to separate the received action potentials from different neurons by a single electrode.[13] Therefore, an ADC with high resolution (8-10 bit) is required to digitize the waveform of action potentials while an ADC with low resolution is sufficient for the B-noise.[12,13]

In several reported systems,[1-4,7] ADCs have 8 to 10 bit resolution, which have been designed based on the minimum required resolution for APs. The B-noise and APs are digitized with the same resolution whereas it is not necessary that the B-noise is to be digitized with higher resolution. Therefore, such ADCs have not been optimized in terms of the resolution and power consumption.

In this paper, an adaptive resolution ADC is proposed for neural recording implants, which composes of a CT IΣΔ ADC and an automatic AP detector. The proposed ADC has two resolution modes (3-bit and 8-bit) with an adaptive selection. The automatic AP detector distinguishes the AP from the B-noise in the neural signal to determine the resolution of the CT IΣΔ ADC. Based on the useful properties of the neural signal, by using the proposed adaptive CT IΣΔ, both the power consumption and data rate of the ADC are significantly reduced.

The rest of the paper is organized as follows. The proposed CT IΣΔ ADC is described in Section 2. The circuit-level implementation and simulation results of the proposed ADC are presented in Section 3, and finally, Section 4 concludes the paper.

2 | PROPOSED ADAPTIVE CT IΣΔ ADC

2.1 | Resolution and power scaling in IΣΔ ADCs

As illustrated in Figure 2, the IΣΔ ADC consists of a ΣΔ modulator and a decimation filter. When the reset pulse is high, the ΣΔ modulator quantizes the input signal, and the digital decimation filter concurrently processes the output bit stream of the modulator for oversampling ratio (OSR) clock cycles. oth the ΣΔ modulator and decimation filter (all

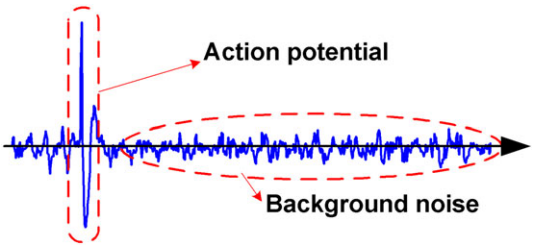

FIGURE 1 A typical neural signal [Colour figure can be viewed at wileyonlinelibrary.com]

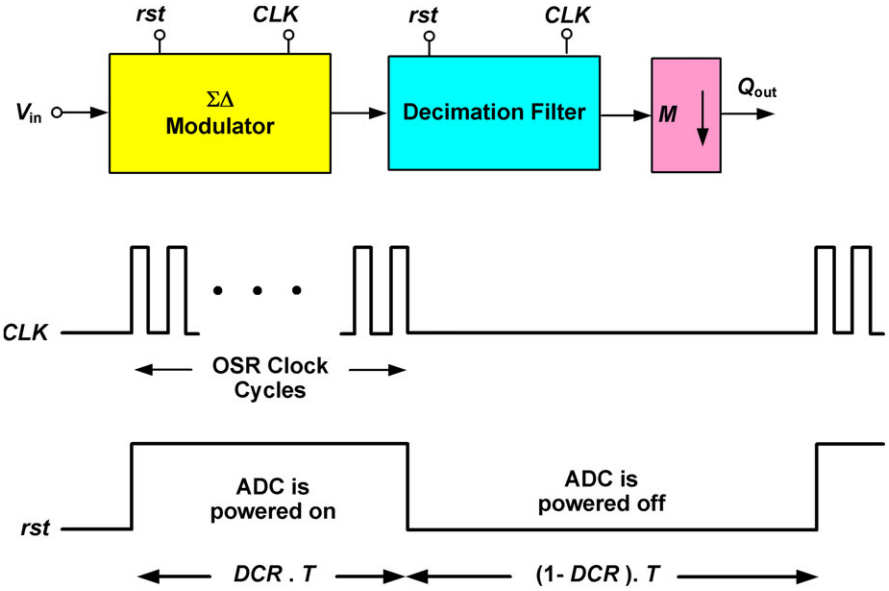

FIGURE 2 General block diagram of an incremental sigma-delta analog-to-digital converter [Colour figure can be viewed at wileyonlinelibrary.com]

memory elements) are reset when the reset pulse is low. The output of the decimation filter is downsampled after OSR clock cycles to provide a Nyquist rate output. The reset frequency is equal to the conversion rate of the ADC, and it is also proportional to the Nyquist rate. The relation between OSR and the duty cycle of the reset (DCR) pulse can be expressed as follows:

$$OSR = \frac{f_s}{f_{rst}} \times DCR, \tag{1}$$

where fs and $f$rst are the oversampling and reset frequencies, respectively. This equation shows that the OSR can be adjusted by DCR. The resolution of an IΣΔ ADC with an N-level quantizer and Lth-order loop filter is given by the following[8]:

$$n_{bit} = \log_2\left(\alpha(N-1)\frac{(\mathrm{OSR}+L-1)!}{L!(\mathrm{OSR}-1)!}+1\right), \tag{2}$$

where α is the quantizer overload level factor, and it is less than one. It is clear that the resolution is determined by OSR, and for a specific OSR, the value of DCR can be set based on relation (1).

Since the resolution of an IΣΔ ADC can be changed easily, it is utilized here. Furthermore, to power down the circuits of IΣΔ ADC is an effective way to save the power when the converter does not act (ie, when the reset pulse is low). Therefore, the power consumption has a transient manner as shown in Figure 2, and the average power consumption is given by the following:

$$\overline{P} = \frac{1}{T}\int_0^T P dt = \frac{1}{T}\left(\int_0^{DCR\times T} P dt + \int_{DCR\times T}^{T} P dt\right), = \frac{1}{T}[(1\times DCR\times T\times P)+(0\times T\times P)] = DCR\times P, \tag{3}$$

where T is the reset time period, and P is the power consumption of the IΣΔ ADC without any power down, and it is given by the following[14]:

$$P = P_{static} + P_{dynamic} + P_{digital} = k_1\, L + k_2 L.OSR + k_3\, OSR, \tag{4}$$

where P_{static}, P_{dynamic}, and P_{digital} are the static, dynamic, and digital powers of the ADC, respectively. In addition, k_1, k_2, and k_3 are fixed coefficients, which depend on the circuit specifications such as the number of current branches, supply voltage, etc. Relation (3) shows that a higher resolution results in more average power consumption and vice versa.

2.2 | Structure of the proposed ADC

In the proposed adaptive CT IΣΔ ADC, APs are digitized with high resolution, and the B-noise digitization is performed with low resolution. Figure 3 depicts the block diagram of the proposed adaptive CT IΣΔ ADC. It includes a CT IΣΔ ADC and the combination of an automatic AP detection and multiplexer to adjust the ADC's resolution. The neural signal is applied to the automatic AP detector with a single bit output, AP_{out}. In the automatic AP detector, the neural signal is compared with a predefined threshold voltage level to detect the APs. The threshold level is obtained by the calculation of the root mean square (RMS) value of the neural signal. When the neural signal becomes higher than the threshold level, an AP is detected, and AP_{out} is high. Then, the output of the AP detector is remained unchanged until 2 ms. This window time is similar to a typical AP duration plus the refractory period. The AP_{out} controls the 2:1 multiplexer where the inputs are high- and low-DCR pulses. If the neural signal content is the AP, the high DCR is applied to the adaptive CT IΣΔ ADC. Otherwise, the low DCR is applied. The high-DCR and low-DCR pulses determine two modes of ADC with 8-bit (high resolution) and 3-bit (low resolution), respectively.

The AP-firing rate is different in separate regions of the human brain whose maximum is 1.5 AP/second,[4,12,15] and the typical duration of the AP is 1 ms. Therefore, the average time of the B-noise presence in the neural signal is 99.85%, and the APs are only 0.15% of the time. According to the relation (3), the average power consumption is proportional to the DCR pulse, and it is determined by the ADC's resolution corresponding to the neural signal content. Based on the time percent coefficients of the B-noise and APs, and using the relation (3), the average power consumption is obtained as follows:

$$\overline{P} = 0.9985\ (DCR_L.P) + 0.0015(DCR_H.P) \approx DCR_L.P, \tag{5}$$

where DCR_L and DCR_H denote the low and high DCRs, respectively. This relation shows that the ADC power consumption is approximately equal to the low-resolution mode. Given that f_s and f_{rst} are fixed, by plugging DCR_L and DCR_H and their respective OSRs in (1), we can write

$$\frac{DCR_H}{DCR_L} = \frac{OSR_H}{OSR_L}, \tag{6}$$

where OSR_H and OSR_L denote the OSR in high- and low-resolution modes, respectively. DCR_H will be 25% if the ADC is time multiplexed among four channels. In this case, according to the relations (5) and (6), we have the following:

$$\overline{P} = \frac{0.25\ OSR_L}{OSR_H}.P. \tag{7}$$

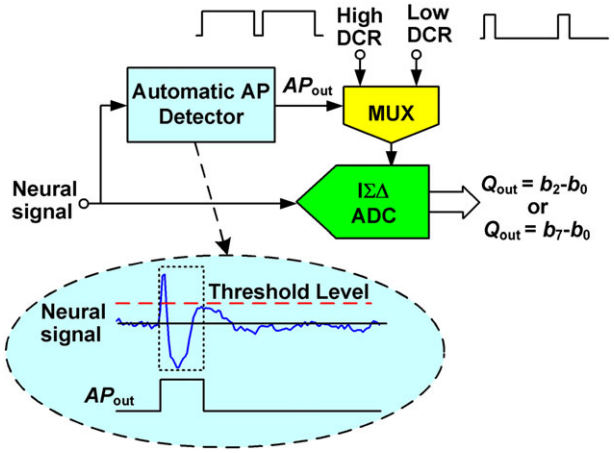

FIGURE 3 Proposed adaptive continuous-time incremental sigma-delta analog-to-digital converter [Colour figure can be viewed at wileyonlinelibrary.com]

Since the proposed ADC operates in two resolution modes, it is designed with high-resolution mode specifications to satisfy the low-resolution mode requirements as well. This means that OSR_H is utilized in relation (4). Therefore, from the relations (4) and (7), we have the following:

$$\overline{P} = \frac{0.25\ OSR_L}{OSR_H}(k_1\ L + k_2 L.OSR_H + k_3.OSR_H) = 0.25(\underbrace{\frac{OSR_L}{OSR_H}k_1\ LP_{static}} + \underbrace{k_2 L.OSR_{L\,P_{dynamic}}} + \underbrace{k_3.OSR_{L\,P_{digital}}}). \quad (8)$$

To select the order of the IΣΔ ADC, OSR_H and OSR_L for 3- and 8-bit resolutions are obtained from the relation (2), and then by placing them in the relation (8), three power terms including P_{static}, $P_{dynamic}$, and $P_{digital}$ are achieved. Table 1 shows P_{static}, $P_{dynamic}$, and $P_{digital}$ for the first-order to fourth-order IΣΔ ADC with a single-bit quantizer. Clearly that P_{static} and $P_{dynamic}$ increase with the order of the IΣΔ ADC, but $P_{digital}$ is decreased. Consequently, to minimize the average power consumption, $\overline{P}$, the second-order IΣΔ ADC is selected here.

Because of the presence ratio of the B-noise and APs in the neural signal, the adaptive IΣΔ ADC quantizes the neural signal with 3-bit in 99.85% and 8-bit in 0.15% of the time, respectively. Since the output data packet of the ADC should also carry the output of the AP detector, the ADC generates an average of 4.0075 bits per sample, and hence, there is approximately 50% data reduction in the proposed ADC compared with the conventional 8-bit ADC utilized in the neural recording systems. This data reduction reduces the power dissipation and area in different parts of the neural recording systems particularly in the wireless telemetry.

2.3 | System-level design of the proposed ADC

Two main sections of the proposed ADC are the CT IΣΔ ADC and automatic AP detector. Furthermore, the CT IΣΔ ADC consists of a CT IΣΔ modulator and a decimation filter. These sections are described in more details in the following.

2.3.1 | CT IΣΔ modulator

Figure 4 shows the utilized second-order CT IΣΔ modulator in the proposed adaptive ADC with a cascade of integrators feedback (CIFB) configuration. In this structure, a single-bit quantizer along with nonreturn to zero (NRZ) feedback digital-to-analog converters (DACs) are employed. Owing to the low-sampling frequency of the modulator, the excess loop delay (ELD) does not play a dominant role here.[16]

Generally, IΣΔ modulators are analyzed in time domain and the resolution is calculated by the output of the last integrator. The length of each conversion is M clock cycles (M is equal to the OSR). After M clock cycles, the comparator's input, V_x, is given by the folloing[17]:

$$V_x(M) = b_1\, c\frac{M(M-1)}{2}V_{in} - a_1 c V_{ref} \sum_{j=0}^{M-1}\sum_{i=0}^{j-1} d_{out}(i) - a_2\, V_{ref} \sum_{i=0}^{M-1} d_{out}(i), \quad (9)$$

where $d_{out}(i) = \pm 1$, and $V_x(M)$ is bounded by $\pm V_{ref}$ as follows:

TABLE 1 Different power consumption terms in an incremental sigma-delta analog-to-digital converter versus the order of the analog-to-digital converter

Order	P_{static}	$P_{dynamic}$	$P_{digital}$
1	$\frac{1.75}{257}k_1$	$1.75k_2$	$1.75k_3$
2	$\frac{1}{11}k_1$	$2k_2$	k_3
3	$\frac{2.25}{11}k_1$	$2.25k_2$	$0.75k_3$
4	$\frac{3}{8}k_1$	$3k_2$	$0.75k_3$

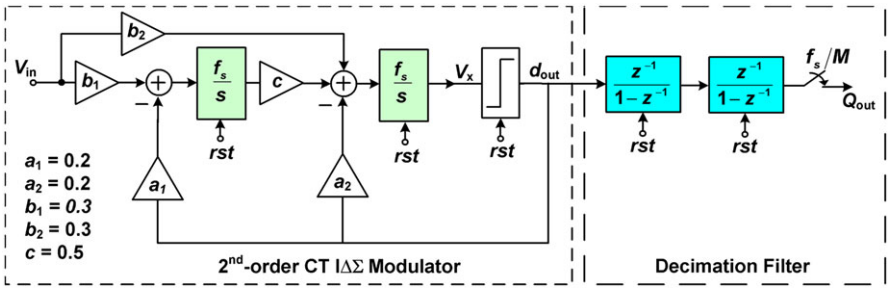

FIGURE 4 Block diagram of the second-order continuous-time incremental sigma-delta analog-to-digital converter [Colour figure can be viewed at wileyonlinelibrary.com]

$$-V_{ref} \le V_x(M) \le +V_{ref}. \tag{10}$$

This inequality is rearranged resulting in the following relation:

$$\frac{-2\,V_{ref}}{M(M-1)\,b_1 c} \le V_{in} - \frac{2}{M(M-1)\mathrm{b}_1} V_{ref}\left(a_1 \sum_{j=0}^{M-1}\sum_{i=0}^{j-1} d_{out}(i) - \frac{a_2}{c}\sum_{i=0}^{M-1} d_{out}(i)\right) \le \frac{2\,V_{ref}}{M(M-1)\,b_1\,c}. \tag{11}$$

By forcing the middle part of the above inequality to zero, the estimation of V_{in} is obtained as follows:

$$\widehat{V}_{in} = \frac{2}{M(M-1)\mathrm{b}_1}\, V_{ref}\left(a_1 \sum_{j=0}^{M-1}\sum_{i=0}^{j-1} d_{out}(i) - \frac{a_2}{c}\sum_{i=0}^{M-1} d_{out}(i)\right). \tag{12}$$

The quantization error is the difference between $\widehat{V}_{in}$and V_{in}. It is limited within$\pm(1/2)\,V_{LSB}$. According to (11), V_{LSB} can be expressed by the following:

$$V_{LSB} = \frac{4\,V_{ref}}{M(M-1)b_1 c}. \tag{13}$$

Therefore, the equivalent number of bits can be expressed as follows:

$$n_{bit} = \log_2\left(\frac{2V_{ref}}{V_{LSB}}\right) = \log_2\left(b_1 c\frac{M(M-1)}{2}\right) \approx 2\log_2(M) + \log_2(b_1 c) - 1. \tag{14}$$

According to the relation (14), the required resolution is determined with the value of M and the modulator coefficients b_1 and c. These coefficients are chosen to minimize M owing to the relation between M and the power consumption.

The CT IΣΔ ADC requires an S/H circuit at the input, which needs additional power consumption. The S/H circuit can be eliminated if the frequency response of the signal transfer function (STF) has an approximately unity amplitude at the signal bandwidth.[8] If the S/H is removed at front of the IΣΔ ADC, it results in a modified STF. To analyze this, an averaging filter, $G(z)$, is assumed at front of the modulator as shown in other study.[8] For a second-order IΣΔ ADC, it is given by the following:

$$G(z) = \frac{1 + 2z^{-1} + 3z^{-2} + \ldots + Mz^{-(M-1)}}{M.(M+1)/2}. \tag{15}$$

This relation shows a weighted average on the input signal similar to an S/H circuit. It is clear that the low attenuation at the edge of the signal bandwidth is obtained with a smaller value of M.

The noise transfer function (NTF) of the modulator is first generated in z-domain with the Schreier's Delta-Sigma Toolbox,[18] and the maximum NTF out-of-band gain is set to 1.2 to avoid instable modulator while having a single-bit DAC. The resulted coefficients for the modulator are scaled to minimize M. Figure 5 shows the frequency response of STF for the simulated second-order CT IΣΔ ADC with $M = 32$. As the vertical dotted line represented in Figure 5, the maximum in-band attenuation is 1.74 dB at the edge of the signal bandwidth, and as a result, the S/H circuit is

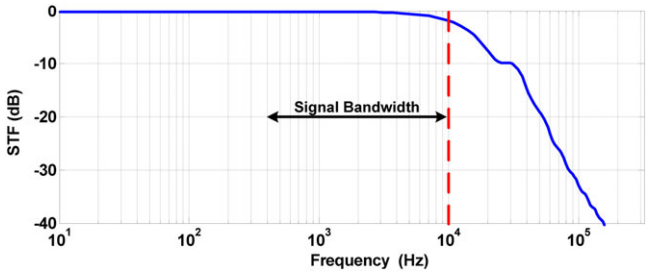

FIGURE 5 Signal transfer function of the second-order continuous-time incremental sigma-delta analog-to-digital converter [Colour figure can be viewed at wileyonlinelibrary.com]

eliminated. The synthesized NTF of the DT loop filter is then converted to the continuous time one, and the coefficients of CT loop filter are obtained as shown in Figure 4.

2.3.2 | Decimation filter

The simple implementation of the decimation filters is one of the advantages of IΣΔ ADCs. This filter can be optimized to minimize the ADC output noise (quantization and thermal noises) for a given value of M.[19] The output of the decimation filter is obtained from relation (12) where the input signal has been estimated. So, by substituting the modulator coefficients in relation (12), the output of the decimation filter is given by the following:

$$Q_{out} = \frac{2}{M(M-1)}\left(\sum_{j=0}^{M-1}\sum_{i=0}^{j-1} d_{out}(i) - \frac{3}{5}\sum_{i=0}^{M-1} d_{out}(i)\right). \tag{16}$$

Since the first term in relation (16) is the output of two cascaded integrators, and its value is much larger than the second term, the second term can be neglected for 8-bit resolution. As a result, a digital filter with the following transfer function is utilized as the decimation filter:

$$H(z) = \frac{z^{-2}}{(1-z^{-1})^2}. \tag{17}$$

As shown in Figure 4, the simplest way to implement this decimation filter is the cascade of two integrators.

2.3.3 | Effect of ELD and clock jitter in CT IΣΔ ADC

To verify the performance of the proposed CT IΣΔ ADC, some behavioral simulations have been performed in MATLAB/SIMULINK. As discussed earlier, the ELD does not cause instability in the modulator owing to its low-sampling frequency. The time delay of the loop, t_d, is given by the following[20]:

$$t_d \approx \frac{n_t \times f_s}{f_T}, \tag{18}$$

where f_T is the speed of the transistors, f_s is the oversampling frequency, and n_t is the number of series transistors in the feedback path. f_T and f_s are in the range of a few GHz and MHz, respectively. Since a few transistors are used as the switches in the feedback DAC, t_d can be less than 10% of the clock period, and the ELD will not affect the performance of the modulator.

Another nonideality, which can degrade the performance of the CT IΣΔ ADC is the clock jitter. The clock jitter restricts the maximum value of OSR in CT modulators with both NRZ and return-to-zero (RZ) DACs.[21] A random Gaussian noise with a variance of σ_j^2 is modeled as the clock jitter. The in-band-noise (IBN) due to the clock jitter in a CT IΣΔ modulator with an NRZ DAC is given by the following[16]:

$$INB_{\sigma_j}^{NRZ}[dB] \approx \frac{M}{M+1}10\log_{10}\left[\frac{(2.I_{DAC})^2\sigma_j^2 0.7}{T_s^2 \quad M}\right] + \frac{1}{M+1}10\log_{10}\left[\frac{0.5(I_{DAC})^2}{M}\right], \tag{19}$$

where $I_{DAC}$is the peak amplitude of the DAC pulse. Figure 6 shows the simulated signal-to-noise and distortion ratio (SNDR) degradation because of the clock jitter in high- and low-resolution modes. As it is seen, the amount of the clock jitter up to 0.001% of the clock period is acceptable with a slightly degradation in SNDR. Since the sampling frequency of the proposed ADC is in the range of a few MHz, the realization of the required clock with such amount of jitter is feasible on chip as well.

2.3.4 | Automatic AP detector

The automatic AP detector is based on the RMS value measurement of the neural signal to define the threshold voltage, V_{THR}. The neural signal is compared with V_{THR} to define the output of the AP detector. The RMS measurement of the neural signal should be frequently updated owing to the nonstationary nature of neural signals and their time variant statistical characteristics (eg, RMS value). The V_{THR} is usually set above the RMS value of the neural signal (V_{rms}) as follows:

$$V_{THR} = K \times V_{rms}, \tag{20}$$

where K is a constant, and its typical value is between 3 and 7.[22] The value of K affects the accuracy of AP detection, choosing a low value for K results in false AP detections and reduced energy efficiency. On the other hand, selecting a high value for K will prevent high-amplitude B-noise from being detected as the AP; however, the ADC will digitize low-amplitude APs with low resolution improperly.

The conversion rate of the simulated ADC is 25 kS/s, and hence, the time between two consecutive samples is 40 μs. So, the ADC digitizes 25 samples of the AP since its duration is about 1 ms. For more clarity, consider an AP waveform extracted from the real neural signal, which is shown in Figure 7 with different values of V_{THR}. For $K = 3$, the AP is detected in t_{a}, which is about 26 μs. In the worst case, suppose that the first sample is taken immediately after $t = 0$ where the AP is not detected yet. In this case, it is converted with 3-bit resolution, and all the next samples are digitized with 8-bit resolution because the AP is certainly detected after t_{a}. For $K = 7$, the AP is detected in t_{b}, which is about 50 μs. In this case, the first and second samples of the AP are digitized with 3-bit resolution. Therefore, with $3 \leq K \leq 7$, one and/or two samples between 25 samples of the AP are incorrectly digitized with 3-bit resolution. In the simulated ADC, the value of K is selected as 4.8 in order to correctly digitize more samples of the APs.

Figure 8 depicts the block diagram of the automatic AP detector. The serial two-level bit stream output of the modulator, d_{out}, with the sampling frequency of f_{s} is applied to control the embedded switch in the multiplying DAC (MDAC). Therefore, depending on the value of d_{out}, either V_{in} or $-V_{\mathrm{in}}$ is applied to the input of the variable gain amplifier (VGA). Actually, the MDAC operates as a multiplier. As a result, by considering the modulator output as $d_{out}(t) = V_{in}(t) + q_n$, the output of the MDAC, V_{i1}(t), is given by the following:

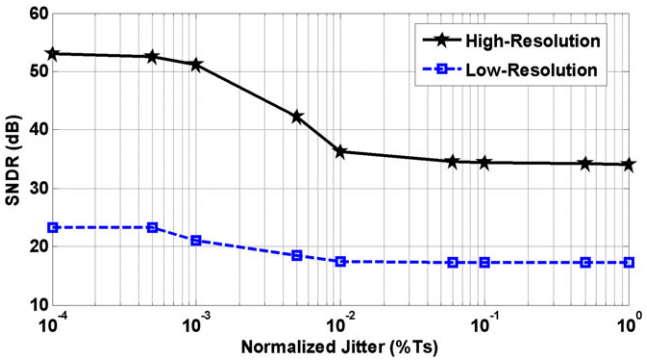

FIGURE 6 Simulated signal-to-noise and distortion ratio versus the clock jitter [Colour figure can be viewed at wileyonlinelibrary.com]

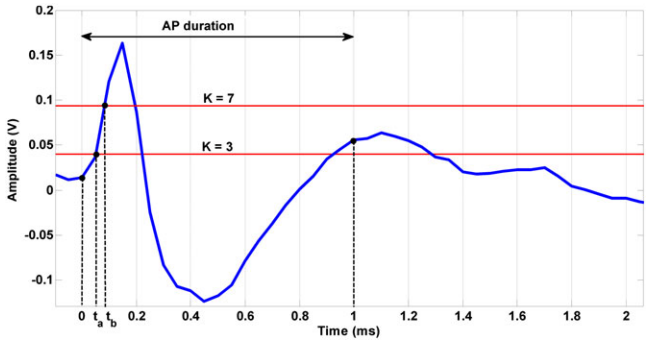

FIGURE 7 Waveform of a real action potential with two threshold levels [Colour figure can be viewed at wileyonlinelibrary.com]

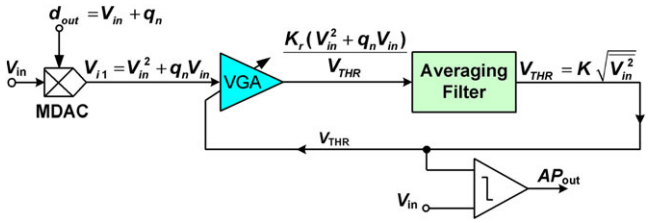

FIGURE 8 Proposed automatic action potential detector [Colour figure can be viewed at wileyonlinelibrary.com]

$$V_{i1}(t) = d_{out}(t) \times V_{in}(t) = V_{in}^2(t) + q_n \times V_{in}(t), \tag{21}$$

where q_n is the shaped quantization noise at the output of the modulator. Then, $V_{i1}(t)$ is applied to the input of the VGA with a gain of K_r/V_{THR}. By this gain, the VGA operates as a divider. The output of the VGA is filtered with the low-pass-averaging filter with a low-cutoff frequency. All high-frequency components due to the switching operation in the MDAC and also the shaped quantization noise of the modulator are suppressed by the averaging filter. Finally, the output of the averaging filter (which is a DC voltage) is used to control the gain of the VGA, and hence, the loop is closed. The output of the averaging filter is the threshold voltage, and it is given by the following:

$$V_{THR} = \sqrt{K_r \, \overline{V_{in}{}^2(t)}} = K\sqrt{\overline{V_{in}{}^2(t)}}\,. \tag{22}$$

This relation shows that V_{THR} is proportional to the RMS value of the input signal. As shown in Figure 8, a comparator is utilized to compare the input neural signal with V_{THR}. When the neural signal, $V_{in}(t)$, becomes larger than V_{THR}, the comparator output is high, and an AP is detected.

3 | CIRCUIT-LEVEL IMPLEMENTATION AND SIMULATION RESULTS OF THE PROPOSED ADC

The circuit-level realization of the proposed adaptive CT IΣΔ ADC is shown in Figure 9. It is simulated using TSMC 90-nm CMOS process with 1-V power supply. In these simulations, the Cadence Spectre-RF is utilized, and the post layout simulation results are provided. To evaluate the performance of the proposed ADC, transistor level simulations in different process corner cases and temperature variations are provided. The targeted neural signal bandwidth is 300 to 10 kHz, and it is digitized with an adaptive resolution (3 or 8-bit).

The modulator oversampling frequency (f_s) is 3.2 MHz. By this clock frequency, the simulated ADC can be time multiplexed among four channels. The frequency of the reset pulses (high and low DCRs) is 25 kHz, which is equal to the conversion rate of 25 kS/s, and it is slightly higher than the Nyquist rate. The duty cycle of the reset pulses (high and low DCRs) are 25% and 4.6%, which correspond to $OSR_H = 32$ and $OSR_L = 6$ for 8-bit and 3-bit resolutions, respectively. The second-order CIFB modulator is implemented using active-RC integrators. In the simulated modulator, the

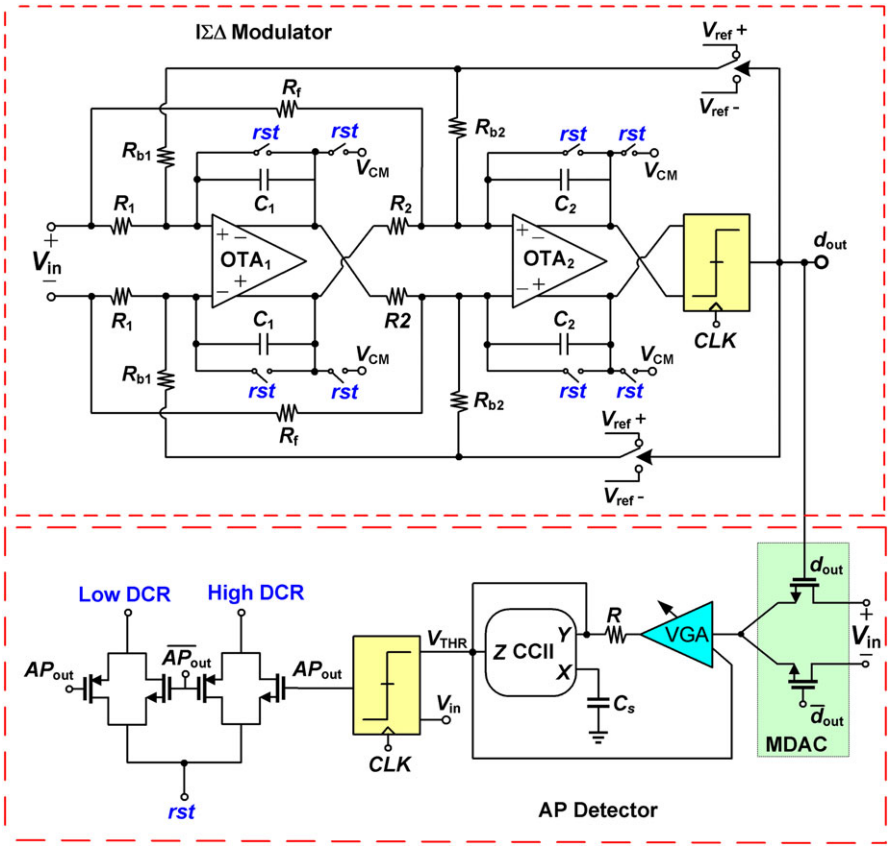

FIGURE 9 Circuit-level realization of the proposed adaptive continuous-time incremental sigma-delta analog-to-digital converter [Colour figure can be viewed at wileyonlinelibrary.com]

values of the passive devices are determined using the proposed power-efficient design method in other study.[14] In the modulator realization, the value of the resistors are selected according to the circuit noise considerations, and as possible as large resistors are utilized to reduce the power dissipation. Then, the value of the capacitors are determined to realize the desired coefficients of the modulator. Metal–insulator–metal (MIM) capacitors and polysilicon resistors are utilized in the realization of the proposed CT IΣΔ ADC, and the values of the designed passive devices are summarized in Table 2.

Because of the high-swing requirement in the single-bit second-order CT modulator, a fully differential two-stage Miller-compensated operational transconductance amplifier (OTA) is utilized in both integrators. Two separate OTAs with similar structure are designed to achieve the required specifications for the CT ΣΔ modulator. Figure 10 depicts the schematic of the simulated OTA as well as the common-mode feedback (CMFB) circuit. The devices sizes of the first OTA, which is used in the first integrator, are also shown in Figure 10. The specifications of the simulated OTAs are summarized in Table 3.

The comparator structure introduced in other study[23] is employed here to implement the required comparator. It is a cross-coupled latch with a fully differential preamplifier to reduce both the offset and kickback noise. It is worth mentioning that in the steady state, the latency of the proposed AP detector is mainly determined by the speed of the comparator, which is used to compare the neural input signal with the threshold level. The decision time of the simulated comparator is about 0.5 μs, and hence, it does not affect the proper operation of the proposed adaptive ADC.

TABLE 2 Simulated device parameters

Parameter	Value	Parameter	Value
R_1	625 kΩ	R	200 kΩ
R_2	250 kΩ	C_1	2.5 pF
R_{b1}	625 kΩ	C_2	2.5 pF
R_{b2}	408 kΩ	C_s	3 pF
R_f	408 kΩ		

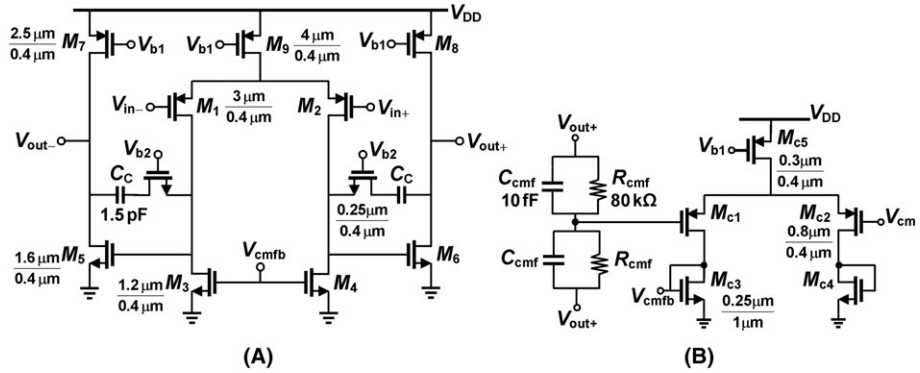

FIGURE 10 A, Simulated two-stage operational transconductance amplifier and B, common-mode feedback circuit

TABLE 3 Power and area breakdown of the simulated adaptive incremental sigma-delta analog-to-digital converter

			Value	
		Specification	OTA_1	OTA_2
CT IΣΔ ADC	CT IΣΔ modulator	Gain (dB)	51	47
		Unity gain BW (MHz)	4.6	4.9
		Phase margin (degree)	68	70
		Power dissipation (μW)	14.2	17.1
		Slew rate (V/μs)	2.11	2.27
	Decimation filter	Power dissipation (μW)	4.8	
		Area (mm^2)	0.0027	
AP detector	VGA	Power dissipation (μW)	1.83	
		K_r	23.04	
	Averaging filter	Cutoff frequency (Hz)	153	
		Power dissipation (μW)	1.2	
Adaptive CT IΣΔ ADC		Area (mm^2)	0.1267	
		Static power dissipation (μW)	39.6	
		Average power Dissipation (μW)	1.89	

Abbreviations: ADC, analog-to-digital converter; AP, action potential; CT, continuous-time; OTA, operational transconductance amplifier; VGA, variable gain amplifier.

The VGA circuit introduced in other study[24] is employed to implement the divider, and it is shown in Figure 11. The gain of the VGA is K_r/V_{THR} where V_{THR} is the output DC voltage of the AP detector, and K_r is a constant. K_r is defined by the aspect ratios of M_2, M_3, and M_5 transistors. The device parameters and bias currents in the simulated VGA are also illustrated in Figure 11. The specifications of the simulated VGA are summarized in Table 3.

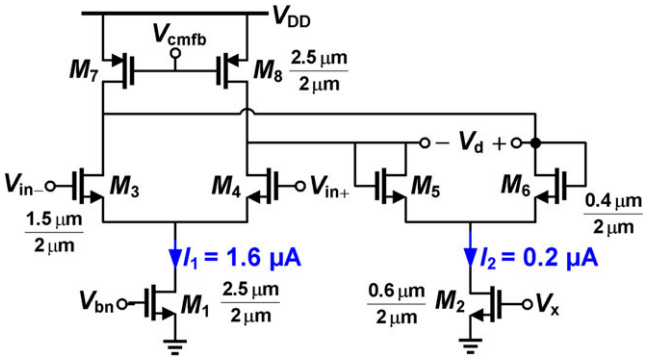

FIGURE 11 Circuit schematic of the simulated variable gain amplifier[24] [Colour figure can be viewed at wileyonlinelibrary.com]

The averaging low-pass filter has very low-cutoff frequency around 100 Hz. To implement this filter directly, large resistors and capacitors are needed. Here, a second generation current conveyor (CCII) based on the capacitance multiplier circuit, which is adopted from other study,[25] is used. As shown in Figure 12A, the utilized CCII has a low-impedance input (X), a high-impedance input (Y), and a high-impedance output (Z). The equivalent impedance seen from node Y to the ground, Z_{EQ}, is given by the following[25]:

$$Z_{EQ} = \left(\frac{r_x}{\alpha\beta} + \frac{1}{sC_S\alpha\beta}\right) \| r_z, \tag{23}$$

where r_x and r_z are the equivalent resistances at X and Z nodes, respectively, and α is the tracking error factor, which is about one. The current gain β is given by I_Z/I_X. In addition, the transfer function of the averaging filter is given by the following:

$$H(s) = \frac{r_z}{r_z + R + Rr_z sC_S\alpha\beta}, \tag{24}$$

According to the relation (24), the capacitor C_S is multiplied by a factor of $\alpha \times \beta$. Because of the low-power and wide-swing requirement in the averaging filter, a class-B CCII introduced in other study[26] is utilized in the CCII-based capacitance multiplier here. This circuit does not need any biasing circuit as shown in Figure 12B. The specifications of the simulated averaging filter are also summarized in Table 3.

The layout of the adaptive CT IΣΔ ADC without the decimation filter is illustrated in Figure 13, which occupies 554 μm × 225 μm active area. Usually, the decimation filter is realized in the succeeding digital section and/or digital processor in neural recording systems. Nevertheless, the decimation filter is synthesized here using the Synopsys Design Vision tool. Furthermore, the layout of the decimation filter is realized using the Cadence SoC Encounter, which occupies 57 μm × 48 μm silicon area. The post layout simulations have been performed, and the power consumption

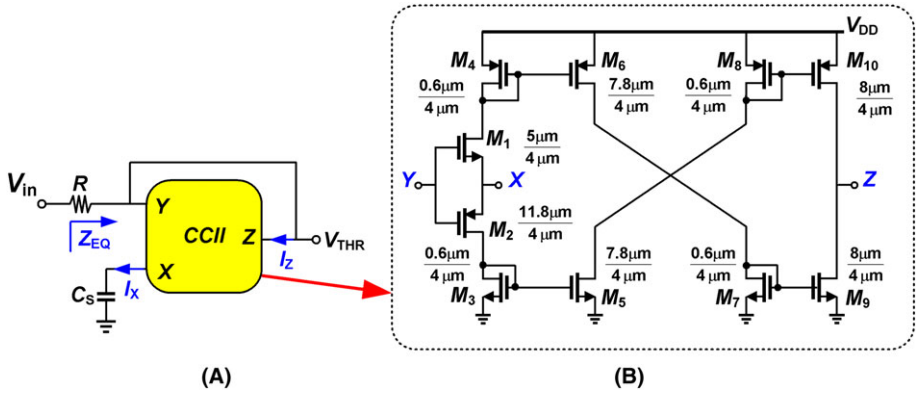

FIGURE 12 A, Simulated averaging filter[25] and B, second generation current conveyor circuit used in the averaging filter[26] [Colour figure can be viewed at wileyonlinelibrary.com]

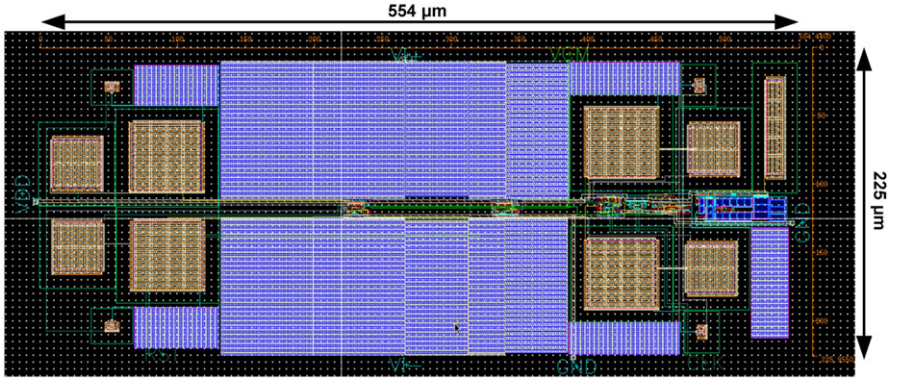

FIGURE 13 Layout of the simulated adaptive continuous-time incremental sigma-delta analog-to-digital converter [Colour figure can be viewed at wileyonlinelibrary.com]

of the decimation filter is estimated, which is about 4.8 μW. In addition, the simulations confirm the proper circuit operation and the estimated power consumption by the Design Vision.

The input-referred in-band RMS voltage noise of the simulated CT IΣΔ modulator and AP detector are about 178 and 4.2 μV_{rms}, respectively. The input-referred noise of the modulator does not affect the performance of the designed ADC considerably since it is much smaller than the LSB of the ADC, which is $V_{LSB} = 3.9$ mV. The amplitude of APs in a neural signal is around 100 to 500 μV, and it is amplified with 40 to 60 dB gain before the digitization. Therefore, the input-referred noise of the simulated AP detector is much smaller than the neural signal amplitude.

Figure 14 shows the dynamic range of the simulated ADC in different process corner cases and temperature variations when the ADC is in high-resolution mode. In these simulations, the circuit noise has been neglected. Excluding the circuit noise, in typical-typical (TT) process corner case, the achieved maximum SNDR is about 52.2 and 21.7 dB in high- and low-resolution modes, respectively. The output power spectral density (PSD) of the simulated ADC in both high- and low-resolution modes are shown in Figure 15. The achieved maximum SNDR is about 50.4 and 19.9 dB in high- and low-resolution modes while considering the circuit noise. By integrating the power of the circuit noise within the desired bandwidth, the maximum SNDR is decreased about 1.8 dB compared with the case that the circuit noise has been neglected.

Figure 16 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) errors of the simulated adaptive ADC. In high-resolution mode, the achieved maximum DNL and INL errors are +0.37/−0.24 LSB and + 0.24/−0.31 LSB, respectively. The maximum DNL and INL errors are obtained as +0.146/−0.097 LSB and + 0.048/−0.097 LSB, respectively, in low-resolution mode.

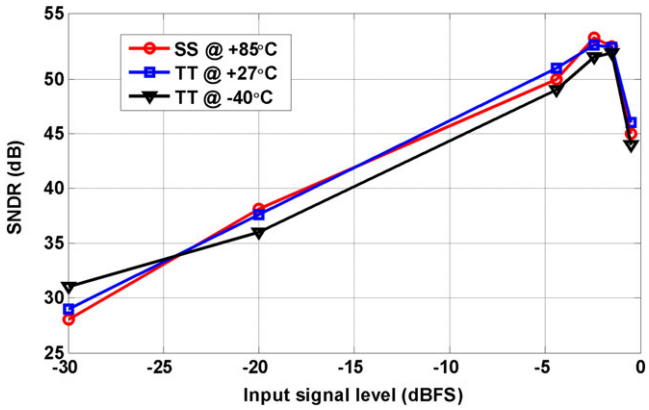

FIGURE 14 Simulated signal-to-noise and distortion ratio versus the input signal level in different process corner cases when the ADC is in high-resolution mode, and the circuit noise has been neglected [Colour figure can be viewed at wileyonlinelibrary.com]

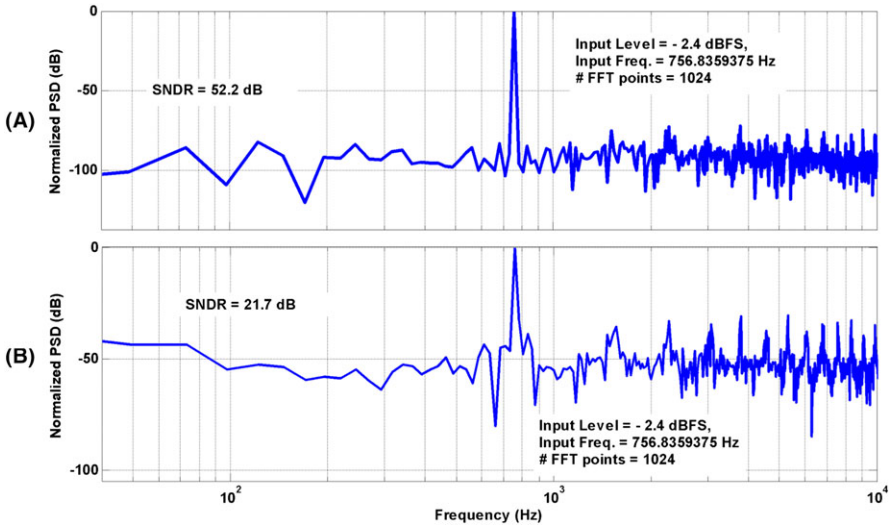

FIGURE 15 Simulated power spectral density of the adaptive continuous-time sigma-delta analog-to-digital converter in A, high- and B, low-resolution modes excluding the circuit noise [Colour figure can be viewed at wileyonlinelibrary.com]

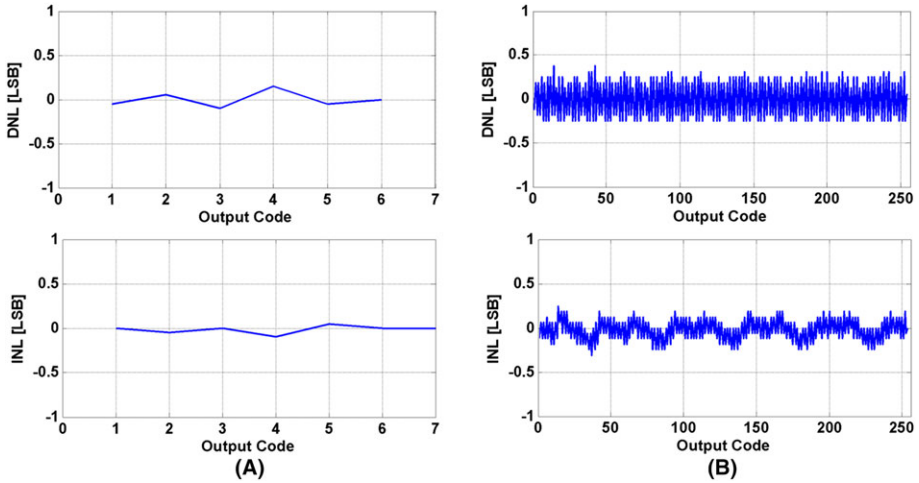

FIGURE 16 Simulated differential nonlinearity and integral nonlinearity errors of the adaptive continuous-time sigma-delta analog-to-digital converter in A, low- and B, high-resolution modes [Colour figure can be viewed at wileyonlinelibrary.com]

The average power consumption of the simulated ADC including the decimation filter is about 1.89 μW while the total static power dissipation is about 39.6 μW. The average power consumption is reported here since the neural signal is nonstationary. It has been calculated by averaging the power consumption in different window times.[27] When the adaptive ADC operates only in high-resolution (8-bit) mode, it has the highest-power dissipation. In this case, the simulated power consumption per channel is about 10 μW since the ADC has been designed to record four different neural channels by time multiplexing, and it is turned off in 75% of the time. On the other hand, when the simulated ADC only works in low-resolution (3-bit) mode, it has the lowest-power consumption. In this case, the power dissipation per channel is about 1.85 μW, which is near the average power consumption when the ADC is used to digitize a real neural signal. The power dissipation of different parts of the simulated ADC is summarized in Table 3.

To evaluate the performance of the proposed ADC, a real prerecorded neural signal is utilized. This signal has been intracortically recorded from the auditory cortex of a guinea pig as it has been mentioned in the previous study.[1] It is worth mentioning that this previously recorded neural signal has the same average number of APs as in other study.[15] Figure 17 shows the simulated transient response of the adaptive ADC. Figure 17A depicts the previously recorded neural signal. The output of the automatic AP detector is illustrated in Figure 17B. The output of the adaptive CT

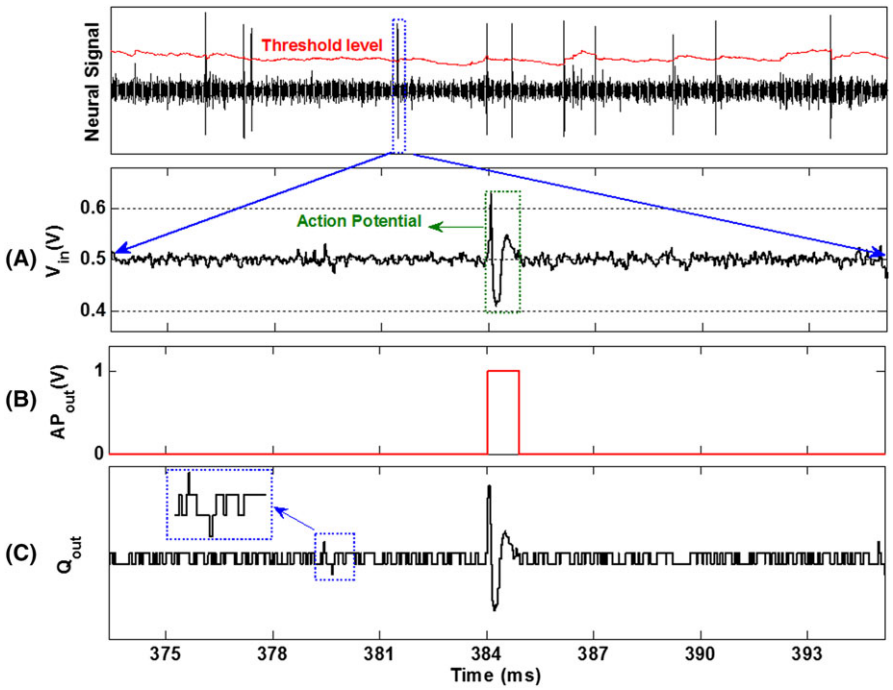

FIGURE 17 Simulated transient response of the proposed analog-to-digital converter with a neural input signal: A, neural input signal, B, output of the action potential detector, and C, output of the analog-to-digital converter, Q_{out} [Colour figure can be viewed at wileyonlinelibrary.com]

IΣΔ ADC is shown in Figure 17C. As it is seen, the APs are well detected, and the ADC is adaptively switched between 3-bit and 8-bit resolution modes. Hence, the AP and B-noise are correctly digitized with different resolutions.

The proposed adaptive IΣΔ ADC quantizes the neural signal with 3-bit in most of the times. Therefore, a large-data reduction is obtained here. Since the output data packet of the ADC should also carry the output of the AP detector, the ADC generates an average of 4.0075 bits per sample. This data reduction reduces the power dissipation and area in succeeding parts of the neural recording implants, particularly in the wireless telemetry systems.

Table 4 compares the simulated performance of the proposed adaptive ADC with some recently reported ADCs for biomedical applications. Generally, the ADCs used in the neural recording systems have 8 to 10-bit resolution. Both the introduced ADC in the previous study[12] and the simulated ADC here have 8-bit resolution. In that study,[12] a nonlinear SAR ADC is used by adjusting the quantization levels with an exponential function, and more quantization levels are assigned for digitization of the APs. The ADC resolution in that study[12] is always 8-bit, and its 5-LSB bits are zero at most of the time. As a result, this ADC can be used to reduce the output data rate with an additional digital circuit. So, there is not any ADC power saving in the previous study,[12] but the reduction of the output data rate results in some power saving in the succeeding stages of the neural recording system. Moreover, in this neural recording system, a high-precision VGA is always needed to provide a full-scale input for the ADC. In contrast, the proposed ADC reduces the power consumption in both ADC and the following stages. This is achieved by changing the ADC resolution and reducing the output data rate simultaneously. The output of the AP detector can be simply used in the data rate reduction in the following stages without needing any additional circuit.

The SAR ADC has stringent requirements in the reference buffer and front-end circuits resulting in more power consumption. In addition, the LSB-first SAR ADC uses its previous sample as an initial guess for the current sample.[28] For a full-scale input signal such as APs, the LSB-first SAR ADC will require more conversion steps than the conventional SAR ADC.[29] The performance of such ADCs highly depends on the input signal amplitude. The amplitude of the neural signal (APs and the B-noise) varies among different channels in the multielectrode neural recording systems. These variations are mainly due to the random distance between different electrodes and the corresponding neurons. Therefore, a VGA with high-precision gain is needed to provide a full-scale input signal for the LSB-first SAR ADC. Finally, the reasonable figure of merit (FoM) of the proposed ADC confirms its performance as a good candidate for wireless neural recording implants.

TABLE 4 Performance summary and comparison

	TCASI'15 [6]	TBCAS'14 [12]	TBCAS'14 [13]	JSSC'14 [28]	TCASII'16 [29]	VLSI'16 [+++] 30	CTA'11 [+++] [31]	This work*
Application	Biomedical	Neural	Neural	Biomedical	Neural	Biomedical	Neural	Neural
Architecture	CT IADC	SAR (nonlinear)	SAR	SAR	SAR (dual rate)	IADC	Cyclical ADC	CT IADC
CMOS process	0.18 μm	0.18 μm	90 nm	0.18 μm	0.18 μm	90 nm	90 nm	90 nm
V_{DD} (V)	1.2/1.8	1.8	1.2	0.5	1	20	1.2	1
Peak SNDR (dB)	75.9	64.1	69.38	59	45.8	85.3	69.38	50.4/19.9
Sampling rate (kS/s)	8	25	100	4	20/2	2	100	25
Bandwidth (kHz)	0.25	10	10	2	10/1	0.976	10	10
Power	2.175 μW	87.2 μW [+]	5 μW	31 nW	151 nW	8.6 μW	5 μW	1.89 μW**
Area (mm^2)	0.337	0.036	0.1	0.12	0.12	-	0.07	0.1273
FoM (fJ/conv.Step)[+] [+]	850	3340	322	17	487	290	322	345

Abbreviations: ADC, analog-to-digital converter; CT, continuous-time; SAR, successive approximation register; SNDR, signal-to-noise and distortion ratio.

[+]Including reference circuit.

[++]FoM = Power/(2*BW*2^{ENOB}).

[+++]Simulation results.

*Post layout simulation results.

**Including decimation filter.

4 | CONCLUSIONS

In this paper, an adaptive CT IΣΔ ADC is proposed to digitize neural signals in wireless neural recording implants. The ADC has 8-bit and 3-bit resolutions for APs and B-noise, respectively, which is adaptively selected by detecting APs in a neural signal. An automatic AP detector is presented to detect the APs. To reduce the power consumption, both the AP detector and ADC utilize the ΣΔ modulator simultaneously, and the former uses it to realize a multiplier. The output data rate of the proposed ADC and its average power dissipation are significantly reduced since the ADC operates in low-resolution mode at most of the time. The effectiveness of the proposed adaptive CT IΣΔ ADC has been confirmed with system and circuit levels simulation results.

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