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A power efficient buck-boost converter by reusing the coil inductor for wireless bio-implants

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SUMMARY

In this paper, a buck-boost converter circuit for wireless power transfer via inductive links in bio-implantable systems is presented. The idea is based on reusing the power receiver coil to design a regulator. This method employs five switches to utilize the coil inductor in a frequency other than the power-receiving signal frequency. Reusing the coil inductor decreases the on-chip regulator area and makes it suitable for bio-implants. Furthermore, in the proposed technique, the regulator efficiency becomes almost independent of the coil receiving voltage amplitude. The proposed concept is employed in a buck-boost regulator, and simulation results are provided. For a 10 MHz received signal with the amplitude variation within 3 ~ 6 V and with the converter switching rate of 200 kHz, the achieved maximum efficiency is 78%. The proposed regulator can also deliver 10 μA to 4 mA to its load while its output voltage varies from 0.6 to 2.3 V. Simulations of the proposed converter are performed in Cadence-Spectre using TSMC 0.18 μm CMOS technology. Copyright © 2017 John Wiley & Sons, Ltd.

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KEY WORDS: buck-boost converters; AC to DC converters; voltage regulators; CMOS full-wave rectifiers; bio-implants; inductive power link

1. INTRODUCTION

Inductive links for power transmission to implantable medical devices (IMDs) have been extensively used in animal cases and have potential to widely spread over the human targets. Some well-known applications for IMDs are cochlear implants [1], visual prosthesis [2], and invasive wireless neural recording [3].

Power consumption and the chip area are two imperative issues that should be addressed in the design of IMDs and in some cases are the bottlenecks of the technology [3, 4]. As shown in Figure 1, the received AC power from the inductive link should be converted to DC power. Furthermore, it should be regulated at a certain level so that it can be applied as a supply voltage for other parts of the implant. For this to be realized, several solutions have been already reported. The traditional alternative is to employ a linear regulator at the rectifier output [5, 6]. The variation of the regulator input voltage level is the main problem in this method. This may increase the voltage drop over the regulator, and, as a result, the efficiency of the regulator is decreased. In inductive links, the regulator input voltage level can be significantly deviated from its specified level due to the variation of the received signal. It should be noted that the variation of the received signal accounts for several reasons such as the variation in distance or angle between the power transmitting and receiving coils and also because of the wetness of the path between these two coils.

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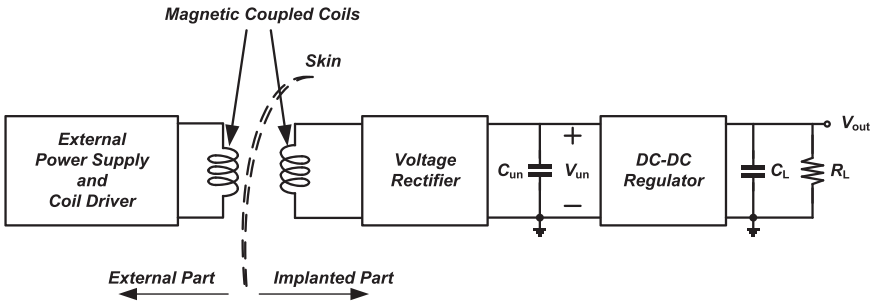

Figure 1. Power conversion structure in bio-implant systems.

In [7, 8], AC to DC boost converters with the switching frequency of 2 ~ 100 times higher than the frequency of the input power signal are proposed. In these techniques, although the required DC voltage is successfully achieved, however, the high switching rate decreases the efficiency of the regulator because of the large power dissipation on their power switches.

Nonlinear regulators such as buck-boost converters can also be the solution for the mentioned problem. They can provide wide range of the output currents without the instability concerns [9, 10]. Furthermore, they can have several output voltages with different levels [11]. Despite these superiorities, the frequently used large off-chip inductor in the conventional buck-boost converters can be troublesome. As a clarification, it is worth mentioning that this inductor is usually in the range of μH [4].

In this paper, a new method is developed in order to take advantages from the buck-boost converter while the need of its inherent large inductor is resolved. As it is known, a large off-chip coil is usually available in the power-receiving part of the wireless bio-implants. The proposed idea is to reuse this coil in a different frequency as the inherent inductor in a buck-boost converter. In other words, in the proposed regulator, the power-receiving coil is utilized in two different power receiving and regulator switching frequencies. This way, the buck-boost inherent off-chip inductor is avoided. The proposed regulator not only improves the efficiency but also makes the efficiency to be almost independent of the received power signal amplitude. Furthermore, the proposed regulator is capable of producing DC voltages at levels higher or lower than the received voltage. The power consumption of some applications such as the invasive wireless neural recording sensors is in the order of tens of μW [12] to more than hundreds of mW [3]. In addition, because these sensors are implanted under the skin to record the action potential of the brain, their size should be as small as possible. Furthermore, the heat of the sensor could be harmful for the adjacent cells. Therefore, in modern invasive wireless neural recording systems, the sensor size and power consumption are the main design issues. Inherent capability of the switching regulators to produce a wide range of current makes the proposed idea suitable for this kind of applications. As the inductor of the power receiver coil is reused in the proposed converter, the size is significantly decreased. Furthermore, the high efficiency of the proposed regulator alleviates the power consumption issue.

The rest of the paper is organized as follows. In Section 2, the theory and operation of the proposed converter are presented. Several circuit level simulation results of the proposed converter are provided in Section 3. Finally, the conclusions are given in Section 4.

2. PROPOSED CONVERTER ARCHITECTURE AND OPERATION

2.1. Basic configuration of the conventional buck-boost converter

The basic configuration of a buck-boost converter is shown in Figure 2 [13]. This circuit works in two phases notated as ϕ_1 and ϕ_2. When ϕ_1 is high, switches S_1 and S_3 are closed while S_2 and S_4 are open. As a result, the inductor is charged with a linear current as it is stated in (1). The charging interval of the inductor is regarded as t_{rise}.

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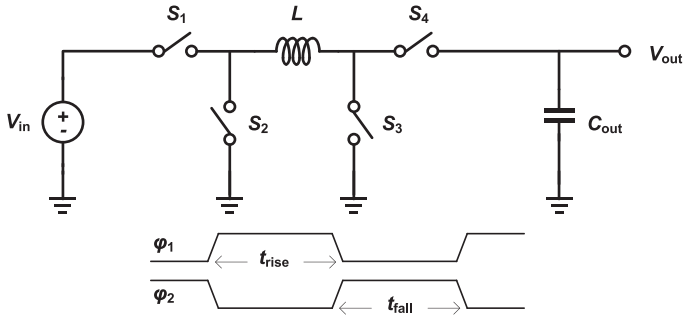

Figure 2. Basic configuration of an ideal buck-boost converter.

$$\phi_1 : V_{\text{in}} = L\frac{di_{\text{L}}(t)}{d(t)}, \quad 0 \le t < t_{\text{rise}} \tag{1}$$

where $i_{\text{L}}(t)$ is the current of the inductor and V_{in} is the input DC voltage. During the phase ϕ_2, S_2 and S_4 are closed, and S_1 and S_3 are open, and the current of the inductor is discharged to C_{out}. The discharging time is named as t_{fall} because the current of the inductor falls down to zero within this interval. The output voltage, V_{out}, according to $i_{\text{L}}(t)$ can be calculated in phase ϕ_2 as follows:

$$\phi_2 : L\frac{di_{\text{L}}(t)}{d(t)} = -V_{\text{out}}, \quad t_{\text{rise}} \le t \le (t_{\text{rise}} + t_{\text{fall}}) \tag{2}$$

One may integrate (1) and (2) over their time limits. The current $i_{\text{L}}(t_{\text{rise}})$ is regarded as an initial condition for (2). Thus, neglecting the probable ripple at the converter output and assuming it as a DC voltage [13], V_{out} can be obtained as follows:

$$V_{\text{out}} = \frac{t_{\text{rise}}}{t_{\text{fall}}} V_{\text{in}} \tag{3}$$

Relation (3) shows that V_{out} can be higher or lower than V_{in}, depending on the values of t_{rise} and t_{fall}.

2.2. Proposed inductor-reused buck-boost converter

The proposed inductor-reused buck-boost converter is shown in Figure 3. Here, the off-chip power-receiving coil is represented by L_{s}, R_{s}, and V_{s} according to the simplified model introduced in [14]. In this model, L_{s} and R_{s} are self-inductance, and series resistance of the IMD's coil and V_{s} is a sinusoidal voltage source, which is induced by an outer coil. The frequency of V_{s} is considered to be f_1. L_{s} is a large off-chip inductor. So it can be a proper alternative to be reused in order to realize a buck-boost converter. To reach this goal, the timing in conventional buck-boost converters from two phases, ϕ_1 and ϕ_2 in Figure 2, should be changed into three phases. In the first phase, the power from the coil is received, and then it is stored in a capacitor located at the output of the rectifier. Two other phases are utilized in the buck-boost operation to convert the initial voltage of the capacitor to a desirable DC voltage level. This way, the coil is reused in two different timing intervals notated as the power-receiving phase and buck-boost operation, respectively. The only difference of the proposed buck-boost operation phase with the conventional buck-boost converters is that unlike the DC voltage source, the initial voltage of the capacitor should be applied as the input of the proposed converter.

In Figure 3, ϕ_1 and ϕ_2 are connected to ϕ_{r} and ϕ_{f} terminals, respectively. In the next section, it will be seen that ϕ_2 will be the input of the control unit, and the output of the control unit will be connected to ϕ_{f} terminal. The utilized full-wave passive rectifier is composed of the M_1-M_4 transistors [12]. According to ϕ_1 and ϕ_2, the proposed inductor-reused buck-boost converter has three phases of the

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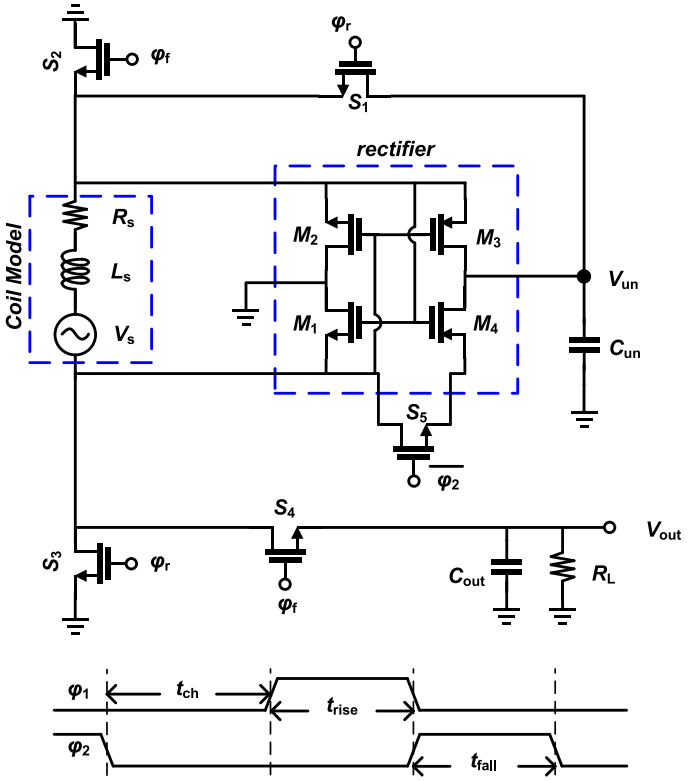

Figure 3. Proposed inductor-reused buck-boost converter. [Colour figure can be viewed at wileyonlinelibrary.com]

operation. During the first phase, the level of ϕ_1 and ϕ_2 is low, and thus, S_1–S_4 switches are open, and switch S_5 is closed. In this phase, the rectifier charges C_{un} to its maximum value, which is equal to the V_s amplitude, as shown in Figure 4. The pulse repetition frequency of ϕ_1 and ϕ_2 in Figure 3 should be much lower than f_1 to give enough time to the capacitor to be charged by V_s. In other words, it takes several periods for V_s to charge C_{un} to its maximum value, depending on the value of C_{un} and amplitude of V_s. So the period of ϕ_1 and ϕ_2 should be larger than the period of V_s. In the second phase, S_1 and S_3 switches are closed, and the energy stored in C_{un} is discharged to L_s, as shown in Figure 5. This phase is equivalent to ϕ_1 in conventional buck-boost converters, described in Section 2.1. During the last phase, $S_{1,3,5}$ switches are open, and $S_{2,4}$ switches are closed. Consequently, L_s delivers its energy to C_{out} in order to drive the load as it is depicted in Figure 6.

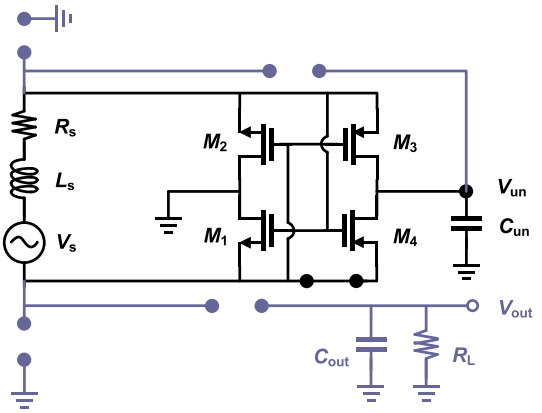

Figure 4. Proposed inductor-reused buck-boost converter in t_{ch}. [Colour figure can be viewed at wileyonlinelibrary.com]

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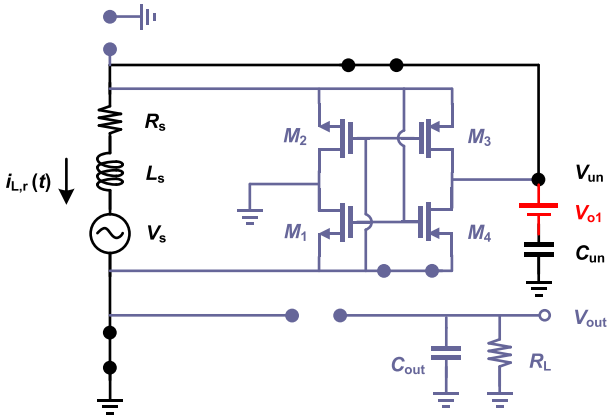

Figure 5. Proposed inductor-reused buck-boost converter in t_{rise}. [Colour figure can be viewed at wileyonlinelibrary.com]

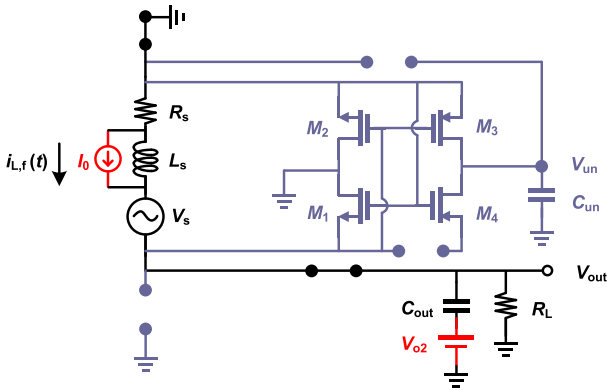

Figure 6. Proposed inductor-reused buck-boost converter in t_{fall}. [Colour figure can be viewed at wileyonlinelibrary.com]

This phase is completely like ϕ_2 in conventional buck-boost converters. In the following, these three phases are explained in details.

2.2.1. Charging phase (Φ_{ch}). In this phase, S_1–S_4 switches are open, switch S_5 is closed, and C_{un} is charged by V_s through M_1–M_4 transistors as it is shown in Figure 4. This phase lasts until the DC voltage of C_{un} reaches to its maximum value, which is the amplitude of V_s. This voltage will be used as the initial voltage for C_{un} at the start of the next phase. Also, at the end of this phase, C_{un} is fully charged and thus pulls no more current. Therefore, the current of the inductor is zero. This value will be regarded as an initial condition at the start of the next phase.

2.2.2. Inductor's current rising phase (Φ_{rise}). At this phase and the next phase, the circuit in Figure 3 should be worked as a buck-boost converter. Therefore, the rectifier transistors are off in this phase. The equivalent circuit of the proposed converter in this phase is shown in Figure 5. As it is seen, V_{DS} of both M_1 and M_3 transistors is equal to zero. In addition, because the drain and source of M_2 and M_4 transistors are exchanged, their V_{GS} is zero. This way, $M_{3,4}$ transistors are excluded from the rest of the circuit, and $M_{2,4}$ transistors are off during Φ_{rise}. The initial voltage of C_{un} at the start of this phase is determined by the amplitude of V_s, which is shown by V_{o1}. Furthermore, because C_{un} is already pre-charged up to its maximum level, the initial condition of the inductor at the start of Φ_{rise} is zero. However, during Φ_{rise}, the current of the inductor is gradually increased owing to the discharging phenomenon of C_{un} in the shown RLC loop.

At the end of this phase, the current of the inductor is needed to determine the initial condition in the next phase. The analysis of the RLC loop in this phase can be carried out taking into account the two

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separate voltage sources specified as V_s and V_{o1}. Applying the superposition theorem, the steady state and transient time analysis are performed on the RLC circuit regarding to the V_s and V_{o1}, respectively. This way, the current of the inductor owing to the voltage source V_s is given by the following:

$$I_{s,r}(j\omega) = \frac{1}{R_s + j\left(L_s\omega - \frac{1}{C_{un}\omega}\right)} V_s(j\omega) \tag{4}$$

The magnitude of $I_{s,r}(j\omega)$ can be determined as follows:

$$\left|I_{s,r}(j\omega)\right| = \frac{1}{\sqrt{{R_s}^2 + \left(L_s\omega - \frac{1}{C_{un}\omega}\right)^2}} |V_s(j\omega)| \tag{5}$$

The second term of the inductor current denoted as $i_{t,r}(t)$, which accounts for V_{o1}, can be calculated by solving Equation (6):

$$V_{o1} = \frac{1}{C_{un}}\int i_{t,r}(t)dt + R_s i_{t,r}(t) + L_s \frac{di_{t,r}(t)}{dt} \tag{6}$$

The characteristic equation of this circuit will be as follows:

$$\frac{d^2\left(i_{t,r}(t)\right)}{dt^2} + 2\alpha\frac{d\left(i_{t,r}(t)\right)}{dt} + \omega_0^2 i_{t,r}(t) = 0 \tag{7}$$

where $\alpha = R_s / 2L_s$ is the damping coefficient and $\omega_0 = 1/\sqrt{L_s C_{un}}$ is the resonance frequency. According to the values of α and ω_0, Equation (7) can have three different responses, which are called as the over-damped, under-damped, and critically damped. The response time of the circuit is regarded as the time in which the C_{un} is completely discharged to L_s. Thus, in order to achieve a fast response, the under-damped response is preferred. However, it should be considered that in order to minimize the leakage current, the time constant of the circuit should be much more than the switching time of the transistors. Empirically, assuming that $\omega_0 \approx 3 \times \alpha$ may lead to an acceptable response. With this assumption, the circuit in Figure 5 shows an under-damped response for V_{o1}. This can be stated as follows:

$$i_{t,r}(t) = A_0 e^{-\alpha t}\sin(\omega_d t) \tag{8}$$

where $i_{t,r}(t)$ is the transient response of the inductor current accounts for V_{o1}. Also, ω_d is the ringing frequency, and it is equal to $\sqrt{\omega_0^2 - \alpha^2}$ (rad/sec) and $A_0 = V_{o1}/L_s\omega_d$ (A). The current $i_{t,r}(t)$ reaches to its maximum value within t_{rise}, which can be obtained as follows:

$$t_{rise} = \frac{\arctan\left(\frac{-\alpha}{\omega_d}\right) + \frac{\Pi}{2}}{\omega_d} \tag{9}$$

As it is shown in Figure 5, the time duration of this phase is determined by t_{rise}. The minimum total current of the inductor at the end of this phase can be expressed as follows:

$$i_{L,r(\min)}(t_{rise}) = \left|i_{t,r}(t_{rise})\right| - \left|i_{s,r}(t_{rise})\right| \tag{10}$$

where $i_{L,r(min)}(t_{rise})$ is the initial condition of the inductor at the start of the next phase.

2.2.3. Inductor's current falling phase (Φ_{fall}). The simplified circuit in this phase is shown in Figure 6 . The initial current of the inductor is defined as I_0, and the DC voltage of the output is assumed as V_{o2}. As it is seen, M_2 transistor is short-circuited, and because of the zero initial condition of C_{un} from the previous phase, M_3 is always off. Similarly, because V_{GS} of M_1 is zero, this transistor is also off during

DOI: 10.1002/cta

this phase. Furthermore, as drain and source terminals of M_1 are exchanged, switch S_5 is open, and also, M_4 is off. This way, the rectifier can be ignored in this phase, and the equivalent circuit can be considered as a mere RLC loop. The time interval in which the total current of the inductor, $i_{L,f}(t)$, is unloaded to C_{out} is called as t_{fall}. To determine t_{fall}, the time for which $i_{L,f}(t)$ reaches to zero should be calculated through the circuit analysis. For this analysis, three different voltage sources should be considered. Thus, the first term of $i_{L,f}(t)$ accounts for $v_s(t)$, and the two other last terms are owing to the initial condition of C_{out} an L_s notated as V_{o2} and I_0, respectively. It should be noted that V_{o2} is the same as the DC voltage of the converter output.

If the effect of $v_s(t)$ on the total inductor current, $i_{L,f}(t)$, is represented by $i_{s,f}(t)$, then this current amplitude can be given by the following:

$$\left|I_{s,f}(j\omega)\right| = \frac{\sqrt{1+(R_L C_{out}\omega)^2}\times|V_s(j\omega)|}{\sqrt{(R_L(1\text{-}L_s C_{out}\omega^2)+R_s)^2+(R_s R_L C_{out}\omega+L_s\omega)^2}} \tag{11}$$

where $|I_{s,f}(j\omega)|$ is Fourier transform of $i_{s,f}(t)$. For the second and third terms of the inductor current, the transient response of the circuit in Φ_{fall} should be solved. The characteristic equation of this phase is similar to (7) except that here α and ω_0 are as follows:

$$\alpha = \frac{1}{2}\frac{L_s+R_s R_L C_{out}}{R_L L_s C_{out}}\ (1/\sec) \tag{12}$$

$$\omega_0 = \sqrt{\frac{R_s+R_L}{R_L L_s C_{out}}}\,(rad/\sec) \tag{13}$$

Identically, according to the values of α and ω_0, the characteristic equation in this phase can have three different responses. It should be noted that in order to decrease the ripple at the converter output, the value of C_{out} should be large enough. This way, the characteristic equation in this phase usually has an over-damped response. The initial condition for (7) in Φ_{fall} can be obtained from I_0 and V_{o2} as follows:

$$i_{t,f}(0) = I_0, \tag{14}$$

$$\frac{di_{t,f}(0)}{dt} = \frac{-R_s I_0 - V_{o2}}{L_s}, \tag{15}$$

where $i_{t,f}(t)$ is the transient current response of the inductor to I_0 and V_{o2}. The response of the circuit is determined as follows:

$$i_{t,f}(t) = \left(\frac{R_s I_0 + V_{o2} + L_s I_0 s_2}{L_s(s_2-s_1)}\right)e^{s_1 t} - \left(\frac{R_s I_0 + V_{o2} + L_s I_0 s_1}{L_s(s_2-s_1)}\right)e^{s_2 t} \tag{16}$$

where s_1 and s_2 are the natural frequencies of the RLC loop in Φ_{fall}.

The ideal case during Φ_{fall} is achieved if the total current of L_s is discharged into C_{out}, and also, the reverse current is zero. As $i_{L,f}(t) = i_{t,f}(t) + i_{s,f}(t)$, the relation (17) guarantees the positivity of $i_{L,f}(t)$.

$$i_{t,f}(t) \geq \left(i_{s,f}(t)\right)_{p\text{-}p} \tag{17}$$

where $(i_{s,f}(t))_{p-p}$ is the peak-to-peak amplitude of $i_{s,f}(t)$. The pulse width of ϕ_2, notated as t_{fall}, can be calculated as follows:

DOI: 10.1002/cta

$$i_{t,f}(t_{fall}) = \left(i_{s,f}(t_{fall})\right)_{p\text{-}p} \tag{18}$$

From parametric values of ω_0 and α in the characteristic equation in both of last two phases, it is concluded that t_{rise} and t_{fall} depend only on L_s, R_s, C_{un}, and C_{out}. Hence, the variation of I_0, V_{o1}, and V_{o2} has no effect on t_{rise} and t_{fall}. This confirms the robustness of the proposed circuit against the timing scheme of the different phases.

2.3. Control unit of the proposed converter

The output voltage in Figure 3 increases up to the maximum value that the converter produces at its output. To regulate the voltage at a certain level, a control unit is needed to limit the output voltage at the desired value. As is shown in Figure 7(a), this control unit is employed in the feedback branch of the proposed converter. To realize V_{ref}, a robust and accurate voltage reference generator introduced in [15] is utilized. To regulate V_{out}, the control unit compares a fraction of that notated as γV_{out} with V_{ref} where γ is a resistive ratio of V_{out} that is realized by off-chip resistors. Furthermore, these off-chip resistors can be used to compensate the process variation errors of the reference voltage. In the comparison unit, If $\gamma V_{out} > V_{ref}$, the output of the comparator is low, and S_2 and S_4 switches are off. Similarly, if $\gamma V_{out} < V_{ref}$, the output of the comparator is high, and in ϕ_2, S_2 and S_4 switches are closed until the end of this phase. This way, the output is regulated. As it is shown in Figure 7(b), the utilized comparator is a conventional cross-coupled positive feedback amplifier [16]. Here, γV_{out} is connected to V_{in-}, and also, V_{ref} and V_{com} are connected to V_{in+} and V_{out+}, respectively.

2.4. Design procedure of the proposed converter

A design example of the proposed inductor-reused buck-boost converter is presented, and its theoretical analysis and calculations are elaborated in the following section. For this circuit, the design parameters are C_{un}, C_{out}, R_L, and the aspect ratio of the switches.

It should be noted that L_s and R_s are self-inductance and series resistance of the off-chip coil, respectively. According to the experimental results, the values of L_s and R_s are considered to be 2 μH and 0.5 Ω, respectively [4]. In addition, as $v_s(t)$ is assumed an inductive voltage source in bio-implant applications, its frequency, f_1, is obtained from the minimum power loss calculations. For near-field in-body power transfer applications, frequencies about 10 MHz have minimum losses when passing through the body [17]. So the frequency of $v_s(t)$, f_1, is assumed as 10 MHz. To achieve a fast response in Φ_{rise}, as it was mentioned before, it is assumed $\omega_0 \approx 3 \times \alpha$. C_{un} = 200 nF satisfies this relation and from (7) gives $|\alpha|$ = 0.5 e + 6 (1/sec) and $|\omega_0| \approx$ 1.58 e + 6 (rad/sec). Also, ω_d is equal to $\sqrt{\omega_0^2 - \alpha^2} = 1.5e + 6$(rad/sec) and $A_0 = V_{o1} / L_s\omega_d \approx$ 0.53 A. The current $i_{t,r}(t)$ reaches to its maximum value within t_{rise}, which can be obtained from (8) and (9) as t_{rise} = 0.64 μs and $i_{t,r}(t$ = 0.64 μs) = 330 mA.

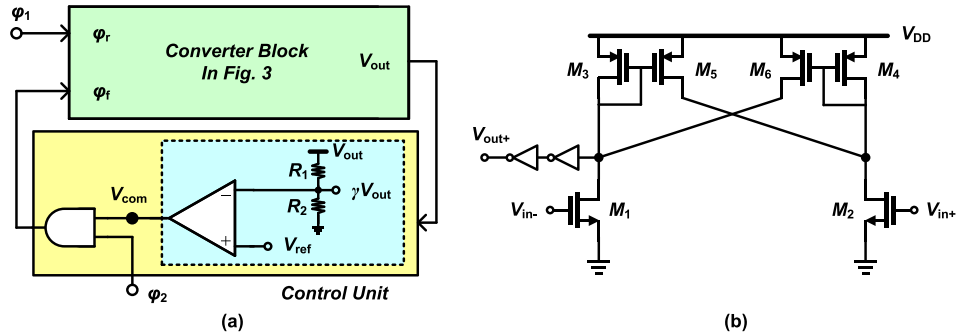

Figure 7. (a) Control unit circuit of the proposed inductor-reused buck-boost converter and (b) utilized comparator. [Colour figure can be viewed at wileyonlinelibrary.com]

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During Φ_{rise}, the effect of $v_s(t)$ on $i_{L,t}(t)$ should also be surveyed. For this, the steady state sinusoidal response of current, $i_{s,r}(t)$, should be considered. From Figure 5 and relation (5), it can be written as follows:

$$\left|I_{s,r}(j\omega)\right| >> \frac{1}{40\pi}\left|V_s(j\omega)\right| \tag{19}$$

where $I_{s,r}(j\omega)$ and $V_s(j\omega)$ are the Fourier transforms of $i_{s,r}(t)$ and $v_s(t)$, respectively. In power transfer via the inductive link, the received voltage amplitude rarely reaches to 10 V [18]. So, at the worst case, the amplitude of $i_{s,r}(t)$ is less than 80 mA, and therefore from the relation (10), the minimum value of $i_{L,r}(t)$ at the end of Φ_{rise} is obtained as 250 mA.

In Φ_{fall}, the circuit in Figure 6 should be analyzed. The value of C_{out} is determined regarding the specified ripple of the output voltage. If the ripple is considered to be 0.5 mV for a 1 mA load current, C_{out} can be obtained as follows:

$$C_{out} = \frac{I_{Load}\Delta t}{\Delta V} = \frac{1^{mA}5^{\mu s}}{0.5^{mV}} = 10\mu F \tag{20}$$

where ΔV is the ripple of the output voltage, I_{Load} is the load current, and Δt is the switching period. As for some implantable neuroprosthetic applications such as retinal implants, C_{out} is off-chip, and the calculated value is reasonable [4]. In Φ_{fall}, from relations (12) and (13), the values of α and ω_0 are 0.5×10^6 (1/sec) and 0.22×10^6 (rad/sec), respectively. Because $\alpha > \omega_0$, the response of the circuit is over-damped. According to (11), the maximum amplitude value of $i_{s,f}(t)$ is about 8 mA.

The pulse width of ϕ_2, notated as t_{fall}, is obtained from (18) as 150 nsec. It is rounded to a lower value to overcome the non-idealities of the components and preventing the reverse current.

In design of the switches, the aspect ratio (W/L) of transistors should be high enough to tolerate the maximum current passing through them. In other words, the series resistance of the switches should be small enough compared with R_s (e.g., $R_{switch} << R_s$). On the other hand, these transistors could not be so large, as they increase the transient response of the circuit. Also big switches results in large parasitic capacitors. This will affect the time constants of RLC loops that are considered in Φ_{rise} and Φ_{fall}. This may result in deviation of the t_{rise} and t_{fall} from their calculated values. Of course, the effective length of transistors should have the smallest value of the utilized technology to reduce the parasitic capacitors. It is worth to mention that in this design, thick oxide transistors of TSMC 0.18 um CMOS process are utilized owing to the voltage limitations. The minimum feature size of these transistors is L_{min} = 0.35 μm. The size of all utilized switches are the same with (W/L) = 50 × 64/0.35 μm.

3. SIMULATION RESULTS

To evaluate the functionality of the proposed converter, the circuit-level simulation results are provided in this section. The simulations are performed in Cadence Spectre using TSMC CMOS 0.18 μm technology. For the circuit shown in Figure 3, the transient simulations are performed. In the absence of the control unit, the output of the converter in Figure 3 reaches to its maximum voltage that the converter can drive the load. The simulation result of this circuit is shown in Figure 8. As it is seen, the maximum output voltage level of the converter is about 2.3 V. The simulated transient current of the inductor in Φ_{rise} and Φ_{fall} is shown in Figure 9. The simulation result showing the current in Φ_{rise} follows Equation (10) where a sinusoidal steady state current is summed with a transient current. In addition, as it is seen, the current of the inductor is discharged to C_{out} in Φ_{fall}, and it reaches to zero at the end of this phase.

Transient simulations for the complete converter that is shown in Figure 7(a) are performed assuming that the received voltage level and switching frequency are equal to 4 V and 200 kHz, respectively. Also, the output voltage of the circuit is considered to be 1 V for a 1 kΩ load. The output power is considered to be in the range of mW because the proposed converter is designed for IMD applications such as retinal implants, cochlear implants, and invasive wireless neural recording

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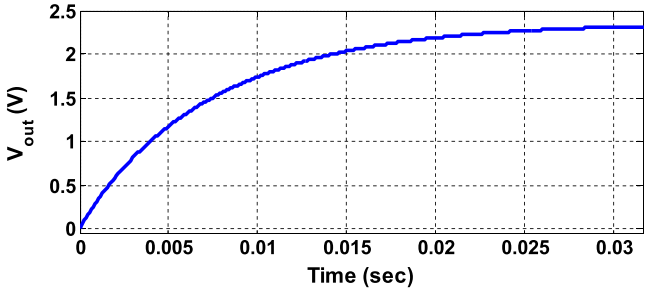

Figure 8. Simulated output voltage of the proposed converter in Figure 3 without the control unit. [Colour figure can be viewed at wileyonlinelibrary.com]

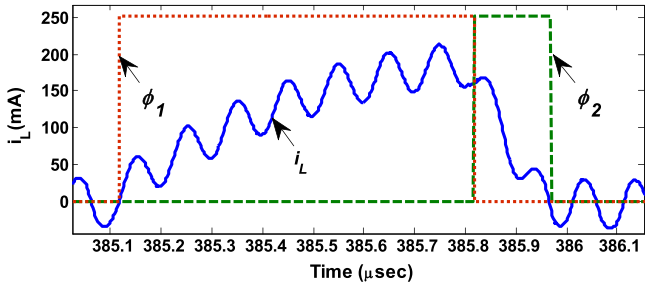

Figure 9. Inductor current of the proposed converter in Figure 3 in ϕ_1 and ϕ_2 phases. [Colour figure can be viewed at wileyonlinelibrary.com]

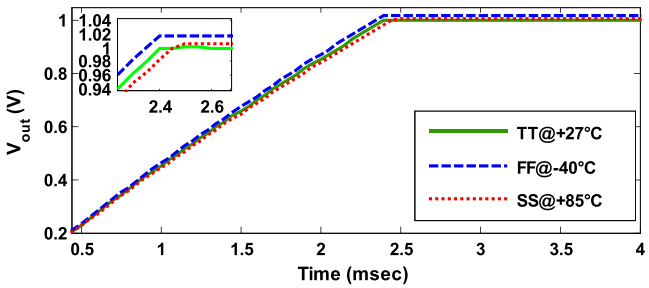

Figure 10. Output voltage of the circuit in Figure 7(a) in different process corner cases for V_{out} = 1 V. [Colour figure can be viewed at wileyonlinelibrary.com]

systems where their power consumption is in this range [2–4, 6,18]. The simulated output in different process and temperature corner cases are illustrated in Figure 10. It can be seen that for the worst case, the maximum output voltage error is less than 20 mV. In addition, simulation results show that the maximum voltage ripple is 0.5 mV at a 1 mA load current. Interestingly, this value is the same as assumed in (20).

According to the measurement results in [18], here, it is assumed that the voltage amplitude of the received AC signal across the coil varies in the range of 3 ~ 6 V. The proposed converter with different amplitudes of the input voltage level is simulated, and the related efficiency is plotted in Figure 11. The simulation results confirm a suitable degree of the efficiency robustness against the variation of the coupling coefficient (k_P) between the power transferring and receiving coils. The coupling coefficient in IMDs can be changed by different factors like the wetness of the skin, distance, and the angle between the two coils. This, in turn, leads to the variation of the coil received voltage amplitude. If a linear regulator is used in IMDs, the variation of k_P may result in a significant power loss on the regulator and also the reduction of its efficiency. For example in [18], when the unregulated input voltage of the linear regulator is 3.55 V, its efficiency is about 91% with 250 mV

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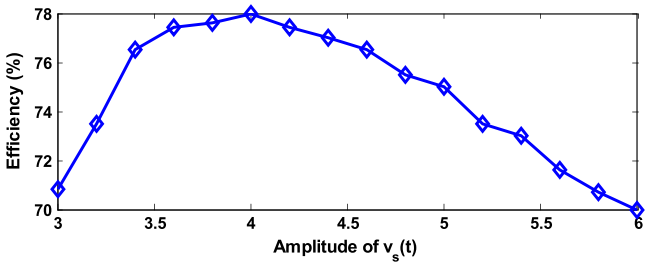

Figure 11. Power efficiency of the proposed converter versus different input voltage amplitudes for $V_{out} = 1$ V and $R_L = 2$ kΩ. [Colour figure can be viewed at wileyonlinelibrary.com]

dropout voltage. However, if the input voltage amplitude is increased to 6 V, the efficiency may decrease to less than 55%. In contrast, as it is seen in Figure 11, by using a nonlinear regulator for IMD applications, the variation of the efficiency is less than 8% for the input voltage variation within 3 ~ 6 V while its maximum efficiency is 78%.

It should be noted that the utilized rectifier in the proposed converter is taken from [12], and its efficiency is not included in Figure 11. This is because in this paper, only the DC-to-DC converter is studied. As in the other similar works, only the converter results are reported. Thus in order to have a fair comparison, we have also investigated the efficiency of this part, and the efficiency of the rectifier itself is excluded. Furthermore, it should be noticed that the rectifier structure could be simply replaced by other highly efficient topologies (e.g.; active rectifiers). However, in the proposed structure, a simple passive rectifier has been utilized.

A Monte-Carlo simulation is performed to evaluate the power efficiency robustness of the proposed converter against the process variations and device mismatch. This simulation is performed in Cadence Spectre-RF using the mismatch models of TSMC CMOS 0.18 μm technology with 100 iterations. As shown in Figure 12, the mean of the output power efficiency is 77.8%, and its standard deviation (σ) is about 0.43%, which is negligible and confirms the robustness of the proposed converter. The reason is that only ON resistance (r_{on}) of the switches affects the efficiency in Monte-Carlo simulations. Because

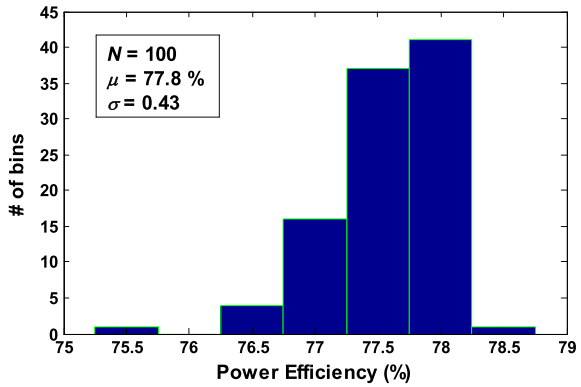

Figure 12. Histogram of the power efficiency against process variations and mismatch of the switches. [Colour figure can be viewed at wileyonlinelibrary.com]

Table I. Power dissipation contribution of each element in Figure 3 for $V_s = 4$ V.

Element	Power dissipation/total power (%) *
$S_1 + S_3$	33.8
$S_2 + S_4$	6.2
R_s	60.0

*Excluding rectifier.

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Table II. Simulated performance summary of the proposed converter.

Parameter	Value
Technology	0.18 μm CMOS
Input DC voltage (after rectifier)	1.5 V ~ 3.5 V
Output DC voltage	0.6 V ~ 2.3 V
Output current	1 μA ~ 4 mA
Switching frequency	200 kHz
Maximum efficiency	78%
Line regulation	0.048 *V*/V
Load regulation	0.027 *V*/V
Maximum ripple	±0.5 mV

the size of these switches is chosen large enough, the variation of r_{on} accounts for the device mismatch and process variations is negligible. It should be mentioned that r_{on} is defined to be much smaller than the series resistance of the inductor (R_s). This way, the standard deviation of the power efficiency histogram is small enough.

For $V_s = 4$ V, the contribution of the power dissipation of each section in Figure 3 is given in Table I. Also, the performance summary of the proposed buck-boost converter is given in Table II. It should be mentioned that in this table, the effect of the rectifier circuit is not considered. Although the proposed inductor-reused buck-boost converter works in three phases, its maximum power efficiency and other performances are acceptable as a buck-boost converter.

4. CONCLUSIONS

In this paper, the realization of a buck-boost converter for power transferring through the inductive links, especially for the bio-implant applications, is introduced. By reusing the inherent inductor of the coil, the large off-chip inductor of the conventional buck-boost converter is eliminated. According to the simulation results, the performance of the proposed converter is comparable with other works and has a good robustness. The efficiency of the proposed converter is independent of the received voltage amplitude. So it can be regarded as a suitable alternative for linear regulators utilized in power-receiving inductive links. The main superiority of the proposed inductor-reused buck-boost converter is that it utilizes only five switches and a low power control unit. This way, a voltage converter with a lower complexity is achieved. The simulation results confirm that it can be a proper choice for low-power bio-implant applications.

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