CrossMark

An Automatic Action Potential Detector for Neural Recording Implants

Saeid Barati[1] · Mohammad Yavari[1] ⓘ

Abstract

In this paper, a low-power CMOS analog automatic action potential (AP) detector is proposed for wireless neural recording implants. The proposed AP detector is based on comparing the neural input signal with an analog threshold level. The threshold level is obtained by calculating the root mean square value of the neural input signal. In order to generate the threshold voltage level, the AP detector incorporates a continuous-time (CT) sigma-delta ($\Sigma\Delta$) modulator in its analog signal processing section. This structure benefits from the combination of a CT $\Sigma\Delta$ modulator and a single-bit DAC as the multiplier to reduce the power consumption. Although in contrast to the traditional methods, the required circuits are not biased in the subthreshold region, the total power consumption is reduced. The proposed AP detector is designed in TSMC 90 nm CMOS technology and consumes 11.8 μW from a single 1-V power supply. It is worth mentioning that the utilized CT $\Sigma\Delta$ modulator can also be used in the analog-to-digital converter to significantly reduce both the power consumption and silicon area of the complete neural recording system.

Keywords Action potential detection · Neural recording systems · CT $\Sigma\Delta$ modulators · Root mean square (RMS) · Analog-to-digital converters · Threshold level · CMOS technology

1 Introduction

The implanted neural recording micro-systems under the brain skull record neural signals, and then, they send them wirelessly from different regions of the brain to

✉ Mohammad Yavari
myavari@aut.ac.ir
https://www.ele.aut.ac.ir/yavari

Saeid Barati
s_barati@aut.ac.ir

[1] Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), 424 Hafez Ave., Tehran 15914, Iran

the outside world [10, 16]. Nowadays, these systems are increasingly considered by neuroscientists and neurophysiologists. In these systems, more channels are needed to record the activity of the neurons simultaneously as well as the real time. But, more recording sites result in the massive amount of data, and it needs more power dissipation to transfer the data to the outside world. Since small level of chronic heat dissipation (80 mW/cm^2) can lead to the tissue damage, this can be unsafe for activity of the neurons. Accordingly, the data rate reduction is more important in the neural recording systems. On the other hand, in most implanted wireless systems, the power is wirelessly transferred through inductive links [3] and it is very difficult to transfer more power to the implant. Moreover, different power supply voltages have been used in these systems such as 5–0.45 V [6, 10, 16]. So, the power consumption is very important in such systems and it should be highly reduced.

The neural signal contains a background noise and small action potentials (APs). Since in many applications, the presence and timing of the action potentials in the neural signal are the useful information, it is used in the data reduction [10]. The AP detection circuit, which is used to distinguish the AP from the background noise in a non-stationary noisy analog waveform, has the main role in this data reduction method. Generally, the neural signal amplitude is around 100–500 µV. To prepare the neural signal for AP detection, it is amplified with a gain around 40–60 dB within the bandwidth of 300 Hz to 10 kHz. The duration of the action potentials is approximately 1 ms and after this time, the nerve or muscle is unresponsive to further stimulation, and hence, nothing happens. This is called the refractory period as shown in Fig. 1.

Among the AP detection methods, the AP detection by the hard threshold is the most popular technique. In this method, the neural signal is compared with a pre-defined threshold voltage (V_{THR}) level to detect the AP. By multi-stage neural signal conditioning (amplification and filtering), APs are distinguished from the background noise sufficiently and the voltage ratio of the AP to the background noise remains almost constant. Nonetheless, the amplitude of the neural signal (AP and background noise) varies among different channels in the multi-electrode neural recording systems.
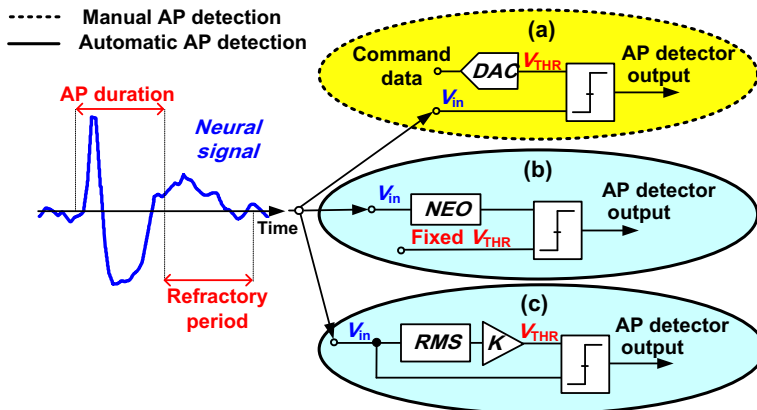

Fig. 1 a Manual AP detection, **b** automatic AP detection by NEO, and **c** automatic AP detection by RMS measurement

These variations are mainly due to the random distance between different electrodes and the corresponding neurons. Owing to the neural signal amplitude variations in different channels, a fixed presumption of the threshold level cannot be set easily.

The threshold-based AP detection approach is classified into two main categories: manual [10] and automatic [4, 9, 13]. The manual AP detection is shown in Fig. 1a. It utilizes a DAC to set the V_{THR} based on a command data, which is sent by the user to the implanted system wirelessly, resulting in more complexity. The automatic AP detection is shown in Fig. 1b. It is comprised of a nonlinear energy operator (NEO) and a comparator. The analog implementation of the NEO can be realized by multipliers, differentiators, etc. Besides, its function is defined as:

$$\text{NEO} = \left(\frac{dV_{\text{in}}}{dt}\right)^2 - V_{\text{in}} \times \left(\frac{d^2 V_{\text{in}}}{dt^2}\right). \tag{1}$$

The neural signal is injected into the NEO, and then it is compared with a fixed V_{THR}. As another type, based on the RMS measurement, the automatic AP detection calculates the RMS value of the neural signal to adaptively define V_{THR} as shown in Fig. 1c. In this approach, V_{THR} is considered as:

$$V_{\text{THR}} = K \times \text{RMS} \tag{2}$$

where K is a constant and its typical value is between 3 and 7 [4]. In this method, the RMS measurement is the main challenge and it should be measured frequently because the neural signals have time-variant statistical characteristics, and hence, they are non-stationary signals [15].

In this paper, an automatic AP detector is proposed using an analog RMS measurement. It utilizes a $\Sigma\Delta$ modulator as the multiplier to reduce the power consumption. Recently, the $\Sigma\Delta$ ADC is also utilized in the neural recording [11, 20] and other biomedical systems [5]. In such cases, the sigma-delta modulator of the ADC can also be used in the proposed AP detector.

The rest of the paper is organized as follows. The proposed AP detector is presented in Sect. 2. Analysis of the proposed AP detector is provided in Sect. 3. The circuit-level simulation results of the proposed structure are presented in Sect. 4, and finally, Sect. 5 concludes the paper.

2 Proposed Automatic AP Detector

The RMS measurement is usually realized by two different comparing and computing methods. Due to the extra processing steps, the comparing method is complicated than the computing scheme. It is known that the RMS value of a signal, $V_{\text{in}}(t)$, is calculated as:

$$\text{RMS} = \lim_{T \to \infty} \sqrt{\frac{1}{T} \int_0^T V_{\text{in}}^2(t) \, dt} = \sqrt{\overline{V_{\text{in}}^2(t)}} \tag{3}$$
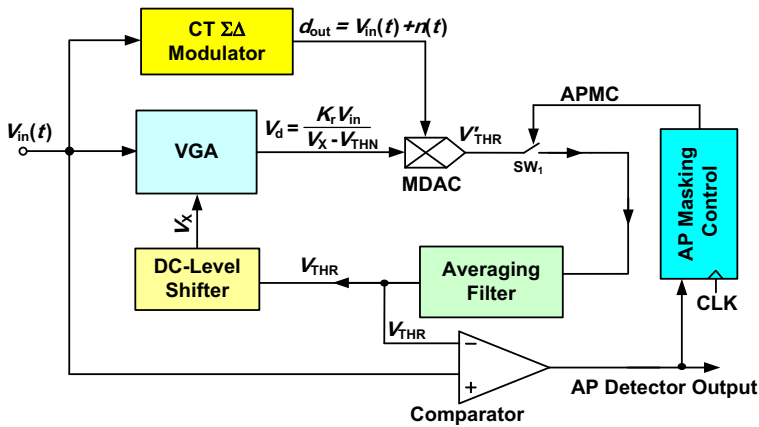
Fig. 2 Block diagram of the proposed automatic AP detector

The RMS computing method can be realized using analog or digital signal processing circuits. In the latter, the RMS value is calculated by digital computation which occupies large chip area making it an unsuitable choice for implanted systems. In contrast, the analog computing method can save the area and offers high-speed circuits [1]. Although it is common to utilize the Gilbert cell multiplier to realize the square function in the analog computing method, it is not suitable for low-power applications. The multiplier is a power hungry part of the analog RMS computing method [4]. In this paper, an action potential detector based on analog computing method and a novel RMS measurement is proposed.

2.1 System Architecture

Figure 2 depicts the block diagram of the proposed automatic AP detector. The detector is implemented using a novel analog processor comprising of a comparator, AP masking control (digital control unit) and tree signal processing modules. These modules include a variable gain amplifier (VGA) as the divider, a CT $\Sigma\Delta$ modulator along with a multiplying DAC (MDAC) to realize the multiplier and the averaging filter. These modules are used in a closed-loop feedback structure to set the V_{THR} which is proportional to the RMS value of the input signal, $V_{\text{in}}(t)$.

The operation of the proposed automatic AP detector is explained as follows. As shown in Fig. 2, the input neural signal, V_{in}, is applied to the VGA where its gain is proportional to K_r/V_X. By this gain, the VGA operates as a divider. The multiplier constitutes of a CT $\Sigma\Delta$ modulator and an MDAC. The serial two-level bit stream of the CT $\Sigma\Delta$ modulator with the sampling frequency of f_s is applied to control the embedded polarity switch in the MDAC. This way, the analog divider output signal, V_d, is converted to its positive or negative value. Thus, it is concluded that the polarity switch operates as a multiplier. The output of the MDAC is passed through a low-pass averaging filter with a low cut-off frequency. It is required to suppress all high-frequency components accounting for the switching operation of the MDAC

and also the shaped quantization noise of the CT $\Sigma\Delta$ modulator. The output of the averaging filter, V_{THR}, is shifted by a DC-level shifter. Finally, a comparator compares the input neural signal with the output of the averaging filter. When the neural signal, $V_{in}(t)$, crosses V_{THR}, an AP is detected, and the comparator output is high. The AP masking control (APMC) unit which is composed of a clocked counter and a few logic gates opens the switch SW_1 after 2 ms when an AP is detected. This window time is similar to a typical AP duration plus the refractory period. In this window time, the comparator output remains at the high state and the switch SW_1 is open.

2.2 Variable Gain Amplifier (VGA) as a Divider

As mentioned before, the VGA is utilized as a divider in the proposed AP detector. The utilized VGA shown in Fig. 3 is similar to the one introduced in [7]. This amplifier consists of an input differential pair (M_3 and M_4) and diode-connected loads (M_5 and M_6). The gate voltage of M_7 and M_8 is controlled by a common-mode feedback (CMFB) circuit which is not shown in Fig. 3 for simplicity. The differential gain of the VGA is given by [7]:

$$A_v = \frac{V_d}{V_{in}} \approx \sqrt{\frac{(W/L)_3 I_1}{(W/L)_5 I_2}} \tag{4}$$

where $I_2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_X - V_{THN})^2$ and V_{THN} is the threshold voltage of the NMOS transistors. The output voltage, $V_d(t)$, is calculated as:

$$V_d(t) = \frac{K_r\, V_{in}(t)}{(V_X - V_{THN})}$$
$$K_r = \sqrt{\frac{2(W/L)_3 I_1}{\mu_n C_{ox}(W/L)_2(W/L)_5}} \tag{5}$$

where the input signal, V_{in}, is divided by V_X with a gain of K_r which is controlled by the I_1 current source and the aspect ratios of M_2, M_3 and M_5 transistors. The simulated device parameters are also illustrated in Fig. 3.

2.3 CT $\Sigma\Delta$ Modulator and MDC as a Multiplier

In the proposed AP detector, the multiplier is implemented by the combination of a CT $\Sigma\Delta$ modulator and an MDAC. This structure converts the analog neural signal to a single-bit two-level data stream to control the MDAC switch. The single-bit first-order CT $\Sigma\Delta$ modulator is illustrated in Fig. 4. The output of the modulator in frequency domain is given by:

$$D_{out}(f) = \underbrace{\frac{\sin(\pi f/f_s)}{(\pi f/f_s)}}_{STF} V_{in}(f) + \underbrace{\frac{2\sin(\pi f/f_s)}{k_1}}_{NTF} Q(f). \tag{6}$$
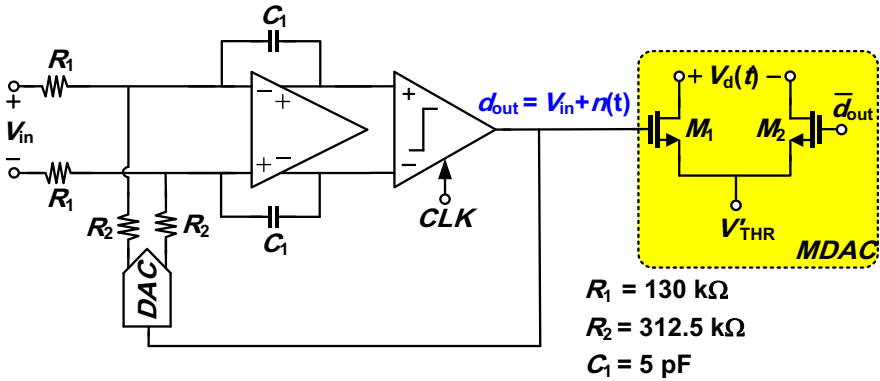
Fig. 3 VGA circuit [7]

Fig. 4 First-order CT $\Sigma\Delta$ modulator

where Q, STF and NTF are the quantization noise, signal and noise transfer functions, respectively. The STF is a sinc function with the gain of unity in the neural signal bandwidth. Assuming a single-bit quantizer utilized in the CT $\Sigma\Delta$ modulator, the root spectral density of the shaped quantization noise can be stated as:

$$N(f) = Q(f)|\text{NTF}(f)| = \frac{\sin(\pi f / f_s)}{k_1\sqrt{12 f_s}}. \tag{7}$$

By increasing the oversampling ratio (OSR), the in-band quantization noise is decreased and the accuracy of the multiplier is enhanced as will be discussed in Sect. 3.2. The proposed AP detector has more efficiency in terms of the power consumption and area. If it is utilized in the neural recording system with $\Sigma\Delta$ ADCs, then its modulator can be shared by the proposed AP detector as well. Therefore, the modulator is designed based on the specifications of the ADC which is used in the neural recording system. The modulator's resolution is considered as 8-bit for a signal bandwidth of 10 kHz.

The noise transfer function (NTF) is firstly generated in z-domain by Schreier's Delta-Sigma Toolbox [19]. Then, the discrete-time (DT) loop filter is derived as $\text{LF}(z) = 1/\text{NTF}(z) - 1$. Owing to the low sampling frequency of the utilized CT sigma-delta modulator, the excess loop delay (ELD) does not cause instability since the delay of the loop filter is less than 10% of the sampling period [21].

The DT loop filter is converted to a continuous-time one using the "d2c" function of the MATLAB Control System Toolbox to obtain the coefficients of the CT loop filter. The non-return-to-zero (NRZ) feedback DAC is considered by the zero-order

Fig. 5 Multiplier realization with the combination of a CT $\Sigma\Delta$ modulator and an MDAC
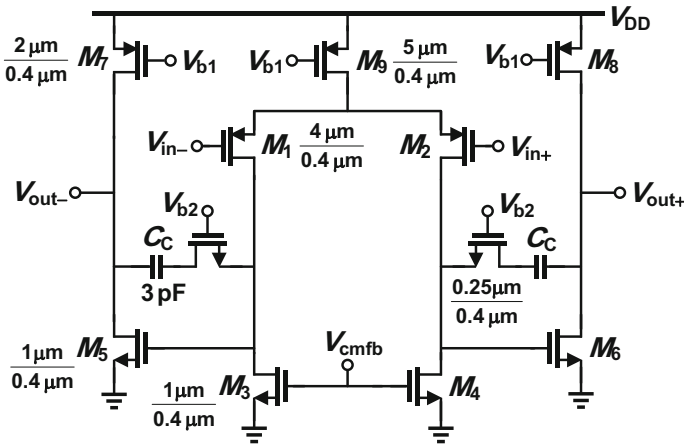

Fig. 6 Simulated two-stage OTA

hold method in the utilized MATLAB function. The structure of single-bit first-order CT $\Sigma\Delta$ modulator is illustrated in Fig. 4, and its scaled coefficients are $\{k_1, k_2\} = \{0.6, 0.5\}$.

Figure 5 shows the circuit realization of the multiplier including the $\Sigma\Delta$ modulator and MDAC. It incorporates a first-order feedback loop filter implemented using active RC integrators. Due to the high swing requirement in the single-bit first-order CT sigma-delta modulator, a fully differential two-stage Miller compensated operational transconductance amplifier (OTA) is utilized here. The schematic of the OTA with the simulated device parameters is depicted in Fig. 6. The circuit-level realization of the comparator including the preamplifier and cross-coupled latch is shown in Fig. 7 which has been introduced in [2]. The comparator employs a fully differential preamplifier to reduce both the offset and kickback noise of the cross-coupled latch. This circuit is used to implement both the comparator of the sigma-delta modulator and AP detection.
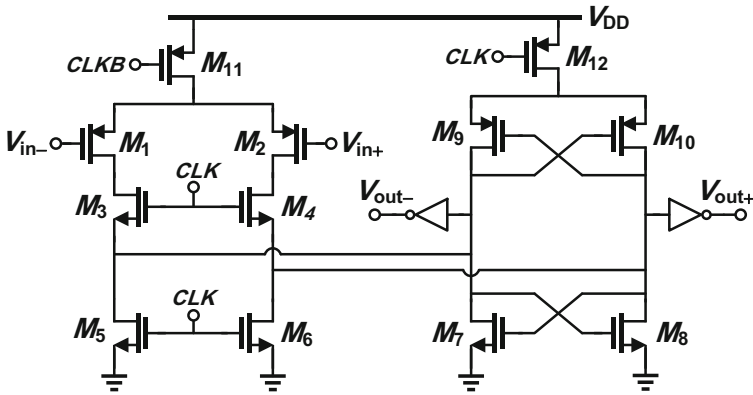
Fig. 7 Simulated comparator [2]

2.4 Averaging Filter

The averaging filter is a low-pass filter with a very low cut-off frequency around a few hundred hertz. Generally, this filter can be realized using discrete-time or continuous-time circuits. In discrete-time implementation, the large time constant realization needs large capacitors. On the other hand, its CT implementation such as the Gm-C one results in lower power consumption and smaller chip area. The cut-off frequency of the low-pass Gm-C filter is set by the G_m/C ratio. Therefore, the low-pass Gm-C filter with a low cut-off frequency can be realized with a very small G_m (around a few nA/V) or with a large capacitor. A very small G_m reduces both the power and area simultaneously, and it has been used in several bio-potential applications including [18, 22]. Nonetheless, the nonlinearity and noise are increased owing to utilizing a very small G_m and some additional techniques are needed to improve the linearity and noise performance [22]. This results in some more area and power consumption. Alternatively, the current conveyors can be used to simply realize a low-pass filter with a very low cut-off frequency [8, 14]. Since, here, the averaging filter is used to suppress the high-frequency components resulting from the switching operation of the MDAC and the shaped quantization noise of the sigma-delta modulator, the required specifications for this low-pass filter are not stringent, and hence, it is realized with current conveyors.

The technique identical to the second-generation current conveyor (CCII) employed as a capacitive multiplier in [8] is applied into the proposed AP detector to realize the averaging filter. As shown in Fig. 8, the utilized CCII has a low-impedance input (X), a high-impedance input (Y), and a high-impedance output (Z). The equivalent circuit for the boosted impedance seen from node Y to the ground, Z_{EQ}, and the transfer function are given by [8]:

$$Z_{EQ} = \left(\frac{r_x}{\alpha\beta} + \frac{1}{sC_S\alpha\beta} \right) || r_z$$

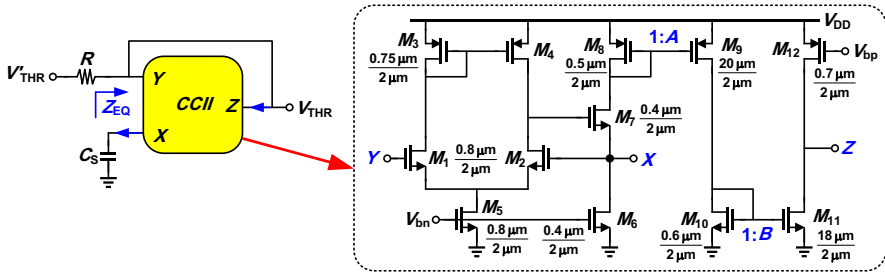$$H(s) = \frac{r_z}{r_z + R + Rr_z sC_S\alpha\beta} \tag{8}$$

Fig. 8 Schematic of the averaging filter [8]

where r_x and r_z are the finite output resistance at X and Z terminals, respectively, and $\alpha = V_X/V_Y$ is the tracking error factor which is less than one. The current gain $\beta = A \times B$ where A and B, as shown in Fig. 8, are the current mirror ratios of M_8–M_9 and M_{10}–M_{11}, respectively. The relation (8) indicates that the capacitance C_S is multiplied by a factor of $\alpha\beta$. The circuit-level realization of the averaging filter with the simulated device parameters is illustrated in Fig. 8.

3 Structural Analysis of the Proposed Automatic AP Detector

3.1 Time-Domain Analysis

As shown in Fig. 5, when d_{out} is high, the MDAC output, $V'_{THR}(t)$, is connected to the positive terminal of the divider output, $V_d(t)$. As a result, $V'_{THR}(t)$ is given by:

$$V'_{THR}(t) = d_{out} \cdot V_d(t). \tag{9}$$

By considering $d_{out}(t) = V_{in}(t) + n(t)$, where $n(t)$ is the shaped quantization noise of the sigma-delta modulator, and from relations (5) and (9), $V'_{THR}(t)$ can be written as:

$$V'_{THR}(t) = \frac{K_r\, V_{in}^2(t)}{V_X - V_{THN}} + \frac{K_r\, n(t).\, V_{in}(t)}{V_X - V_{THN}}. \tag{10}$$

where the first and second terms in the right hand of the relation (10) show the squared function of the input signal, $V_{in}(t)$, and the intermodulation function of $V_{in}(t)$ and $n(t)$, respectively. The MDAC output signal, $V'_{THR}(t)$, is passed from the averaging filter with sufficiently low cut-off frequency to filter out all of the AC terms. So, the second term in the right hand of the (10) is eliminated because the quantization noise is shaped into the high frequencies. Therefore, the filter output, V_{THR}, is the average of its input, $V'_{THR}(t)$, and it is obtained as:

$$V_{THR} = \overline{V'_{THR}(t)} = \frac{K_r}{V_X - V_{THN}} \overline{V_{in}^2(t)} \tag{11}$$

Since V_X is a DC voltage, it will be extracted from the averaging equation. The output of the averaging filter is shifted by a DC-level shifter so that $V_X = V_{THR} + V_{THN}$ where V_X is the DC-level shifter output as shown in Fig. 2. By plugging $V_X = V_{THR} + V_{THN}$, Eq. (11) is modified as:

$$V_{THR} = K\sqrt{\overline{V_{in}^2(t)}}, \quad K = \sqrt{K_r} \tag{12}$$

This equation shows the relationship between V_{THR} and the RMS of the input signal. The factor K, if properly set, determines how much the threshold level should be above the RMS value of the neural input signal.

3.2 Analysis of Threshold-Level Accuracy

As mentioned before, the APs are detectable by the threshold level between 3 and 7 times of the RMS value of the neural input signal. Therefore, there is an enough range of the acceptable accuracy for the threshold level. In this section, the parameters affecting the accuracy of the threshold level have been analyzed. To analyze the accuracy of the proposed AP detector, the frequency-domain transformation of the MDAC output in Eq. (9) can be obtained as:

$$V'_{THR}(f) = \frac{1}{f_s}\int_{-f_s/2}^{f_s/2} d_{out}(\lambda) \cdot V_d(f - \lambda)d\lambda. \tag{13}$$

Regarding that the STF is a sinc filter and its gain is unity within $[-f_s, f_s]$ and assuming that $V_{in}(t)$ is a sinusoidal signal with a frequency of f_0 (within the bandwidth of the neural signal) and amplitude A_i, by plugging (5), (6) and (7) into (13), the frequency response of $V'_{THR}(f)$ is obtained as:

$$\left| V'_{THR}(f) \right| = \frac{K_r A_i^2}{4(V_X - V_{THN})}[\delta(f - 2f_0) + 2\delta(f) + \delta(f + 2f_0)]$$
$$+ \frac{2K_r A_i}{k_1\sqrt{12f_s}(V_X - V_{THN})}\left(\frac{2\pi f}{f_s}\right). \tag{14}$$

For an averaging filter with $f_{-3\,dB} \ll f_0$, all of the out-of-band components are filtered out. Regarding the relationship between the input and output of the averaging filter $V_{THR} = \overline{V'_{THR}(t)}$ and plugging $V_X = V_{THR} + V_{THN}$ in (14), the frequency spectrum of the averaging filter output, $V_{THR}(t)$, is given by:

$$\left| V_{THR}(f) \right|^2 = \frac{K_r A_i^2}{2} + \frac{2K_r A_i}{k_1\sqrt{12f_s}}\left(\frac{2\pi f}{f_s}\right). \tag{15}$$

The first term in relation (15) is the desired squared RMS value of the sinusoidal input with a gain of K_r. The second term is the intermodulation of the sinusoidal input with the shaped quantization noise. The signal-to-quantization noise ratio (SQNR)
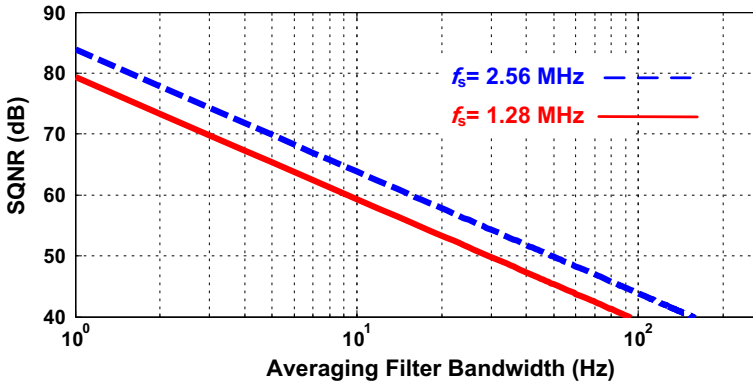
Fig. 9 SQNR of the threshold level versus the sampling frequency of the $\Sigma\Delta$ modulator and bandwidth of the averaging filter
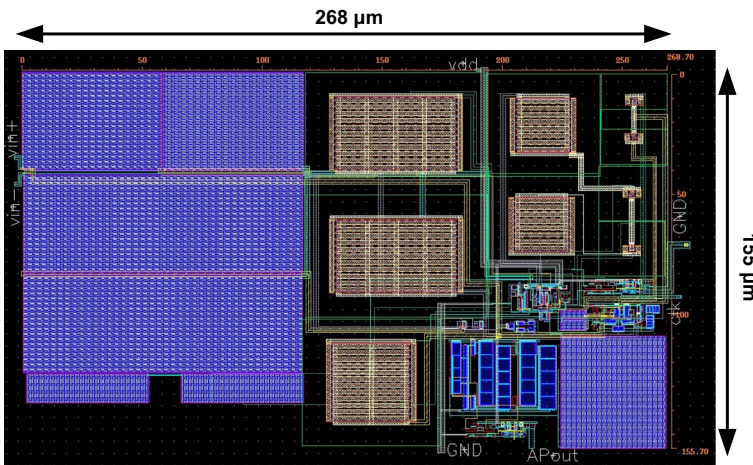

Fig. 10 Layout of the proposed automatic AP detector

is defined as the ratio of the desired value to the integral of the second term in the bandwidth of the averaging filter. Hence, the SQNR is obtained as:

$$SQNR = \frac{A_i k_1 \, f_s \sqrt{3 f_s}}{2\pi f_A^2} \tag{16}$$

where f_A is the -3 dB frequency of the averaging filter. This equation shows that the SQNR depends on the sampling frequency, signal level, and -3 dB frequency of the averaging filter. In Fig. 9, the SQNR is plotted versus the bandwidth and sampling frequency of the averaging filter and $\Sigma\Delta$ modulator, respectively. According to Fig. 9, the accuracy of the automatic AP detector is enhanced if the sampling frequency of the sigma-delta modulator is increased and/or the cut-off frequency of the averaging filter is decreased.
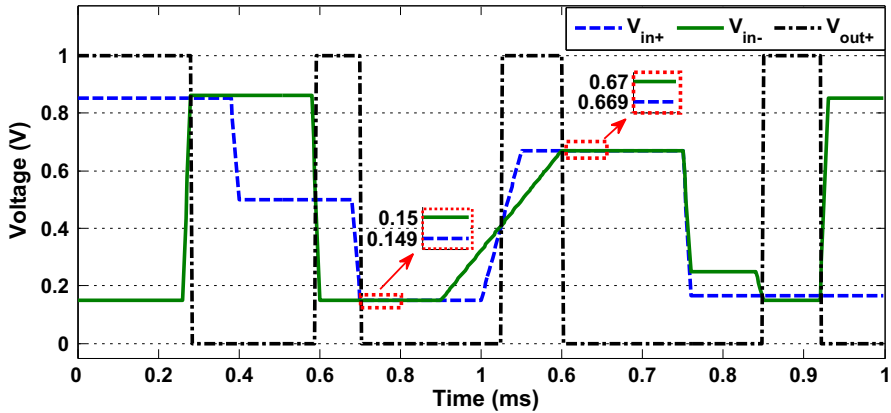
Fig. 11 Overdrive test of the simulated comparator

4 Circuit-Level Simulation Results

Transistor-level simulations in different process corner cases, power supply, and temperature variations, and also considering the device mismatch are provided to evaluate the performance of the proposed automatic AP detector. It is simulated using TSMC 90-nm CMOS process in Cadence Spectre-RF with 1-V power supply. Metal–insulator-metal (MIM) capacitors and polysilicon resistors are used in the realization of the proposed AP detector. The layout of the proposed AP detector is illustrated in Fig. 10, which occupies 268 μm × 155 μm silicon active area. In the following, the post-layout simulation results of the proposed AP detector are presented.

The simulated overdrive test of the comparator is shown in Fig. 11. As shown in Fig. 7, the comparator regenerates at the falling edge of the CLK. The CLK signal is not shown in Fig. 11 since its frequency is high, and hence, it cannot be properly illustrated in this figure. Moreover, the comparator circuit is fully differential and one of its outputs is shown in Fig. 11. According to Fig. 11, the simulated comparator works well both in full-scale and small input levels and its input common-mode range is sufficient to accommodate the large common-mode variations in the neural input signal. The simulated offset, sensitivity, and decision time of the comparator are about 1.8 mV, 0.28 mV, and 0.72 ns, respectively.

The utilized VGA and averaging filter are based on [7] and [8] with the confirmed performances. The CT $\Sigma\Delta$ modulator operates at 1.28 MHz sampling rate with an OSR of 64. The simulated output spectrum of the $\Sigma\Delta$ modulator with a -3.6 dBFS sinusoidal input signal is shown in Fig. 12. The resulting maximum signal-to-noise and distortion ratio (SNDR) is about 44.2 dB excluding the circuit noise. The achieved maximum SNDR is about 42.6 dB while considering the circuit noise. By integrating the power of the circuit noise within the desired bandwidth, the maximum SNDR is decreased about 1.6 dB compared to the case that the circuit noise has been neglected.
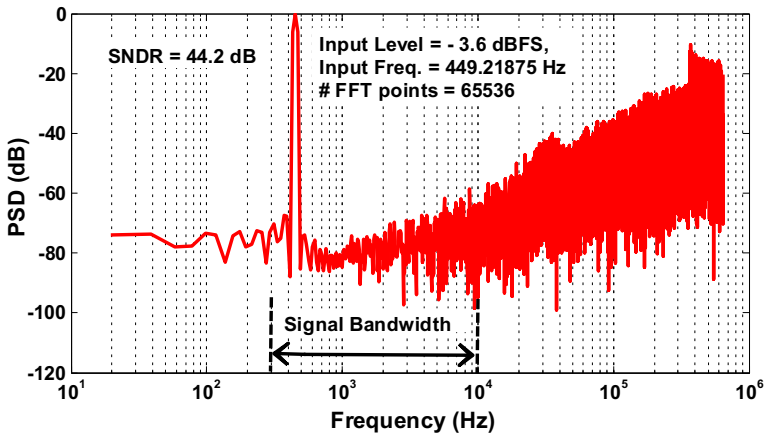
Fig. 12 Simulated power spectral density (PSD) of CT $\Sigma\Delta$ modulator (TT @ 27 °C) excluding the circuit noise
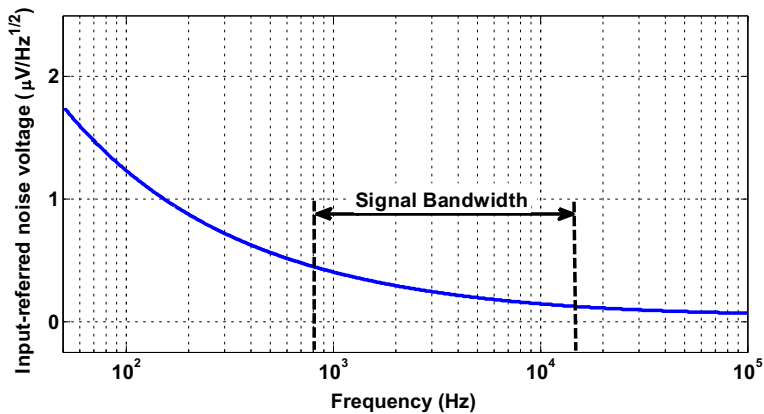

Fig. 13 Input-referred noise voltage of the simulated automatic AP detector

The utilized OTA in the integrator is designed to achieve the DC gain and unity-gain bandwidth (GBW) about 52 dB and 3.6 MHz, respectively. The -3 dB frequency of the simulated averaging filter is about 153 Hz, and it is realized with $C_S = 2$ pF, $R = 100$ kΩ with the current gain of $\beta = 1200$ ($A = 40$ and $B = 30$). A noise simulation is performed to obtain the input-referred noise voltage of the complete circuit. Figure 13 shows the simulated input-referred noise voltage. The thermal noise level is about 9.2 nV/Hz$^{1/2}$, and the noise integration from 300 Hz to 10 kHz gives an RMS noise voltage about 1.9 μV_{rms}. The input-referred RMS noise voltage at the output of the averaging filter is about 218 μV_{rms} which is much smaller than the level of the APs.

To evaluate the accuracy of the proposed AP detector, a 50 mV sinusoidal input signal with the frequency of 5 kHz (neural signal bandwidth is 10 kHz) is applied. Figure 14 shows the simulated output response. As it is clear, the threshold level is about 672 mV (172 mV superimposed on the common-mode voltage of 0.5 V)
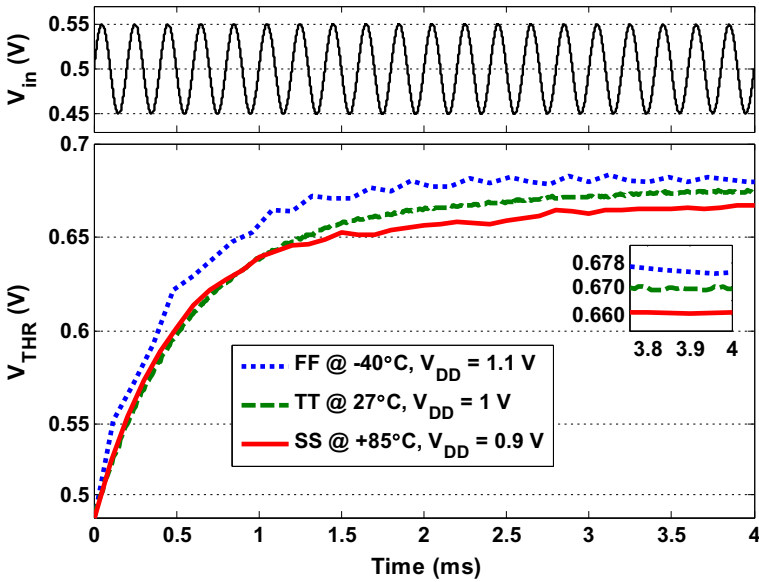
Fig. 14 Threshold level of simulated AP detector in different PVT cases
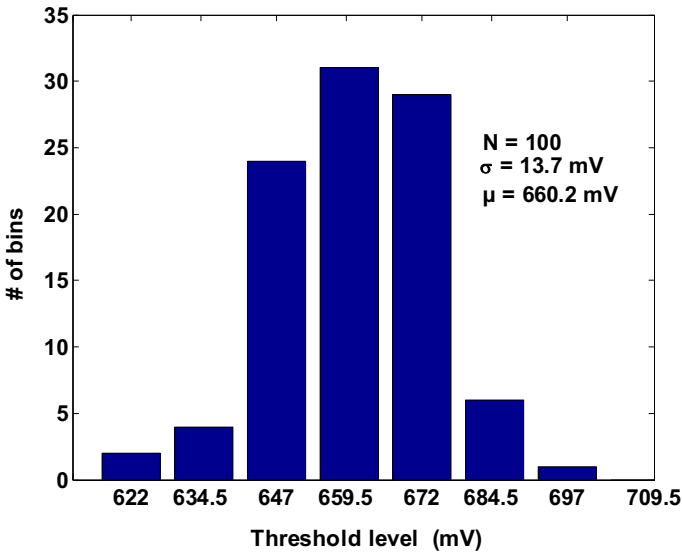

Fig. 15 Monte Carlo schematic simulation results of the automatic AP detector

which is equal to 4.8 times of the RMS of the input signal ($K = 4.8$). As mentioned in the introduction, the acceptable value for K is 3–7. Furthermore, the simulated output in different process corner cases, temperature variations and 10% power supply variations is also illustrated in Fig. 14. As it is seen, V_{THR} is about 672 mV in the typical process corner case and it is reduced to about 661 mV in the worst case. As a
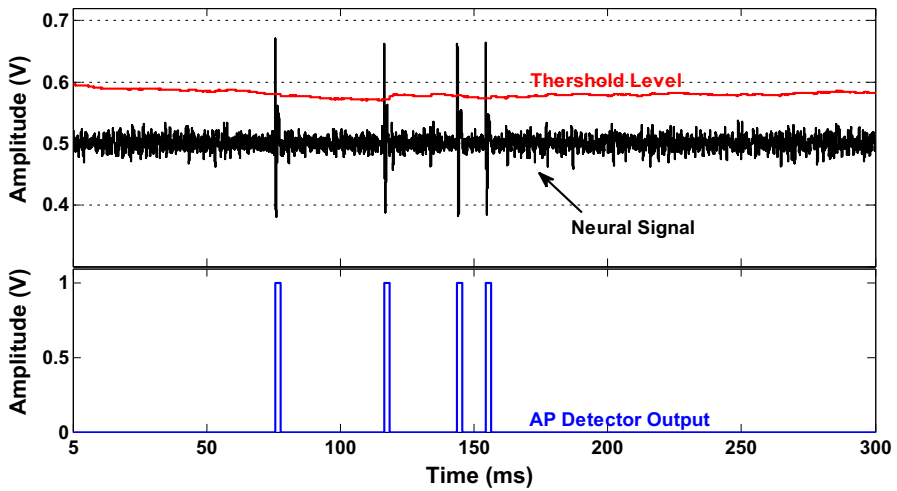
Fig. 16 Simulated operation of the proposed AP detector with high-level neural spikes
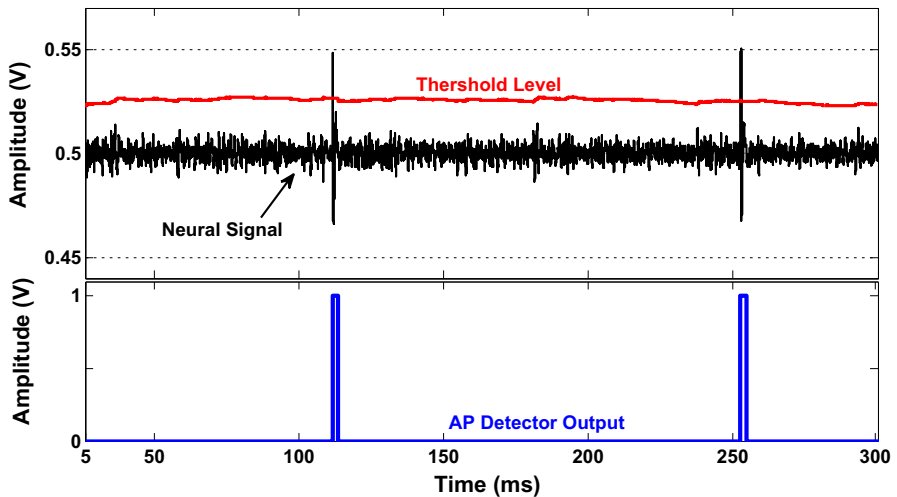

Fig. 17 Simulated operation of the proposed AP detector with low-level neural spikes

result, the maximum error of the output voltage is less than 11 mV in PVT variations. To evaluate the performance of the proposed circuit against the process variations and device mismatch, a Monte Carlo simulation is performed using the mismatch models of TSMC 90-nm CMOS process with 100 runs. As shown in Fig. 15, the performance degradation is negligible.

As mentioned before, since the AP detector is located after the multi-stage amplification and filtering, APs are adequately distinct from the background noise and the voltage ratio of the AP to the background noise almost remains constant in the AP detector. Nevertheless, the amplitude of the neural signal (AP and background noise) is unknown owing to the random distance between the electrodes and the correspond-
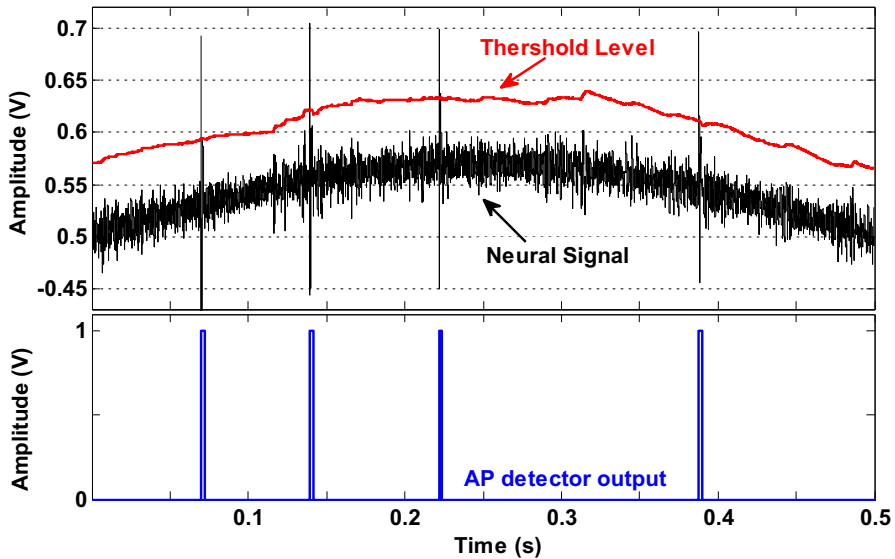
Fig. 18 Simulated operation of the proposed AP detector in the presence of large baseline variations

Table 1 Power and area breakdown of the simulated AP detector

	Divider	CT $\Sigma\Delta$ modulator and MDAC	Averaging filter	Comparator and logic gates
Power dissipation (μW)	2.5	5.8	3.2	0.3
Ratio to total power dissipation	21.2%	49.2%	27.1%	2.5%
Area (mm^2)	0.0016	0.0309	0.007	0.002
Ratio to total area	3.8%	74.5%	16.8%	4.9%

ing neurons. To evaluate the performance of the proposed automatic AP detector, two simulation results are provided by applying a real pre-recorded neural signal with different amplitudes. These signals have been intracortically recorded from the auditory cortex of a guinea pig with the sampling frequency of 20 kS/s. In the first simulation, the amplitude of AP is approximately 150 mV and the top trace in Fig. 16 shows a slice of this signal and the resulted threshold level, V_{THR}. The generated threshold level is $K = 4.8$ times larger than the RMS value of the input signal. Successful operation is observed from the circuit as shown in the down trace of Fig. 16. The second simulation is performed by the neural signal with an amplitude which is one-third smaller than the first simulation, and the result is shown in Fig. 17. The threshold-level V_{THR} is changed proportional to the new RMS value. A unique advantage of the proposed circuit is that it masks action potentials from affecting the threshold level.

Neural recording signals have a baseline variation due to local field potentials (LFPs) or mixing power line interference with the neural signal. This variation can cause some problems in AP detection. The effect of large common-mode voltage

Table 2 Performance comparison with several similar works

References	CMOS process (nm)	Domain	V_{DD} (V)	Power (μW)	Area (mm²)	Sub-V_{TH} biasing	AP detector type
IET ELL'11 [4][a]	180	Analog	1.8	47	–	No	Automatic
TNSARE'09 [9]	180	Analog	1.8	0.78	0.07	Yes	Automatic
WAMICON'13 [12][a]	130	Analog	0.7	56.5	0.014	No	Manual
ISCAS'13 [13]	180	Analog	1.8	1.5	0.03	Yes	Automatic
TBCAS'12 [17]	130	Analog	1.2	2.8	0.16	Yes	Manual
EMBC'13 [23]	130	Digital	–	85	6.17	No	–
TBCAS'16 [24]	65	Analog	0.7	0.04	0.03	Yes	Automatic
This work[a]	90	Analog	1	11.8	0.0415	No	Automatic

[a]Simulation results

Birkhäuser

variations has been evaluated by using 70 mV baseline variations which is intentionally added to the original neural signal. This simulation has been performed in order to observe how the threshold level tracks the relatively large common-mode variations in the baseline of the neural signal. Figure 18 shows the simulated operation of the circuit where the adaptive threshold level follows the baseline variations and the successful operation is observed.

The total power consumption of the simulated AP detector is about 11.8 μW. Table 1 summarizes the power consumption and active area of different parts of the simulated automatic AP detector. As it is seen, the CT $\Sigma\Delta$ modulator and the MDAC consume most of the power and area. The circuit-level simulation results of the proposed AP detector are summarized in Table 2 along with several recent similar works. The main features for comparison are the power consumption, active area, AP detector type (automatic or manual), and sub-V_{TH} biasing. It is worth mentioning that the subthreshold circuits are sensitive to the variations in process, power supply, and temperature (PVT). One of the main advantages of the proposed AP detector over the other schemes is avoiding the use of the devices biased in the subthreshold region. This helps to achieve more robust circuit behavior against the PVT variations. Although "automatic AP detector" is the term used for such circuits, a few of the reported circuits demonstrate dynamic tracking behavior of the generated threshold level.

5 Conclusion

An automatic AP detector circuit is presented for real-time neural recording systems. The AP detector employs an analog signal processing to adaptively generate the threshold level for AP detection. The RMS value of the neural signal is used to detect the AP in real time. The realization of the multiplier using a CT $\Sigma\Delta$ modulator with an MDAC reduces the power consumption and improves the resolution of the AP detector. Furthermore, the $\Sigma\Delta$ modulator can be shared with the ADC of the neural recording system, and hence, the power consumption and active area of the overall system can be reduced.

References

1. M.A. Al-Absi, A. Hussein, M. TaherAbuelma'atti, A low voltage and low power current-mode analog computational circuit. Circuits Syst. Signal Process. **32**(1), 321–331 (2013)
2. P. Amaral, J. Goes, N. Paulino, A. Steiger-Garção, An improved low-voltage low-power CMOS comparator to be used in high-speed pipeline ADCs. IEEE Int. Symp. Circuits Syst. **5**, 141–144 (2002)
3. M. Barati, M. Yavari, A power conversion chain with an internally-set voltage reference and reusing the power receiver coil for wireless bio-implants. Microelectron. J. **74**(4), 69–78 (2018)
4. S. Barati, A.M. Sodagar, Discrete-time automatic spike detection circuit for neural recording implants. Electron. Lett. **47**(5), 306–307 (2011)
5. C. Chen, J. Fan, X. Hu, Y. Hei, A low power, high performance analog front-end circuit for 1 V digital hearing aid SoC. Circuits Syst. Signal Process. **34**(5), 1391–1404 (2015)

6. M. Delgado-Restituto, A. Rodríguez-Pérez, A. Darie, C. Soto-Sánchez, E. Fernández-Jover, Á. Rodríguez-Vázquez, System-level design of a 64-channel low power neural spike recording sensor. IEEE Trans. Biomed. Circuits Syst. **11**(2), 420–433 (2017)

7. Q.-H. Duong, Q. Le, C.-W. Kim, S.-G. Lee, A 95-dB linear low-power variable gain amplifier. IEEE Trans. Circuits Syst. I Regul. Pap. **53**(8), 1648–1657 (2006)

8. G. Ferri, S. Pennisi, S. Sperandii, A low-voltage CMOS 1-Hz low-pass filter, in *IEEE International Conference on Electronics, Circuits and Systems (ICECS)* (1999), pp 1341–1343

9. B. Gosselin, M. Sawan, An ultra low-power CMOS automatic action potential detector. IEEE Trans. Neural Syst. Rehabil. Eng. **17**(4), 346–353 (2009)

10. R.R. Harrison, P.T. Watkins, R.J. Kier, R.O. Lovejoy, D.J. Black, B. Greger, F. Solzbacher, A low-power integrated circuit for a wireless 100-electrode neural recording system. IEEE J. Solid State Circuits **42**(1), 123–133 (2007)

11. Z. Hojati, M. Yavari, An NTF-Enhanced Incremental $\Sigma\Delta$ Modulator Using A SAR Quantizer. Integr. VLSI J. **55**(9), 212–219 (2016)

12. M. Jalalifar, G.-S. Byun, An ultra-low power spike detector for implantable biomedical systems, in *IEEE Wireless and Microwave Technology Conference (WAMICON)* (2013), pp 1–4

13. E. Koutsos, S.E. Paraskevopoulou, T.G. Constandinou, A 1.5 μW NEO-based spike detector with adaptive-threshold for calibration-free multichannel neural interfaces, in *IEEE International Symposium on Circuits and Systems (ISCAS)* (2013), pp 1922–1925

14. M.H. Maghami, A.M. Sodagar, M. Sawan, Versatile stimulation back-end with programmable exponential current pulse shapes for a retinal visual prosthesis. IEEE Trans. Neural Syst. Rehabil. Eng. **24**(11), 243–1253 (2016)

15. R.M. Rangayyan, *Biomedical Signal Analysis: A Case-Study Approach* (Wiley, Hoboken, 2002)

16. S.U. Rehman, A.M. Kamboh, A CMOS micro-power and area efficient neural recording and stimulation front-end for biomedical applications. Circuits Syst. Signal Process. **34**(6), 1725–1746 (2015)

17. A. Rodriguez-Perez, J. Ruiz-Amaya, M. Delgado-Restituto, A. Rodriguez-Vazquez, A low-power programmable neural spike detection channel with embedded calibration and data compression. IEEE Trans. Biomed. Circuits Syst. **6**(2), 87–100 (2012)

18. C. Sawigun, S. Thanapitak, A 0.9-nW, 101-Hz, and 46.3-μVrms IRN low-pass filter for ECG acquisition using FVF biquads. IEEE Trans. Very Large Scale Integr (VLSI) Syst 1–9 (2018)

19. R. Schreier, G.C. Temes, *Understanding Delta-Sigma Data Converters* (Wiley/IEEE Press, Hoboken, 2005)

20. S. Tao, A. Rusu, A power-efficient continuous-time incremental sigma-delta ADC for neural recording systems. IEEE Trans. Circuits Syst. I Regul. Pap. **62**(6), 1489–1498 (2015)

21. S. Tao, A. Rusu, A comparative design study of continuous-time incremental sigma-delta ADC architectures. Int. J. Circuit Theory Appl. **44**(12), 2147–2163 (2016)

22. S. Thanapitak, C. Sawigun, A subthreshold buffer-based biquadratic cell and its application to biopotential filter design. IEEE Trans. Circuits Syst. I Regul. Pap. **65**(9), 774–2783 (2018)

23. T. Wu, Z. Yang, A multichannel integrated circuit for neural spike detection based on EC-PC threshold estimation, in *Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)* (2013), pp 779–782

24. E. Yao, Y. Chen, A. Basu, A 0.7 V, 40 nW compact, current-mode neural spike detector in 65 nm CMOS. IEEE Trans. Biomed. Circuits Syst. **10**(2), 309–318 (2016)