Digital Calibration of Amplifier Finite DC Gain and Gain Bandwidth in MASH $\Sigma\Delta$ Modulators

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***Abstract*—In this brief, a digital background calibration technique is proposed to improve the resolution of discrete-time multistage noise-shaping (MASH) sigma–delta ($\Sigma\Delta$) modulators. The circuit imperfections of switched-capacitor discrete-time integrators (DTIs) degenerate the modulator output resolution, particularly in MASH structures, due to the quantization noise leakage of the early stages at the modulator output. An accumulative error model is proposed to define the errors induced by the limited dc gain and gain bandwidth (GBW) of DTIs as a function of their outputs. Compensating for these errors is possible through two steps, which are the DTI output digital approximation and adaptive filter correction. To identify the adaptive filter parameters, 1-b pseudo-random noise test signals are injected to the inputs of the DTIs. Then, the effect of these test signals is investigated by using a correlation-based least-mean-square algorithm. Simulation results confirm the effectiveness of the proposed method to eliminate the errors associated with the finite dc gain and GBW. Consequently, relaxed amplifiers with lower power consumption can be used.**

***Index Terms*—Digital background calibration, finite gain bandwidth (GBW), limited dc gain, multistage noise-shaping (MASH) sigma–delta ($\Sigma\Delta$) modulators, switched-capacitor circuits.**

I. Introduction

SIGMA–DELTA ($\Sigma\Delta$) modulators, by benefiting from the oversampling and noise shaping, make a better tradeoff between the sampling speed and signal-to-noise ratio (SNR) compared to the Nyquist-rate analog-to-digital converter (ADC) [1]. To achieve higher resolution, cascaded structures offer a robust stable alternative instead of using high-order single-loop $\Sigma\Delta$ topologies. However, they are very sensitive to the analog circuit imperfections since they rely on the precise transfer function matching of the analog and digital sections in order to avoid the leakage of prior stages' quantization noise. Fabricating wideband high-resolution $\Sigma\Delta$ modulators is more challenging, particularly where low supply voltages should be used, because they require high dc gain operational amplifiers with a large gain bandwidth (GBW) product.

To overcome this problem, calibration techniques are usually applied for the compensation. Although calibration techniques are frequently used in pipelined ADCs to handle both linear and nonlinear memoryless errors [2], in $\Sigma\Delta$ modulators a general approach to compensate for the circuit nonidealities in the presence of the integrator memory has yet to be developed.

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Most of the known works are focused on the multibit digital-to-analog converter (DAC) linearization [3]. Some other works address the problem of amplifier limited dc gain by adding analog elements, such as a tunable capacitor [4] or an extra unity gain buffer [5], to the conventional integrator. The accuracy of these analog calibration methods is confined to the accuracy of the added analog element. Thus, they are not able to omit the limited gain effects entirely. As mentioned before, some circuit imperfections, including the amplifier limited dc gain, lead to the quantization noise leakage in multistage noise-shaping (MASH) structures. To decrease the noise leakage, the parameters of digital filters are changed to match the analog circuit in [4] and [6]. Since these calibration schemes are performed in the digital domain, their added area and power consumption are lower than that of the analog calibration techniques.

The calibration methods in [3]–[6] utilize suitable amplifiers with small settling errors. However, some other modulators take advantage of using the amplifier swing reduction architectures to relax the settling requirements [7]. In [8], an adaptive fifth-order polynomial digital filter is applied to a MASH 2-2 modulator to remove the first stage settling errors. Not operating in the background and ignoring the second stage settling errors are the main drawbacks of this method.

In this brief, an accumulative error model is proposed to investigate the effects of both limited dc gain and GBW in discrete-time integrators (DTIs). Also, a digital calibration technique is utilized to compensate for the errors induced by these nonidealities in a MASH 2-2 $\Sigma\Delta$ modulator. This calibration technique operates in the background and corrects both stages of the MASH modulator.

This brief is organized as follows. Section II presents the proposed accumulative error model based on the conventional amplifier limited dc gain and settling models. Section III describes the proposed digital calibration technique. The behavioral simulation results of a MASH 2-2 $\Sigma\Delta$ modulator are provided in Section IV and, finally, Section V concludes this brief.

II. Modeling of Circuit Imperfections

In this section, an accumulative error model is derived from two conventional models. By using this new model, the errors caused by the amplifier limited dc gain and GBW can be stated as a function of DTIs' outputs.

A. Amplifier Finite DC Gain

A conventional switched-capacitor DTI is shown in Fig. 1, where A_v is the amplifier dc gain and C_S, C_I, and C_P are the sampling, integrating, and parasitic capacitors, respectively. In practice, the amplifier cannot provide a good virtual ground and its inverting input has a voltage of $-v_o/A_v$. As a result,

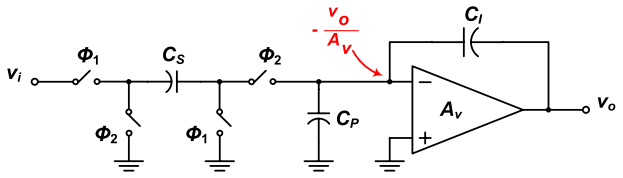

Fig. 1. Conventional switched-capacitor integrator considering the effect of amplifier finite dc gain.

the integrator transfer function (ITF) deviates from its ideal form. The effects of amplifier finite dc gain in a conventional switched-capacitor DTI can be modeled as [1]

$$ITF(z) = \frac{C_S}{C_I}\frac{\alpha z^{-1}}{1-\beta z^{-1}} \tag{1}$$

where the signal independent constants α and β are

$$\alpha = \frac{A_v C_I}{(A_v+1)C_I+C_S+C_P}, \quad \beta = \frac{(A_v+1)C_I+C_P}{(A_v+1)C_I+C_S+C_P}. \tag{2}$$

The ideal ITF can be derived from (1) and (2) by assuming infinite gain for the amplifier ($\alpha = \beta = 1$).

B. GBW and Slew Rate

Considering the settling time of the amplifier, the integrator output can be stated as

$$v_o(nT_s) = v_o\left((n-1)T_s\right) + g\left(v_i\left((n-1)T_s\right)\right) \tag{3}$$

where T_s is the period of the sampling frequency. f_s. $g(.)$ is specified by analog parameters as

$$g(x) = \begin{cases} x(1-e^{-t_s/\tau}) & |x| \le \tau\zeta \\ x - \mathrm{sgn}(x)\tau\zeta e^{((|x|/\tau\zeta)-((t_s/\tau\zeta)-1)} & \tau\zeta|x| \le (\tau+t_s)\zeta \\ \mathrm{sgn}(x)\zeta, t_s & (\tau+t_s)\zeta < |x|. \end{cases} \tag{4}$$

In these equations, t_s is the total available settling time, τ is the integrator's settling time constant, and ζ is the slew rate of the amplifier [9]. According to (3), the parameter x is equal to $v_i((n-1)T_s)$. The relation between the GBW and τ is given by

$$\tau = \frac{1}{f.GBW} \tag{5}$$

where f is the feedback factor of the amplifier. The limited dc gain not only introduces a steady-state error as described in the previous subsection, but also affects the transient waveform through τ. By considering (1) and (3), we have

$$v_o(nT_S) = \beta v_o\left((n-1)T_S\right) + g\left(\alpha v_i\left((n-1)T_S\right)\right). \tag{6}$$

The block diagram shown in Fig. 2(a) describes (6) [10]. If the integrator is slow enough (τ is high enough) to ensure that $|\alpha v_i|$ is less than $\tau\zeta$, the output would be a mere exponential curve without any slewing. Therefore, the relation (6) can be modified as

$$v_o(nT_S) = \beta v_o\left((n-1)T_S\right) + \lambda v_i\left((n-1)T_S\right) \tag{7}$$

where the parameter λ is also a signal-independent constant and is defined as

$$\lambda = \alpha(1-e^{-t_S/\tau}). \tag{8}$$

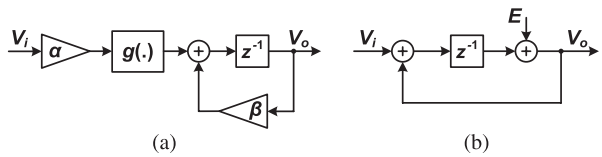

Fig. 2. (a) Conventional and (b) proposed accumulative error modeling of the amplifier finite dc gain and limited GBW.

C. Accumulative Error Model

Another approach is to presume that the integrator is ideal and the errors, induced by the amplifier finite dc gain, GBW, and slew rate, are added to the output as shown in Fig. 2(b). In this case, the output of the integrator is given by

$$v_o(nT_S) = v_o\left((n-1)T_S\right) + v_i\left((n-1)T_S\right) + e(nT_S). \tag{9}$$

By considering the output equation of a slow integrator in (7) and the accumulative error model presented in (9), the amount of error added to the integrator output in each sampling step can be obtained as

$$e(nT_S) = (\beta-1)v_o\left((n-1)T_S\right) + (\lambda-1)v_i\left((n-1)T_S\right). \tag{10}$$

By using (7) to substitute v_i in (10), we have

$$e(nT_S) = \frac{\lambda-1}{\lambda}v_o(nT_S) + \frac{\beta-\lambda}{\lambda}v_o\left((n-1)T_S\right). \tag{11}$$

Thus, when the amplifier is slow enough, the accumulative error can be stated as a function of the current and previous outputs of the integrator. Using this model gives a better perspective on the limited dc gain and GBW effects.

III. Proposed Calibration Technique

In this section, the proposed calibration technique, which is used to compensate the amplifier limited dc gain and GBW in a discrete-time MASH modulator, is presented. According to (11), the error of an integrator is related to its analog output values. Since these values are not accessible in the digital domain, the first step of the calibration is to digitally approximate the integrators' outputs. In the next step, the amount of error added to each integrator is estimated. Finally, with respect to the governing transfer functions, the estimated errors are subtracted from the digital output. Since the exact values of coefficients used in (11) are unknown, digital adaptive filters are utilized to estimate the amount of error added to each integrator output. To identify these coefficients, the injected known pseudorandom test signal and least mean square (LMS) algorithm are utilized.

Fig. 3 shows the structure of the MASH 2-2 $\Sigma\Delta$ modulator. The proposed accumulative error model is used to describe the integrators' behavior. The calibration technique is applied to this modulator because MASH structures are more sensitive to the analog circuit imperfections. The first stage is a second-order feedforward structure with a unity signal transfer function (STF). The input of the first integrator, being $X - Y_1$, shows little signal swing. Moreover, X changes slowly in time because it is oversampled. The second stage is a feedback structure. The gain blocks are located before the second stage integrators to decrease their input and output swing. Hence, the integrators' inputs are small enough to ensure that the condition $|\alpha v_i| < \tau\zeta$ is valid and, thus, their outputs do not slew. Also, class AB

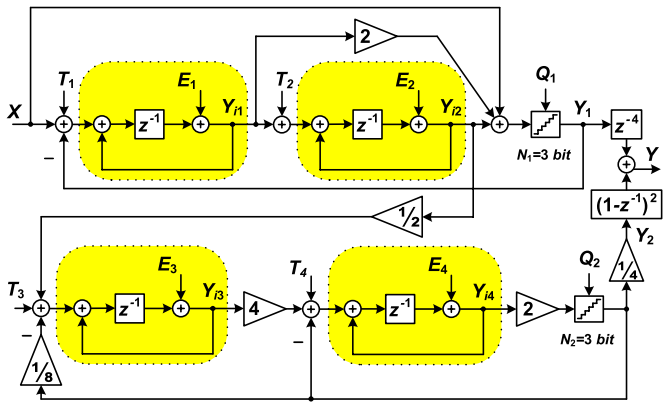

Fig. 3. MASH 2-2 ΣΔ modulator.

amplifiers with large slew rate can be used in the realization of the integrators to further relax this condition.

Two 3-b quantizers are used in each modulator stage. The gain block before the second stage quantizer is realized by the reference voltage scaling. T_1, T_2, T_3, and T_4 are the pseudorandom test signals that are injected to the input of the integrators.

A. Digital Approximation of Integrator's Output

As shown in Fig. 3, Y_1 and Y_2 are the stages' outputs; along with the injected test signals, they are available digitally. Moreover, Y_{i1}, Y_{i2}, Y_{i3}, and Y_{i4} are the integrators' analog outputs. Suppose that Y_{d1}, Y_{d2}, Y_{d3}, and Y_{d4} are their digital estimation counterparts. To obtain a suitable estimation for each integrator output, an appropriate set of known available digital signals should be chosen. It can be shown that

$$Y_2(z) = \frac{1}{4}\left[2Y_{i4}(z) + Q_2(z)\right]. \tag{12}$$

Therefore, the estimation of the last integrator output, Y_{d4}, can be obtained as

$$Y_{d4}(z) = 2Y_2(z) = Y_{i4}(z) + \frac{1}{2}Q_2(z). \tag{13}$$

The right side of (13) consists of two components. The first term is the desired analog signal, while the second term is the approximation error. As will be shown later, because of the different shaping order of each integrator's error at the modulator output, the output estimation of the earlier integrators needs to be more accurate. Hence, Y_{d4} has an acceptable accuracy. The third integrator output can be expressed as

$$Y_{i3}(z) = \frac{(1-z^{-1})}{4z^{-1}}Y_{i4}(z) - \frac{E_4(z)}{4z^{-1}} - \frac{T_4(z)}{4} + Y_2(z) \tag{14}$$

where E_4 is the last integrator output error. Since the analog value of E_4 is not accessible, its digital approximation (E_{d4}), which is produced during the calibration, would be used instead. By considering the relation between Y_{i4} and Y_2 in (13), the digital estimation of the third integrator output can be obtained from (14) as

$$\begin{aligned} Y_{d3}(z) &= \frac{(1+z^{-1})}{2z^{-1}}Y_2(z) - \frac{E_{d4}(z)}{4z^{-1}} - \frac{T_4(z)}{4} \\ &= Y_{i3}(z) + \frac{(1-z^{-1})}{8z^{-1}}Q_2(z). \end{aligned} \tag{15}$$

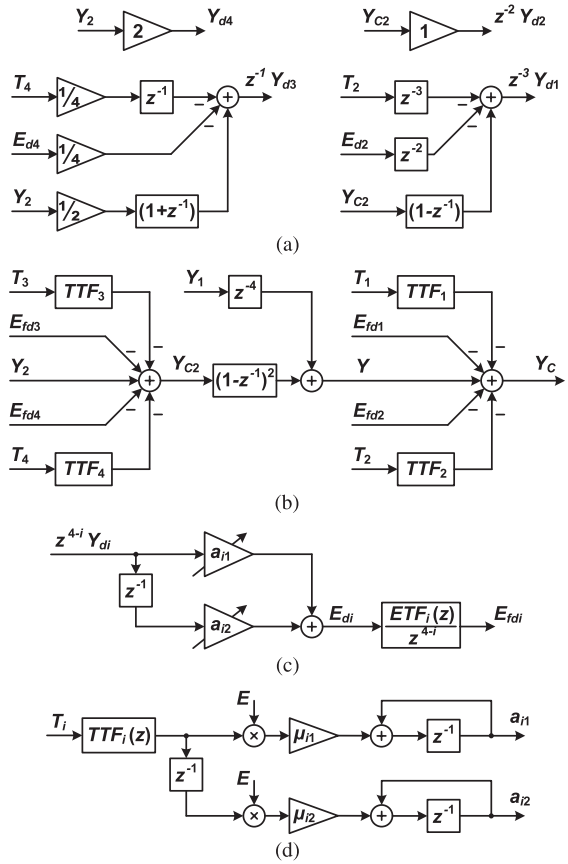

Fig. 4. Block diagram of (a) integrator output approximation, (b) modulator correction, (c) error estimation, and (d) error parameter identification.

Furthermore, since (15) is not causal, generating Y_{d3} is practically impossible. Therefore, $z^{-1}Y_{d3}$ is alternatively generated. It will be shown that adding an extra delay is not a problem. After estimating the outputs of the second-stage integrators, their errors are removed by using adaptive filters; hence, the corrected second stage output is provided. Since the output of the second integrator is the input of the second stage modulator, it can be stated that

$$Y_{d2}(z) = \frac{1}{z^{-2}}Y_{C2}(z) = Y_{i2}(z) + \frac{(1-z^{-1})^2}{4z^{-2}}Q_2(z) \tag{16}$$

where Y_{C2} is the second stage corrected output. Similarly, the first integrator output can be expressed as

$$Y_{i1}(z) = \frac{(1-z^{-1})}{z^{-1}}Y_{i2}(z) - \frac{E_2(z)}{z^{-1}} - T_2(z). \tag{17}$$

Hence, an acceptable approximation of Y_{i1} is obtained as

$$\begin{aligned} Y_{d1}(z) &= \frac{(1-z^{-1})}{z^{-3}}Y_{C2}(z) - \frac{E_2(z)}{z^{-1}} - T_2(z) \\ &= Y_{i3}(z) + \frac{(1-z^{-1})^3}{4z^{-3}}Q_2(z). \end{aligned} \tag{18}$$

Just like Y_{d3}, some extra delays are needed to generate Y_{d1} and Y_{d2}. In general, $z^{4-i}Y_{di}$ is generated instead of Y_{di}. Y_{d1} also requires E_2, which will be substituted with its digital approximation E_{d2}. Considering (13) to (18), the estimation error of the earlier integrators is smaller than the others because of the higher order shaping of Q_2. Fig. 4(a) shows the digital realization of (13), (15), (16), and (18).

B. Digital Adaptive Correction

The next step after the approximation of the integrators' outputs is to estimate the integrators' errors using (11). To accomplish this, digital adaptive filters are used. According to (11), the adaptive filter's transfer function is

$$E_{di}(z) = a_{i1}Y_{di}(z) + a_{i2}Y_{di}(z)z^{-1}, \quad i = 1, 2, 3, 4 \tag{19}$$

where a_{i1} and a_{i2} are the digital approximations of $(\lambda - 1)/\lambda$ and $(\beta - \lambda)/\lambda$, respectively. The integrator output estimation Y_{di} is the adaptive filter input, and the digital estimation of E_i, E_{di}, is its output. The subscript i indicates that the parameters are associated with the ith integrator. After estimating the error of integrators, Y_{C2} is produced by correcting the second stage output. The correction is made by subtracting the estimated digital errors from the modulator output along with the injected test signals. To accomplish this, it is necessary to know the transfer function from the signals to the point they should be subtracted. The uncorrected output of the second stage modulator, considering all inputs, is

$$\begin{aligned} Y_2(z) = {} & z^{-2}Y_{i2}(z) + 2z^{-2}T_3(z) + \frac{z^{-1}(1 - z^{-1})}{2}T_4(z) \\ & + 2z^{-1}E_3(z) + \frac{(1-z^{-1})}{2}E_4(z) + \frac{(1-z^{-1})^2}{4}Q_2(z) \end{aligned} \tag{20}$$

where the expressions placed before the test and error signals are their transfer functions (TTFs and ETFs). With regard to these transfer functions, the second stage corrected output is

$$\begin{aligned} Y_{C2}(z) = {} & Y_2(z) - TTF_3(z)T_3(z) - TTF_4(z)T_4(z) \\ & - ETF_3(z)E_{d3}(z) - ETF_4(z)E_{d4}(z). \end{aligned} \tag{21}$$

Correcting Y_2 is shown in Fig. 4(b). Y_{C2} is used in the first stage's output approximations and the modulator output. The second stage errors would be removed completely if the estimated errors are exactly equal to their analog counterparts. However, in practice, due to the approximation errors, small quantities of errors still remain at the output. The same procedure is performed to compensate for the errors of the first-stage modulator. The modulator output before correcting the first stage errors can be stated as

$$\begin{aligned} Y(z) = {} & z^{-4}X(z) + z^{-4}T_1(z) + z^{-3}(1 - z^{-1})T_2(z) \\ & + z^{-3}E_1(z) + z^{-2}(1-z^{-1})E_2(z) + \frac{(1-z^{-1})^4}{4}Q_2(z). \end{aligned} \tag{22}$$

Equation (22) specifies the TTF and ETF of the first stage signals. The residual error in Y_{C2} is neglected. The corrected final modulator output is

$$\begin{aligned} Y_C(z) = {} & Y(z) - TTF_1(z).T_1(z) - TTF_2(z).T_2(z) \\ & - ETF_1(z).E_{d1}(z) - ETF_2(z).E_{d2}(z) \\ = {} & z^{-4}X(z) + \frac{(1 - z^{-1})^4}{4}Q_2(z). \end{aligned} \tag{23}$$

Correcting the modulator output by subtracting the injected test signals and estimated errors is shown in Fig. 4(b). As indicated in (20), the errors of the second stage integrators are shaped at the output of the second stage. In addition, the residual error after the calibration will be further shaped by passing through the digital filter placed after this stage. Thus, according to (22), the error of earlier integrators is shaped by the lower order. Hence, the output approximation error of the later integrators can be higher. Considering (20) and (22), the effects of the limited dc gain and GBW on the modulator's outputs can be better identified by the proposed accumulative error model compared to the conventional models.

TABLE I
INTEGRATORS' PARAMETERS

	A_v (dB)	GBW (MHz)	τ (ns)	α	λ	β	$(\lambda\text{-}1)/\lambda$	$(\beta\text{-}\lambda)/\lambda$
1st Int.	30	100	3.18	0.941	0.745	0.970	-0.342	0.302
2nd Int.	30	100	3.18	0.941	0.745	0.970	-0.342	0.302
3rd Int.	30	100	2.39	0.966	0.847	0.996	-0.181	0.177
4th Int.	30	250	3.18	0.864	0.684	0.891	-0.462	0.302

Fig. 4(c) illustrates the digital adaptive filter, which estimates the error of an integrator and applies its transfer function. The same number of delays, which were used to implement the integrator output estimation, is removed from the ETF of the corresponding error so that the filtered error estimation E_{fdi} is produced. This is a finite impulse response filter since delayed forms of its output (E_{fdi}) are not used as its input.

C. Filter Parameter Identification

The exact values of analog coefficients in (11) are unknown since the process, voltage, and temperature variations change the circuit parameters. Therefore, an LMS algorithm is utilized to estimate these parameters. A two-level known pseudo-random test signal, with almost a constant power spectral density (PSD), is injected to the input of each integrator. This signal is added to the integrator by an extra switched-capacitor branch. The capacitor value and the amount of voltage, which passes through it, are specified by the amplitude of the test signal. If the test signal amplitude is small, the convergence time would be increased; if it is large, the dynamic range would be decreased. Since the test signal and the integrator error are added to the output in a similar way in each integrating phase, minimizing the test signal at the final output reduces the integrator's error [6]. The LMS algorithm helps the digital coefficients to gradually reach their final values by investigating the correlation between the injected signals and the outputs. The digital coefficients of (19) are updated as

$$\begin{aligned} a_{i1}^{m+1} &= a_{i1}^{m} + \mu_{i1}\left(\sum_{n=mk+1}^{(m+1)k} e[n](t_i * ttf_i)[n]\right) \\ a_{i2}^{m+1} &= a_{i2}^{m} + \mu_{i2}\left(\sum_{n=mk+1}^{(m+1)k} e[n](t_i * ttf_i)[n\text{–}1]\right), \quad i = 1, 2, 3, 4 \end{aligned} \tag{24}$$

where the superscripts $m + 1$ and m specify the new and old coefficients, respectively, and k is the summation length. μ_{i1} and μ_{i2} are the LMS step sizes. The LMS error signal $e[n]$ is replaced with the corrected outputs that, for the adaptive filters correcting the first and second stages, are $y_c[n]$ and $y_{c2}[n]$, respectively. Fig. 4(d) describes (24). Since the second-stage corrected output is needed to estimate the first-stage integrators' outputs, a variable step-size LMS is utilized for the second stage to reduce the convergence time.

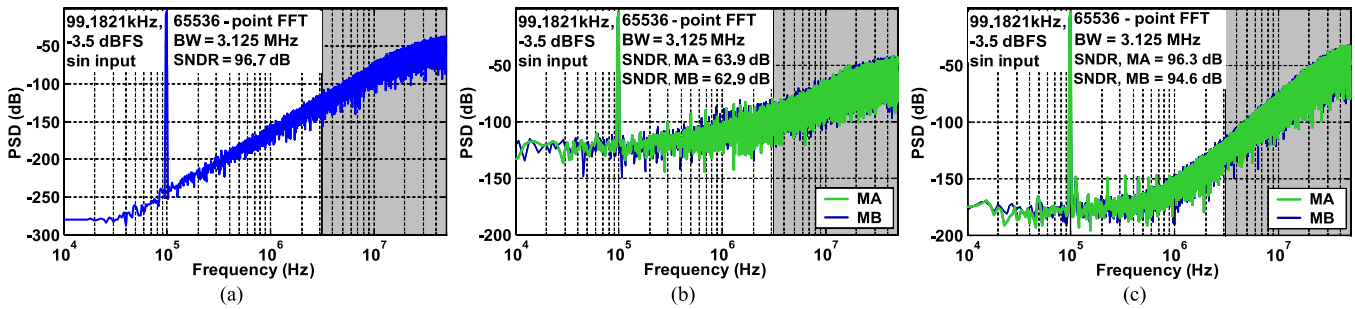

Fig. 5. Simulated output PSD of (a) ideal modulator, (b) modulator with amplifier limited dc gain and GBW, and (c) calibrated modulator.

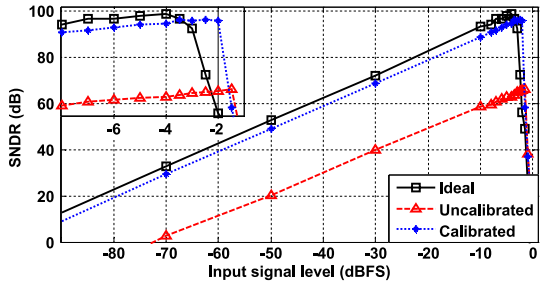

Fig. 6. Simulated SNDR versus the input amplitude.

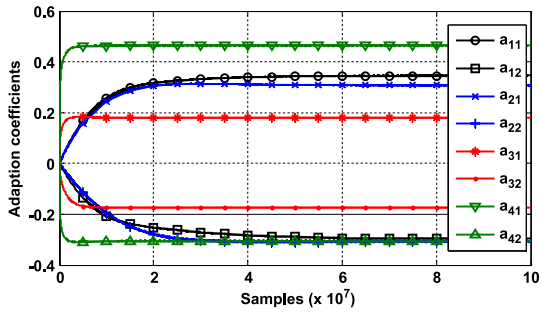

Fig. 7. Convergence of the adaptive filter parameters.

IV. Simulation Results

In this section, to provide behavioral simulation results of MASH 2-2 in MATLAB, two models for integrators, named model A (MA) and model B (MB), are obtained from [10] and [11], respectively. The sampling frequency and oversampling ratio are 100 MHz and 16. The input is a 99.182129-kHz sinusoidal signal. The integrators' parameters are given in Table I. Since the gain of the fourth integrator is larger, its feedback factor α and β are smaller compared to that of the other integrators. Thus, to avoid very large errors, its GBW is chosen to be higher.

Fig. 5 illustrates the PSD of the simulated modulator. The output spectrum is generated by a 2^{16}-point fast Fourier transform. The magnitude of the input signal is -3.5 dBFS. Fig. 5(a) illustrates the PSD of the ideal modulator, which has a 96.7-dB signal-to-noise and distortion ratio (SNDR). After considering nonideal effects using MA and MB, the SNDR drops to 63.9 and 62.9 dB, respectively [see Fig. 5(b)]. Applying the proposed method leads to the PSD of calibrated output in Fig. 5(c), which has 96.3- and 94.6-dB SNDRs for MA and MB, respectively. Hence, the resolution is increased by more than 30 dB. Fig. 6 illustrates the modulator's SNDR versus the input signal amplitude using MA. The calibrated curve drops slightly after the ideal curve since the integrators' outputs have less swing in the calibrated modulator. The convergence of adaptive filter parameters is shown in Fig. 7. To achieve the highest possible resolution, the adaptive parameters are chosen to be small. This leads to a convergence after about 70 M samples, which is almost the same as [6]. This work also addresses the errors induced by the limited GBW and the second stage's errors and needs less coefficients per integrator compared to [6]. Considering a 0.5% mismatch for the first test signal's capacitor and 1% for other test signals' capacitors, the SNDR is equal to 94 dB.

V. Conclusion

In this brief, a digital background calibration technique is proposed to compensate for the effects of the amplifier limited dc gain and GBW in MASH ΣΔ modulators. To describe the effect of these nonidealities at the integrator's output, an accumulative error model is presented. The next digital blocks estimate the amount of errors and remove them from the modulator output. According to the simulation results, the modulator SNDR is significantly improved and, hence, relaxed amplifiers with less power consumption can be used.

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