Journal of Circuits, Systems, and Computers
Vol. 21, No. 4 (2012) 1250033 (10 pages)

DOI: 10.1142/S0218126612500338

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A VERY LOW NOISE WIDEBAND CLASS-C CMOS LC VCO*

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Received 16 October 2011
Accepted 23 November 2011

In this paper, a new class-C voltage-controlled oscillator (VCO) is presented. In the proposed VCO, the tail capacitor of the conventional class-C oscillator is dislocated from the source of the cross-coupled transistors to their gate to achieve a rail-to-rail output swing. This improves the phase noise by 2.9 dB compared to the conventional class-C one. Besides, a new switching scheme is presented in the switched capacitor bank used for coarse tuning of the proposed VCO to lower the on resistance of the switches as well as to reduce the parasitic capacitors. This wide tuning range class-C VCO is designed in a 0.18 μm CMOS technology. It achieves a -125.3 dBc/Hz phase noise at 1 MHz offset from a 2.2 GHz carrier frequency while covering a wide tuning range from 1.82 to 2.65 GHz and consuming 3.5 mW power from a single 0.9 V power supply.

Keywords: Class-C VCO; frequency tuning range; phases noise.

1. Introduction

Interest in utilization of transceivers capable to operate at different frequencies has been widely increased due to the thriving development of the wireless standards in recent years. Oscillators, as an essential building block of the communication systems, are not excepted from this rule. Wide tuning range, low phase noise and power consumption, associated with small chip area are the main requirements in designing an oscillator. Inductance-capacitance (LC) oscillators have shown better noise performance compared to ring oscillators and are extensively used for designing wide band voltage-controlled oscillators (VCOs) in wireless radio frequency applications.[1–3]

The conventional class-C topology is generally recognized to improve the phase noise performance and provide a fully differential output.[4] In a typical class-C oscillator two features have been exploited together to optimize the phase noise. The

*This paper was recommended by Regional Editor Piero Malcovati.

first feature is a tail capacitor making the conduction duration of the switching transistors be much lower than half of the oscillation period, i.e., the current waveforms are made of tall and narrow pulses. The second feature is a bias network which allows the voltage swing at the drains grows to an adequate level and consequently reduces the phase noise. However, since the tail capacitor limits the output swing, the phase noise would not reach its minimum value.

In this paper, we overcome this drawback by dislocating the tail capacitor from the source of the cross-coupled transistors to their gate resulting in a rail to rail output swing which improves the phase noise by 2.9 dB compared to the conventional class-C oscillator. This design presents a new binary weighted capacitor bank to increase the tuning range as well.

The paper is organized as follows. In Sec. 2, the proposed high swing class-C VCO is presented. The circuit level simulation results are provided in Sec. 3. Finally, Sec. 4 concludes the paper.

2. Proposed VCO Architecture

2.1. *Proposed high swing class-C VCO*

It is generally recognized that maximizing the output swing of an oscillator remarkably decreases the phase noise.[5] However, in the RC biased class-C topology proposed in Ref. 4, the output swing is not permitted to switch rail-to-rail due to the presence of a tail capacitor and a current source. To overcome this drawback, the tail current source is omitted and a current mirror is used to bias the oscillator as shown in Fig. 1. Besides, the tail capacitor is moved from the source to the gate of M_1 and M_2 to build the class-C operation. In this figure, the diode connected transistors create a low-impedance biasing network at the cross-coupled transistors' gate and lead to the elimination of resistors of conventional RC-biased class-C oscillator.

To increase the output swing of the conventional class-C VCO, the main transistors' gates are biased at a voltage lower than that of the power supply. Since no tail capacitor is used in this architecture, M_1 and M_2 are allowed to switch rail-to-rail and therefore the output voltage swing is maximized which reduces the phase noise. Furthermore, M_1 and M_2 experience deep turn-off as their gates reach zero voltage. This state is desired to eliminate all unused active devices when they are off and consequently reduce the noise sources of the circuit. Additionally, the proposed high-swing oscillator allows the use of smaller power supplies. The current waveform of M_1 and M_2 for this class-C VCO is shown in Fig. 2. As is seen the drain currents of M_1 and M_2 are as narrow and tall pulses instead of being square waveforms indicating the class-C operation of the proposed VCO.

As shown in Figs. 3 and 4, increasing the current in both VCOs, presented in Ref. 4 and this paper, results in the enhancement of the output swing values and improvement of the phase noise. On the other hand, when the oscillator enters into

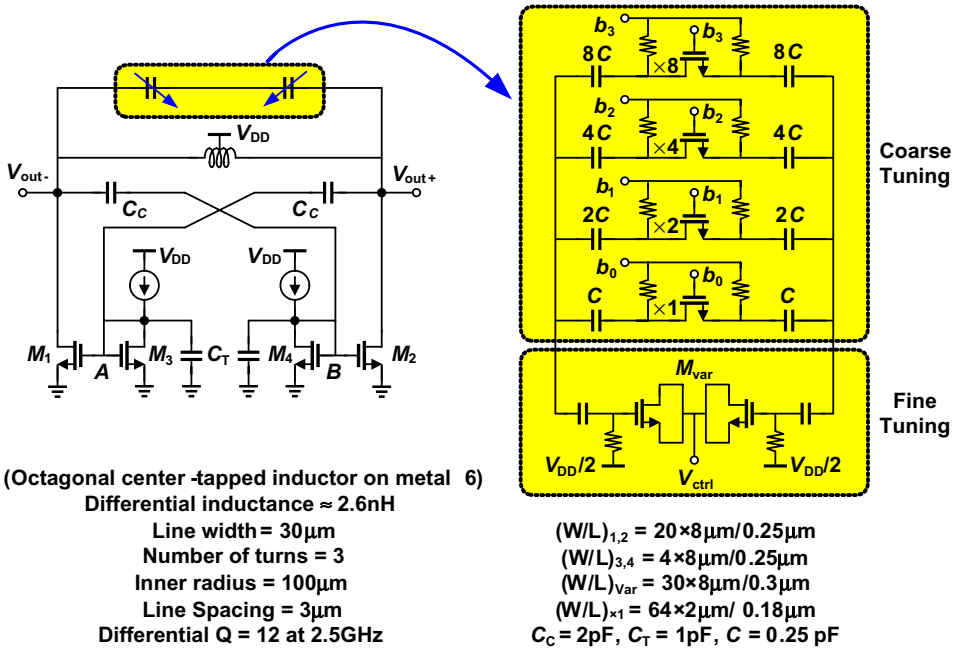


Fig. 1. Proposed class-C VCO.

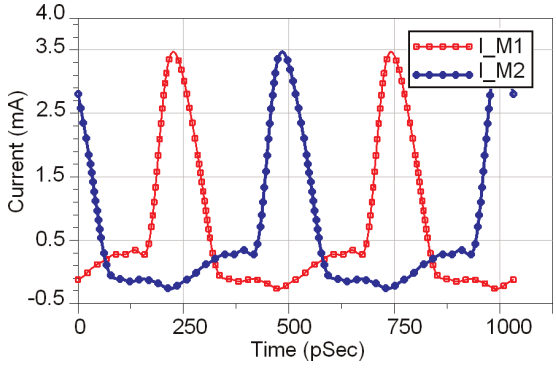


Fig. 2. Drain currents of M_1 and M_2.

the voltage-limited region, even though the output swing is increased, the phase noise is not decreased.[5] Therefore, operating of VCO in this region is not desirable because it is just a waste of power. However, in the presented topology, higher output swing can be achieved before going into the voltage-limited region. Thus, the proposed VCO improves the phase noise by 2.9 dB compared to the conventional class-C VCO at the cost of higher power consumption.

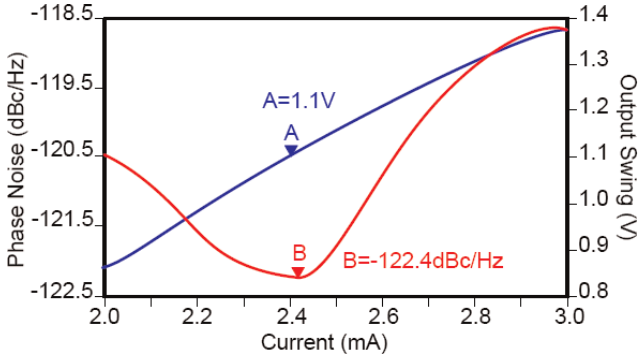


Fig. 3. Phase noise and amplitude of VCO presented in Ref. 4 versus the drain current of main transistors.

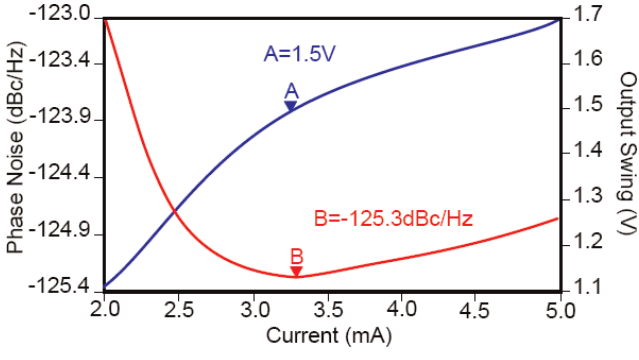


Fig. 4. Phase noise and amplitude of proposed VCO versus the drain current of main transistors.

2.2. *Frequency tuning*

In order to tune the oscillator over a wide frequency range, a large capacitance variation is required. In this respect, a bank of switched metal–insulator–metal (MIM) capacitors and a small varactor is used to cover a wide frequency range. Herein, a 4-bit binary weighted bank of switched capacitors and a pair of nMOS varactors have been used for coarse and fine frequency tuning, respectively. It is worth mentioning that it is possible to improve the tuning range using more control bits. However, the effect of parasitic capacitors will saturate this improvement. Considering these issues, we used a 4-bit binary weighted capacitor bank to obtain a wide tuning range.

Figure 1 shows the detailed schematic of this capacitor bank inspired from Ref. 6. In Ref. 6, large nMOS transistors are used as the main switches to achieve small on resistance and pMOS transistors are employed to bias the drain and source of the

nMOS transistors at the highest supply voltage where they are off. By this way, the parasitic drain-bulk and source-bulk junction capacitors of the main switches are greatly reduced when they are off. However, these small pMOS switches themselves introduce parasitic capacitors which degrade the tuning range of a wideband VCO when this switched-capacitor bank is utilized. So, in the proposed VCO, the resistors are used instead of small pMOS switches in order to improve the tuning range by reducing the parasitic capacitors as shown in Fig. 1. In this figure, $b_3b_2b_1b$ is a 4-bit control word of the capacitor bank. These bits, which can have two different 0 or V_{DD} values, are connected to the gate of the switches and their inverses are connected to the end of the resistors. Since the bulk of the nMOS transistors are connected to the ground, the voltage difference of the drain-bulk and source-bulk junction capacitors becomes the maximum and therefore their capacitances become minimum while the switch gets off. V_{ctrl} is the varactor control voltage changing from 0 V to 0.9 V (V_{DD}) for all coarse tuning bits. This switching topology results in reduced on resistance and off parasitic capacitors where they are both most desirable.

Using resistors leads up to 30% improvement in tuning range compared to using pMOS switches at cost of a slightly increased chip area. Each varactor is ac-coupled to the tank via a series MIM capacitor and its gate is biased at $V_{DD}/2$, to achieve a symmetric tuning range.

It is worth mentioning that the proposed switching scheme is different with that reported in Ref. 3. In Ref. 3, a series-parallel capacitor bank structure has been proposed to minimize the VCO gain variation. However, it does not have any suggestion to overcome the drawback of the parasitic effects induced by the switches.

2.3. *Oscillation amplitude and effective noise*

An indispensable feature in designing a class-C VCO is its feedback path with a voltage gain of K given as:

$$K = \frac{V_A}{V_{out+}} = \frac{V_B}{V_{out-}} = \frac{C_C}{C_C + C_T + C_P}, \tag{1}$$

where C_P is the total parasitic capacitance at nodes A and B in Fig. 1. In the conventional class-C VCO, this feedback path is used to create a negative resistance. It is possible to create this feedback path using an RC-filter or a center-tapped secondary winding of a transformer, the primary of which is replaced with the tank inductance.[4] If the utilized transformer ratio is larger than one, the obtained value of K will be larger than one as well. However, the value of K in the proposed topology is always lower than one.

Simulation results shown in Figs. 5(a) and 5(b) demonstrate how amplitude and phase noise depend on the values of capacitors. It is clearly inferred from these figures that the maximum/minimum the amplitude value is, the highest/lowest the phase

noise will be achieved, as simply expected from Eqs. (2) and (3)[4]:

$$L(\Delta\omega) = 10\log\left(\frac{k_B T}{2\Delta\omega^2 C^2 I_{\text{bias}}^2 R^2}\left(\frac{1}{R}+\frac{\gamma}{K}\frac{1}{R}\right)\right), \tag{2}$$

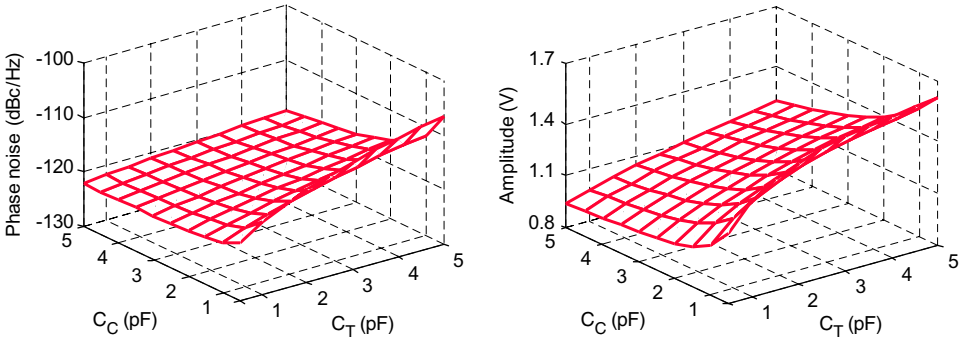
$$A_m = \frac{V_{\text{DD}}}{K+1}, \tag{3}$$

where $L(\Delta\omega)$ is the phase noise at a $\Delta\omega$ offset from the carrier, k_B is the Boltzmann constant, T is the absolute temperature. Also, C and R are, respectively, the capacitance and ohmic losses of the tank and γ and A_m are the channel noise factor and the output swing amplitude, respectively.

It is clear from Eqs. (2) and (3) that increasing or decreasing the value of K has contrary effects on the values of phase noise and output swing, revealing the importance of choosing the optimum value of K. As shown in Eq. (1), the value of K depends on the values of C_T, C_C and C_P. In the proposed VCO, C_P is trivial in comparison with C_T and C_C and hence it can be ignored. Taking Figs. 5(a) and 5(b) into consideration, it is feasible to choose intervals for C_T and C_C in which the amplitude and the phase noise reach their optimum values. It is worth mentioning that, although Eq. (2) shows that the phase noise reduces at large output amplitudes, this equation is valid as long as the oscillator works in the current-limited region. That is why the maximum value of output amplitude and the minimum value of phase noise do not occur at the same point in Figs. 5(a) and 5(b).

3. Simulation Results and Comparison

The proposed and conventional class-C VCOs are simulataed in a 0.18 μm RF CMOS technology using advanced design system (ADS). The simulated device parameters are also shown in Fig. 1. For the sake of a fair comparison between the phase noises, we have intentionally considered similar tuning ranges for these



(a) (b)

Fig. 5. Variation of (a) phase noise and (b) amplitude versus the capacitances of C_T and C_C.

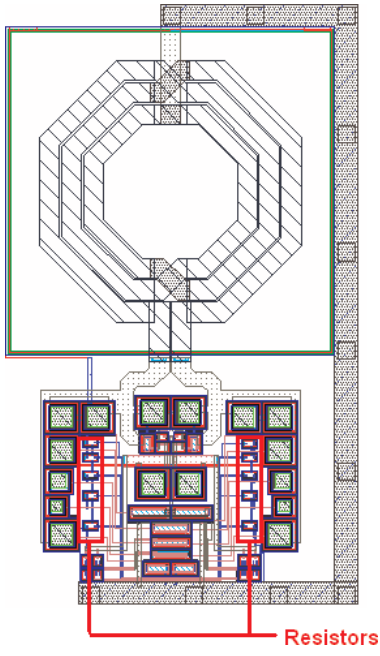


Fig. 6. Layout of the proposed high-swing Class-C VCO.

oscillators in our simulations. Figure 6 shows the layout of the proposed high-swing class-C VCO. The total layout area without bonding pads is 0.4 mm.[2] This figure shows that, resistors used in the capacitor bank cause a negligible increasing in the chip area. It is worth mentioning that using the resistors instead of pMOS switches results in less parasitic capacitors and hence a wide tuning range at cost of slightly increased chip area. The frequency band is 1.82−2.65 GHz as shown in Fig. 7. Sixteen subsections with a little overlap between each two adjacent subsections have formed this continuous frequency band. This figure also shows a very low VCO gain (less than 67 MHz/V) has been achieved using the 4-bit capacitor bank. Variation of phase noise versus the offset frequency is illustrated in Fig. 8 which shows a ∼125.3 dBc/Hz phase noise at 1 MHz offset frequency for 2.2 GHz carrier frequency. Figure 9 presents the transient response of the signals at the drain and gate terminals of M_1 transistor. Since no current-biasing tail transistor is utilized, M_1 and M_2 are allowed to switch rail-to-rail; thus the tank output voltage swing is maximized.

To compare the performance of the proposed oscillator with recent VCOs, two different figure of merits (FoMs) which have been defined in Ref. 5 are utilized. The first FoM is given by:

$$\text{FoM} = 10 \log \left[\frac{k_B T}{P} \left(\frac{\omega_o}{\Delta\omega} \right)^2 \right] - L(\Delta\omega) \tag{4}$$

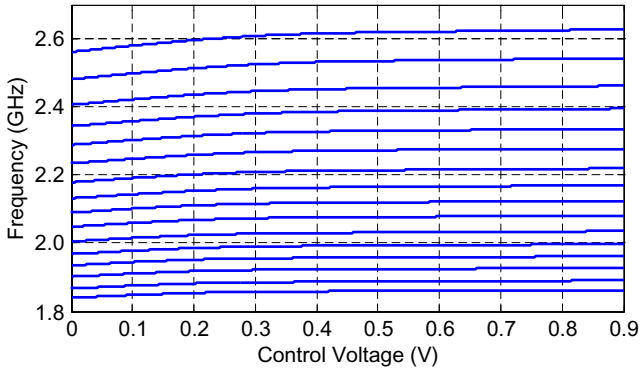


Fig. 7. Simulated VCO tuning curves.

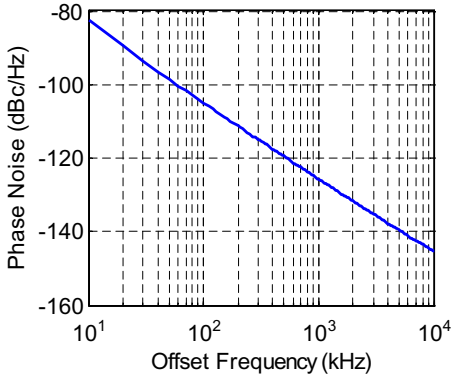


Fig. 8. Simulated phase noise versus the offset frequency.

where k_B is the Boltzmann constant, T is the absolute temperature, ω_0 is the carrier frequency, and $L(\Delta\omega)$ is the phase noise at a $\Delta\omega$ offset from the carrier and P is the power consumption. The second figure of merit named as PFTN involves the tuning range and obtained by substituting the $(\omega_{\max} - \omega_{\min})$ instead of ω_0 in Eq. (4). $\omega_{\max}$ and $\omega_{\min}$ are respectively the maximum and minimum oscillation frequencies.

Comparison of the performance of proposed wideband VCO with the conventional class-C one and several recent designs are summarized in Table 1. Despite the 3.2 dB phase noise improvement estimated by Eq. (2), simulation results shows that the proposed VCO achieves 2.9 dB lower phase noise compared to the conventional class-C oscillator. To have a fair comparison, both proposed and conventional class-C VCOs were simulated in a 0.18 μm CMOS technology in their minimum phase noise state. Besides, to have a better view on the achieved results of the proposed VCO, the measurement results of a few reported designs are included in Table 1 although the comparison of simulated results with measured ones would not be fair.

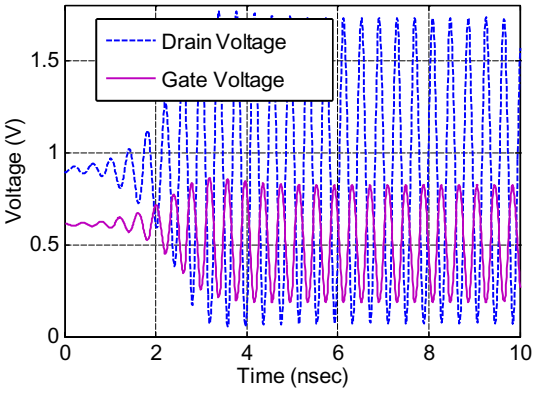


Fig. 9. Transient response of signals at gate and drain terminals of M_1.

Table 1. Performance comparison of the proposed VCO.

References	Technology	Center freq. (GHz)	TR (%)	PN (dBc/Hz)	Power (mW)	PFTN (dB)	FoM (dB)
This work[a]	0.18 μm CMOS	2.2	37	−125.3 at 1 MHz	3.5	178.5	187
Conventional class-C*	0.18 μm CMOS	2.2	37	−122.4 at 1 MHz	2.2	177.3	185.5
[1][b]	0.35 μm CMOS	2	36	−121.6 at 500 kHz	6.72	175.6	185.3
[2][b]	65 nm CMOS	3	26	−127.5 at 1 MHz	28.8	170.7	182.4
[3][b]	0.18 μm CMOS	5.2	18	−113.7 at 1 MHz	9.7	162.6	178.2

Note: [a]Simulation results. [b]Measurement results.

4. Conclusions

In this paper, a new class-C VCO was proposed. In this VCO, the tail capacitor of the conventional class-C oscillator is dislocated from the source of the transistors to their gate to achieve a rail to rail output swing which improves the phase noise by 2.9 dB compared to the conventional class-C VCO. Also, a new switching scheme was presented in the switched capacitor bank of the proposed VCO to lower the on resistance and the parasitic capacitors of the switches.

Acknowledgment

This work has been supported in part by Iranian Nanotechnology committee.

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