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A front-end amplifier with tunable bandwidth and high value pseudo resistor for neural recording implants

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ABSTRACT

In this paper, a tunable front-end amplifier is presented for neural recording implants. To program the low cut-off frequency, a bias circuit is used to adjust the value of pseudo resistors with lower sensitivity to the process variations and also to achieve very large value about 1 TΩ with high linearity. The band pass filter (BPF) can adjust high cut-off frequency and power consumption with two recording modes. The high cut-off frequency is 4.15 kHz and 8.2 kHz in low recording (LR) and high recording (HR) modes, respectively. The low cut-off frequency can be adjusted to 0.8 Hz and 300 Hz. The proposed amplifier is able to separate the neural signals with different frequencies for amplification. It has been designed and simulated in TSMC 0.18 μm CMOS process. The achieved input-referred noise is about 2.1 μVrms and 1.7 μV_{rms} in HR and LR modes, respectively. The total power consumption is 3.6 μW from a 1-V supply with −46.3 dB THD.

1. Introduction

Electronic interfaces in the nervous systems are important because of their use in the neuroscience, medical diagnosis and treatment modalities, but because of the contemporary needs for a complete and efficient system, there is always a new approach to these interfaces, which will provide a good opportunity for circuit and system designers [1]. Clinical experiments on paralyzed humans show that by multiple neural signals from the cerebral cortex, it is possible to develop prosthetic devices. Actually, with the help of multi-electrode arrays, the neural signals can be recorded and directed from the motor cortex of the brain with high speed and resolution, which can control the external prostheses. So researchers are interested in recording and analyzing the neuronal activity in the brain [2].

The analog front-end amplifier (AFE) is one of the important blocks in the design of the neural recording systems. This block is located after the electrodes, and the received signals from the electrodes should first be amplified and then processed and all blocks of the neural recording system are digitally controlled [3,4]. The design of the front-end amplifier has several challenges that need to be addressed. The electrode-tissue interface can add a DC offset voltage to the input signal. In fact, the creation of the DC offset voltage is due to the electromechanical reaction that occurs at the electrode-tissue interface [4]. For example, the neural tissue in the two different electrodes has different DC voltages. The offset voltage range is usually between 1 and 10 mV and it can reach up to 50 mV [4]. This high offset voltage saturates the amplifier because its amplitude is much larger than the input signal. Therefore, a high pass filter is required to remove the DC offset before its amplification [5].

The input-referred noise of the front-end amplifier should be very small because the amplitude of extracellular potential recorded from the neural signal starts from about 50 μV and reaches up to 500 μV [6,7]. Significant information from the received neural signals is typically located in the frequency range of a few Hz to a few kHz [8]. The simultaneous activity of many neurons in one region of the brain produces a signal that is called the local field potential (LFP). Also, the neurons have the ability to produce spike at the time of stimulation [6]. This spike is called the action potential (AP). The frequency contents of the AP signal is usually between about 300 Hz and 10 kHz, but for LFP signals, they are often less than a few hundred Hz [6,8].

With the capacitive-resistive feedback network in the amplifier, it is possible to generate the desired high and low cut-off frequencies for putting the neural signal in the amplification band [3]. In Ref. [9], a capacitive-resistive feedback network is used in the neural recording amplifier. In this structure, pseudo-resistors consisting of PMOS transistors are used to achieve very small low cut-off frequency. But in Ref. [9], the value of the pseudo-resistors is constant which causes the cut-off frequency to be constant. In recent works, there is a tendency for

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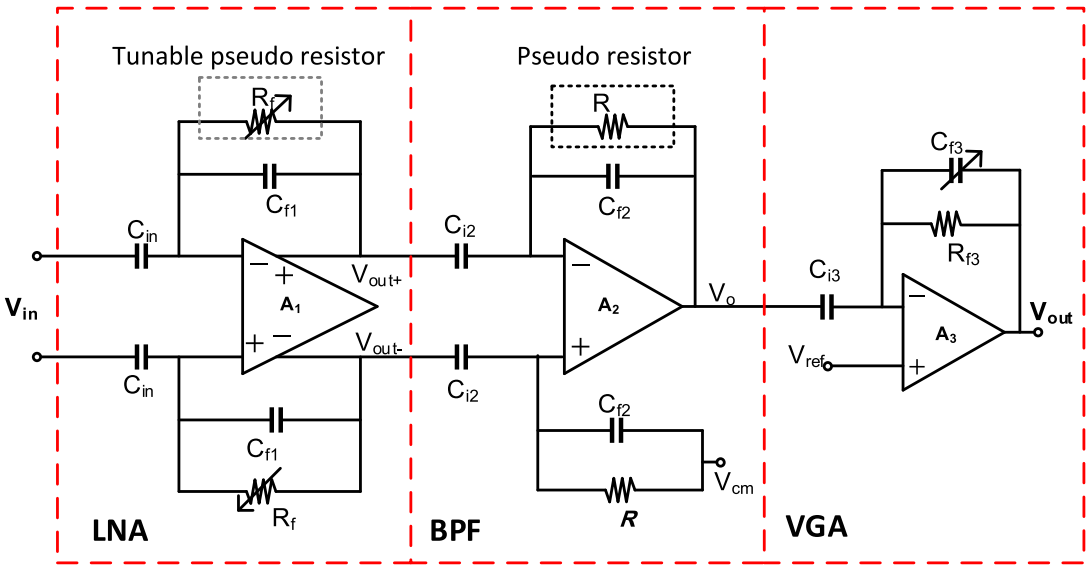

Fig. 1. Schematic of the proposed neural recording analog front-end.

programmable cut-off frequencies because the frequency range of the neural signals is variable and the neural recording systems must be able to separate the different frequency bands in order to be more efficient [4,8,10].

In [8], a combination of the voltage-controlled and current-controlled pseudo-resistors is used to reduce the total harmonic distortion (THD). In Ref. [8], by changing the bias current of the pseudo-resistors, the cut-off frequency is tunable. But, due to the small bias current of these pseudo-resistors, it is difficult to construct a digital-to-analog converter (DAC) to produce this small bias current. A capacitively-coupled structure with reconfigurable topology is used in Ref. [10] where the high and low cut-off frequencies depend on the capacitance and transconductance of the amplifiers making a programmable recording system for neural signals. In this structure, the low cut-off frequency depends on the transconductance of the amplifier and no pseudo-resistor has been used which increases the power consumption and noise of the circuit.

In [11], four stages are used to design the front-end amplifier where the cut-off frequency is tuned by changing the capacitors of the stages. It also uses the pseudo-resistors in the AP mode to generate a proportional low cut-off frequency, but due to the use of pseudo-resistors in the subsequently blocks, the linearity in this system is reduced because the voltage variations across the pseudo-resistors will be increased. In Ref. [12], the analog front-end consists of three stages, including low noise amplifier, programmable gain amplifier (PGA) and an integrator. Parallel channels are used where the LFP signal passes through the integrator after the PGA, while the AP signal is generated from the PGA output. Using of the integrator to reduce high cut-off frequency increases the power consumption while by reducing the bias current of the input transistors of the PGA, the high cut-off frequency can be reduced. Although the neural signals can be separated in Ref. [12], the linearity is not considered. In Ref. [13], a DAC is used to change the gate voltage of transistors realizing the pseudo-resistors, which produces a tunable low cut-off frequency, and its value can be 1 Hz, 150 Hz, and 220 Hz. However, the structure of pseudo-resistor has a low linearity.

The useful way to program the low cut-off frequency is to use a variable pseudo resistor. But to change the high cut-off frequency, both the output capacitor of the amplifier and the bias current of the filter can be changed. To record neural signals with low frequency ranges, the output capacitors of the amplifiers are increased in Refs. [8,10,11] which increase the die area. The bias current of the filter is reduced in Ref. [13] to reduce the high cut-off frequency resulting in low power consumption. This work uses a filter with tunable bias current to program the high cut-off frequency and reduce the power consumption.

In this work, an analog front-end amplifier is designed to record neural signals and has a tunable gain from 45 dB to 55 dB. There are three blocks in this design, which are low noise amplifier, band-pass filter and variable gain amplifier. The high value pseudo-resistors have been used to create small low cut-off frequency and amplify the neural signals at very low frequencies. The pseudo-resistors have a bias circuit which makes the value of pseudo-resistor very large with less variability. When the neural signals are in the low frequency ranges, the AFE is able to reduce the bandwidth and the power consumption by reducing the bias current of the filter. The high and low cut-off frequencies of the front-end amplifier are programmable which causes the separation of the neural signals. In the low recording (LR) mode, the high cut-off frequency is reduced to 4.15 kHz, and the power consumption is reduced by 20% compared to the high recording mode (HR), while in the HR mode, it is 8.2 kHz. The low cut-off frequency can be also adjusted to 0.8 Hz and 300 Hz.

The rest of the paper is organized as follows. In Section 2, the structure, analysis, and design of the proposed neural recording front-end amplifier are presented. The detailed circuit level post layout simulation results are provided in Section 3. Finally, Section 4 concludes the paper.

2. Proposed neural recording analog front-end

2.1. Overall structure

Fig. 1 shows the overall structure of the proposed neural recording analog front-end. This structure consists of three stages. The first stage is a low noise amplifier (LNA) and the second stage is a band-pass filter (BPF). A variable gain amplifier (VGA) is utilized in the last stage.

Since the LNA is designed in the first stage, its input-referred noise is very important. So, the input-referred noise of the LNA should be as low as possible. In designing the LNA, a fully-differential amplifier is used because the fully-differential amplifiers have a high common-mode rejection ratio (CMRR) than single-ended amplifiers. However, single-ended amplifiers are simple to design due to the lack of designing the common-mode feedback circuits. They also have lower power consumption and smaller die area than differential amplifiers. Since the BPF is located after the LNA, its input-referred noise is divided by the gain of the LNA. Therefore, its input-referred noise does not affect the total input-referred noise of the structure as much as the LNA. Moreover, the CMRR of the LNA (first stage) is dominant compared to other blocks,

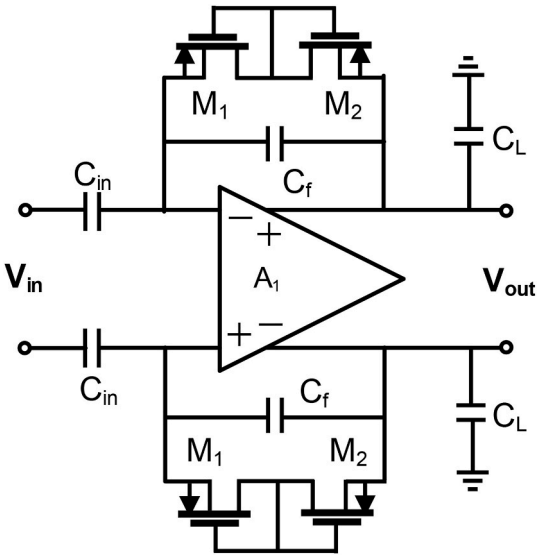

Fig. 2. The conventional neural LNA [9].

which are located after LNA. Therefore, a single-ended amplifier is used to design the BPF in the second stage to reduce the required power consumption and die area. The low and high cut-off frequencies of the front-end should be programmable to separate the neural signals with different frequency ranges. The variable pseudo-resistors are used to change the low cut-off frequency because this frequency depends on the value of feedback capacitor and resistor. To change the high cut-off frequency, a bias circuit is used to change the current of the transistors in the operational amplifier of the BPF which is described below. In the last stage of the design, a variable gain amplifier has been used. Since the amplitude of neural signals is variable, using a variable gain amplifier can amplify the neural signals with sufficient gain resulting in enhanced dynamic range in the total system. This also reduces the required dynamic range, and hence, the resolution of the subsequent analog-to-digital converter (ADC).

2.2. Low noise amplifier

The neural amplifier should be able to amplify the neural signals with small amplitude. On the other hand, the offset voltage generated by the electrodes is also added to the main signal. Therefore, the amplifier should eliminate the large offset voltage and amplify the neural signal at the same time. The capacitive feedback amplifier as shown in Fig. 2 with BPF characteristic can eliminate the DC offset [4]. As mentioned previously, the frequency of some neural signals like LFP is very small. So the amplifier should have a very small low cut-off frequency. For this reason, PMOS transistors are used as pseudo-resistors.

The low cut-off frequency of the LNA shown in Fig. 2 is given by Ref. [9]:

$$f_L = \frac{1}{2\pi C_f R_f} \tag{1}$$

where R_f is the equivalent resistance of M_1 and M_2 transistors. The mid-band gain of this amplifier is given by:

$$A_v = \frac{-C_{in}}{C_f} \tag{2}$$

As mentioned in the previous section, the mid-band gain of the LNA is equal to the ratio of the input and feedback capacitors. To get enough gain, the value of input capacitor should be much larger than the feedback capacitor which reduces the input impedance of the amplifier.

In conventional LNA structure, to achieve a gain of more than 40 dB and also to set the low cut-off frequency close to 1 Hz, the input capacitor (C_{in}) and the feedback capacitor (C_f) have been selected about 100 pF and 1 pF, respectively. To reduce the input capacitor and have a suitable gain, the feedback capacitor should be reduced. But according to equation (1), reducing the feedback capacitor increases the low cut-off frequency. So, to keep the low cut-off frequency constant, the value of the pseudo-resistor must be also increased.

2.2.1. Pseudo-resistors

The design of pseudo-resistors is an important challenge in neural recording systems because these types of resistors, due to their high value, cause the cut-off frequency to be below a few Hz [9]. Larger values of pseudo-resistors allow smaller capacitors in amplifier to be selected in order to achieve the desired gain and frequency response. However, due to their sensitivity to the process and voltage variations, their value changes and causes the system to become non-linear. So, the study of their linearity behavior is also very important [14].

Fig. 3 shows the structure of several widely used pseudo-resistors [3–5,7,8,13–16]. The structure of Fig. 3(a) is a non-tunable pseudo-resistor and since the gates of transistors are inwardly connected to their drain terminals, its transistors are located in deep sub-threshold region and its value is also non-tunable [14]. The structure shown in Fig. 3(b) is known as gate-voltage-controlled back to back MOSFETs (BBMOS), and due to the voltage applied to the gates of transistors, it can be tuned [8]. The pseudo-resistor in Fig. 3(c) is called the complementary structure and it consists of one NMOS and one PMOS transistor [14]. The gates of these transistors are biased by two separate voltages, which eventually lead to tuning of its value.

For comparison of the linearity of the above-mentioned pseudo-resistors, their I/V characteristics are illustrated in Fig. 4. In this simulation, the voltage of nodes A and B is equal to 0.5 V and the voltage across the transistors (V_{BA}) changes between −0.3 V and 0.3 V. In the complementary structure and BBMOS, voltages V_P and V_{TUNE} are the same and it is equal to 0.35 V and the voltage V_n is 0.65 V. So, the transistors are in the sub-threshold region. But the transistors in the non-tunable structure are in the deep sub-threshold region because the voltage V_{GS} is zero. According to Fig. 4(a), the current changes versus voltage changes across transistors (V_{BA}) of the non-tunable pseudo-resistor are greater than the complementary structure. Fig. 4(b) shows the I/V characteristic of the BBMOS pseudo-resistor. In this structure, for positive voltage changes across transistors, the current changes a lot because the transistors are in the sub-threshold region and the current increases as the voltage increases.

As mentioned before, the value of the pseudo-resistor must also be considered along with its linearity, because high value pseudo-resistors

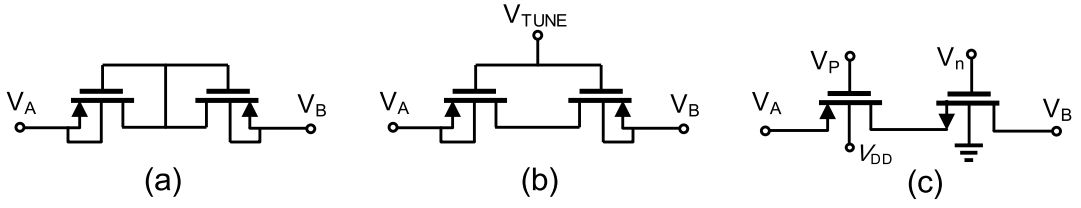

Fig. 3. Pseudo-resistors structures (a) non-tunable [9] (b) gate-voltage-controlled back to back MOSFFETs (BBMOS) [8] and (c) complementary structure [14].

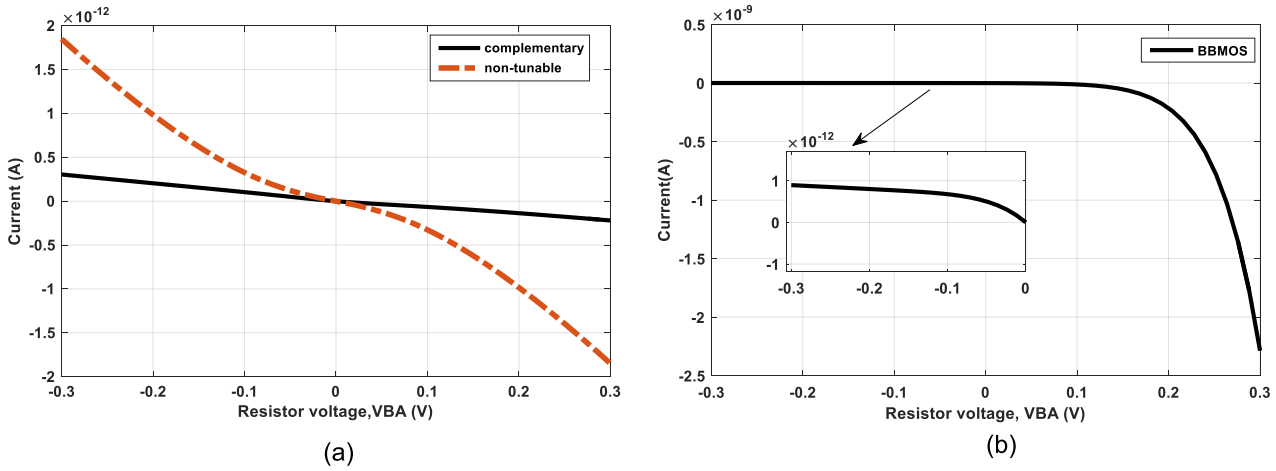

Fig. 4. The I/V characteristic of pseudo-resistors (a) non-tunable and complementary and (b) BBMOS.

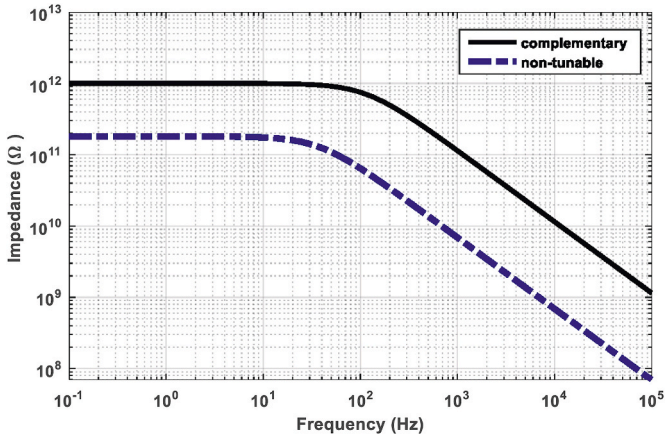

Fig. 5. The resistance of non-tunable and complementary pseudo-resistors.

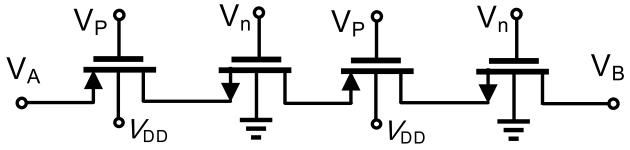

Fig. 6. Double complementary structure in series.

are required to amplify the neural signals at very low frequencies. Fig. 5 shows the impedance value versus frequency for the non-tunable and complementary structures. According to this figure, the complementary structure has a large value of resistance. At frequency of 1 Hz, the pseudo-resistor value is equal to 1 TΩ, while the non-tunable pseudo-resistor value is about 180 GΩ. In the amplifier of Fig. 2, in order to have a gain of 40 dB and a low cut-off frequency of 1 Hz, the input and feedback capacitors must be selected 100 pF and 1 pF, respectively, when the conventional pseudo resistor is utilized. If the complementary pseudo-resistor is placed in this structure, the input and feedback capacitors are reduced to 15 pF and 0.15 pF, respectively. Therefore, the use of high value pseudo-resistor helps to reduce the capacitors, which in addition to increasing the input impedance of the amplifier also reduces the die area.

One way to improve the linearity for pseudo-resistors is to use multiple pseudo-resistors in series, which reduces the voltage changes across the transistors [8,14]. Fig. 6 shows the double complementary structure in series as pseudo-resistor and in Fig. 7, the I/V characteristic

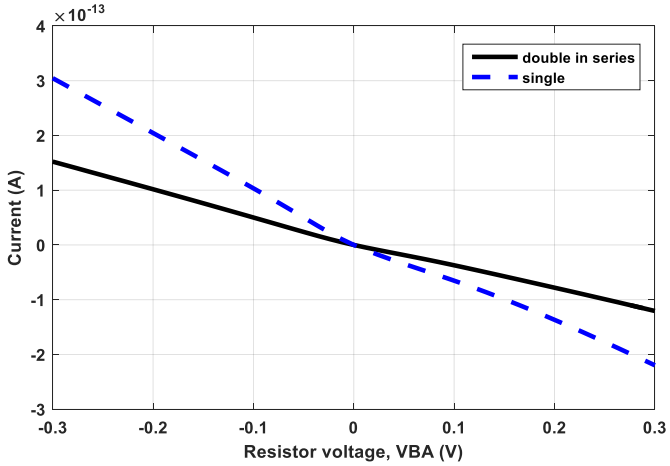

Fig. 7. Simulated I/V curve for the double and single complementary structure.

for the series and single structures shows that the current changes in the series structure are less than the single complementary structure.

Although the series structure for pseudo resistor increases its linearity, the design of the bias circuit for pseudo resistor is very important and challenging because the bias circuit must locate transistors well in the sub-threshold region to get the proper linearity. In addition, the bias circuit should be able to program the value of pseudo resistor to separate the neural signals. Therefore, the value and the linearity of the pseudo resistor depend on its bias circuit.

2.2.2. *Proposed LNA structure*

Fig. 8 shows the circuit schematic of the proposed LNA. In this amplifier, the mid-band gain depends on the value of input and feedback capacitors. The voltage gain is also given by equation (2) and the value of C_{in} and C_f are considered 11 pF and 85 fF, respectively, for having a gain of 42 dB. Transistors M_{p1}-M_{p2} and M_{n1}–M_{n2} are used to realize the pseudo-resistor. The simple equivalent circuit for the electrode is also shown in Fig. 8 where the value of R_T, R_S, and C_S are 12.3 kΩ, 17 GΩ, 205 nF, respectively [17].

The pseudo-resistor used in the proposed LNA is tunable and a bias circuit is used for this purpose. According to Fig. 8, when $S_0S_1 = 11$, voltages V_{p1} and V_{n1} are connected to the pseudo-resistor, In this case, voltages V_{p1} and V_{n1} are 0.35 V and 0.65 V, respectively, and the low cut-off frequency is 0.8 Hz. In order to increase the low cut-off frequency, the value of pseudo resistor must be reduced. In other words, the current of pseudo resistor transistors must be increased. Therefore,

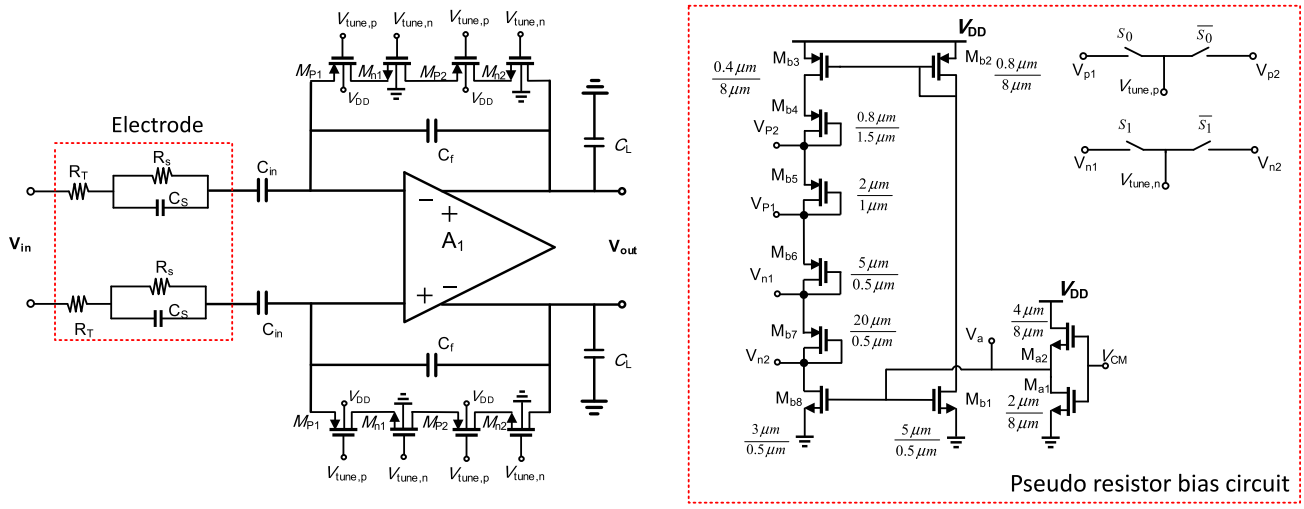

Fig. 8. The proposed neural recording LNA.

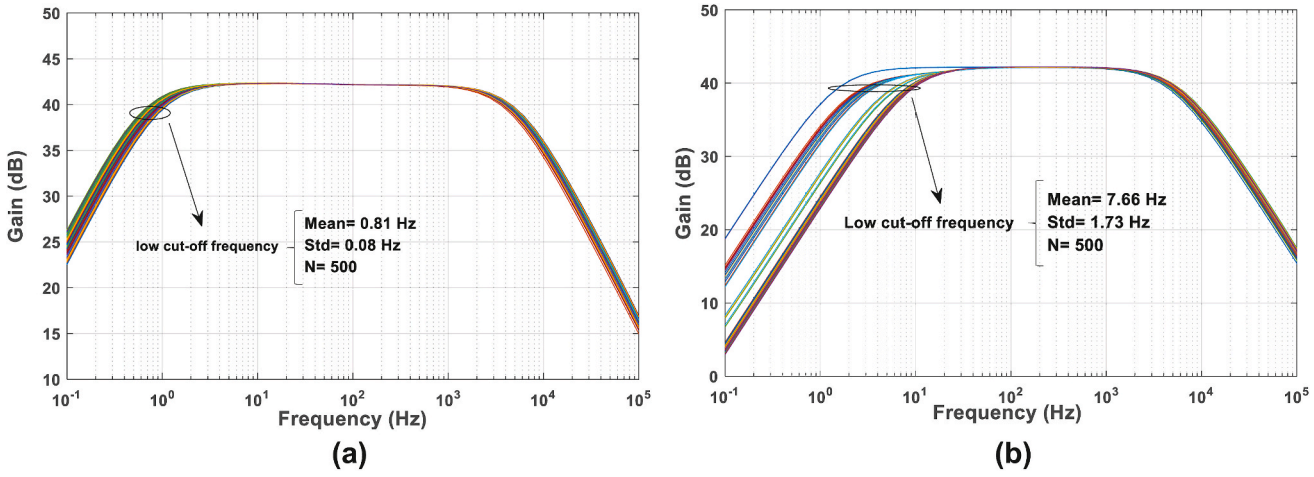

Fig. 9. Frequency response Monte Carlo simulation results of the (a) proposed and (b) conventional LNAs.

the bias circuit must provide two suitable voltages for the pseudo-resistor to increase its current and ultimately reduce its value. When $S_0S_1 = 00$, then voltages V_{p2} and V_{n2} are connected to the pseudo-resistor. The voltages V_{p2} and V_{n2} are 0.15 V and 0.85 V, respectively. In this case, the cut-off frequency is equal to 300 Hz. Therefore, the value of the pseudo-resistor and low cut-off frequency depends on the pseudo-resistor bias circuit, which must be designed to have small variations and sensitivity to process, voltage, and temperature (PVT) variations. The bias circuit uses a voltage attenuator that supplies the gate voltage of transistors M_{b1} and M_{b8}. The input of the attenuator circuit is connected to the V_{CM} voltage, which is equal to half of supply voltage and its output voltage is approximately obtained as [18]:

$$V_a = V_{OD1}\left(1 - \sqrt{\frac{\left(\frac{W}{L}\right)_{M_{a1}}}{\left(\frac{W}{L}\right)_{M_{a1}} + \left(\frac{W}{L}\right)_{M_{a2}}}}\right) \tag{3}$$

where $V_{OD1} = V_{GS1} - V_{TH1}$ and it is the overdrive voltage of the transistor M_{a1} and W/L is the aspect ratio of transistors. In the bias circuit, the V_a voltage is supplied to the gate of transistor M_{b1} by the attenuator circuit. The V_a voltage is obtained according to Equation (3) and its value is about a few tens of mV. The small V_a causes the bias circuit transistors to be located in the sub-threshold region and eventually with small bias currents. In sub-threshold region, the drain-source current is given by Ref. [19]:

$$I_D = I_0\left(e^{\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)}\right)\left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \tag{4}$$

where $V_T = kT/q$, $I_0 = \mu_0 C_{ox}(W/L)$ and V_{TH} is the threshold voltage. The current of bias transistors varies very little.

Because it is controlled by the voltage V_a. Considering ±10% changes for V_{DD} and V_{CM} voltages and according to the relation (3), which shows that the voltage V_a depends mainly on the aspect ratio of the transistors. So, the V_a changes about a few millivolts. On the other hand, according to relation (4), low current changes of bias transistors have little effect on bias voltages of pseudo-resistor due to the exponential relationship.

The Monte Carlo analysis has also been performed to compare the sensitivity between the proposed structure in Fig. 8 and the conventional structure in Fig. 2 to the process variations and devices mismatch. Fig. 9 shows Monte Carlo simulation results of the proposed and conventional LNAs frequency response with 500 runs. In these simulations, the same amplifier (A_1) is used and the input and feedback capacitors are selected as 11 pF and 85 fF, respectively. According to Fig. 9, the standard deviation of the low cut-off frequency in the proposed LNA is about 0.08 Hz, while in the conventional structure, it is 1.7 Hz. As mentioned earlier, the pseudo-resistor in the conventional structure is more

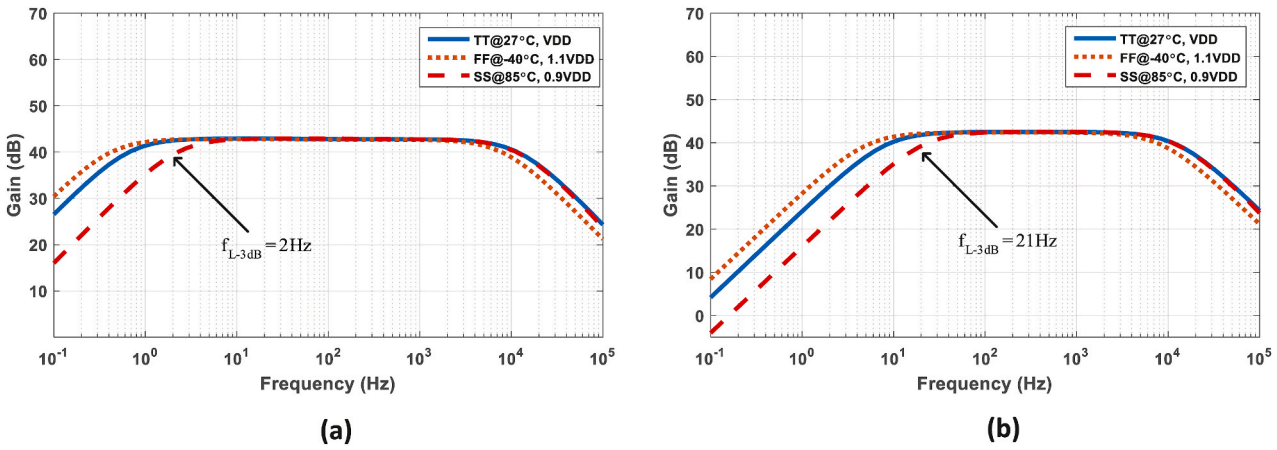

Fig. 10. Frequency response simulation results of the (a) proposed and (b) conventional LNAs in PVT variations.

Table 1
Comparison of the low cut-off frequency value of the proposed LNA with the conventional LNA in PVT conditions.

Parameter	Structure	FF@ −40 °C (V_{DD} = 1.1 V)	SS@ 85 °C (V_{DD} = 0.9 V)	TT@27 °C (V_{DD} = 1 V)
Low cut-off frequency (Hz)	Proposed LNA	0.4	2	0.65
	Conventional LNA	4.6	21	8.2

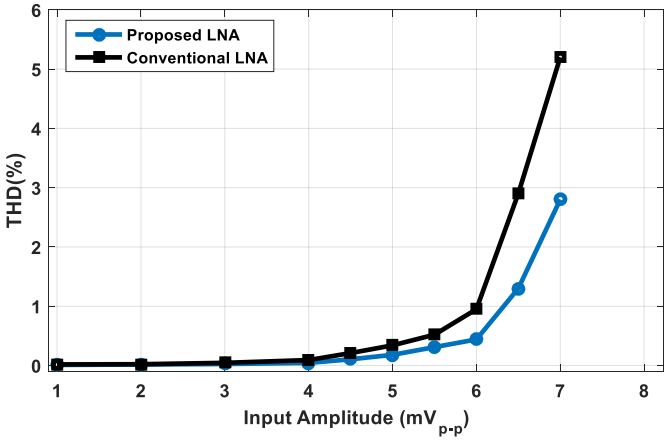

Fig. 11. Total harmonic distortion of the proposed and conventional LNAs.

sensitive, and these changes in the low cut-off frequency are well illustrated. In addition to the Monte Carlo simulation, the frequency response simulation results of the proposed and conventional LNAs in different process corner cases, supply voltage, and temperature (PVT) variations are shown in Fig. 10. According to this figure, the frequency response of the proposed LNA is well robust over PVT conditions. Moreover, the low cut-off frequency values of the proposed and conventional LNAs are reported in Table 1. This table well indicates that the low cut-off frequency value of the proposed LNA has fewer variations than the conventional LNA over PVT variations.

One way to evaluate the performance of the pseudo-resistor linearity is to apply a single-tone sinusoidal signal at 1 kHz with different amplitudes to the amplifier input. By increasing the amplitude of the input signal, voltage variations across pseudo-resistor transistors increase, and then the linearity will be reduced. Fig. 11 shows the THD of the proposed and conventional LNAs versus input signals with different amplitudes. Both the proposed LNA and the conventional LNA have the same gain which is 42 dB. According to this figure, the proposed LNA has a low THD value compared to the conventional LNA for the input signals with higher amplitudes.

Fig. 12 shows the resistance value of the proposed and conventional pseudo-resistors versus temperature variations at 1 Hz in typical corner case. According to this figure, the resistance variations of the proposed pseudo-resistor are less than the conventional pseudo-resistor over temperature variations from 0 °C to 85 °C. In fact, the maximum resistance variations of the proposed pseudo-resistor are about 4 GΩ, whereas it is more than 180 GΩ for the conventional pseudo-resistor.

Given the disadvantages mentioned for conventional non-tunable pseudo-resistors, recent works have focused on designing a bias circuit to adjust the pseudo-resistor value and control its changes. For example, reference [20] uses a feedback loop structure that continuously adjusts the gate voltage of pseudo-resistor transistors according to the input signal. Although the feedback loop circuit adjusts the pseudo-resistor value well with input signal changes, due to the use of an externally-generated voltage circuit and an amplifier, the circuit complexity and the power consumption are increased. But, the bias circuit provided to adjust the pseudo-resistor value has very little power consumption because its transistors are located in sub-threshold region. Reference [21] also uses an external bias circuit for its pseudo-resistor. In Ref. [21], to increase the linearity, parallel architecture has been used. With this parallel structure, the linearity has been improved, and its THD has reached −50 dB. The maximum value of pseudo-resistor is also about 20 GΩ which is not enough for recording low frequency neural signals.

Fig. 13(a) shows the structure of folded-cascode amplifier that is used in the proposed LNA of Fig. 8. In comparison with other single-stage amplifiers, the folded-cascode amplifier has a high output voltage swing [19,22]. So, it is suitable for amplifying the neural signals with variable amplitudes. The flicker noise is dominant at low frequencies, and PMOS transistors have less flicker noise than NMOS transistors [19]. Input transistors in LNA have most effect on input-referred noise. So, the input transistors, M_1 and M_2, have been chosen as PMOS type, and they also have large sizes to reduce the flicker noise. Given that the first stage is a fully-differential folded-cascode, it requires a common mode feedback (CMFB) circuit which is shown in Fig. 13(b). The function of the CMFB circuit is that first the output voltages of LNA are compared to a reference voltage called V_{CM}. The V_{CM} voltage is half the supply voltage. Then, the Vcmfb voltage is generated in proportion to the sampled output voltages, which is given to the amplifier as a bias. So during the process of this feedback loop, the output voltages are equal to the reference voltage. As shown in Fig. 13 (c), a high-swing cascode current mirror is used to bias the main amplifier.

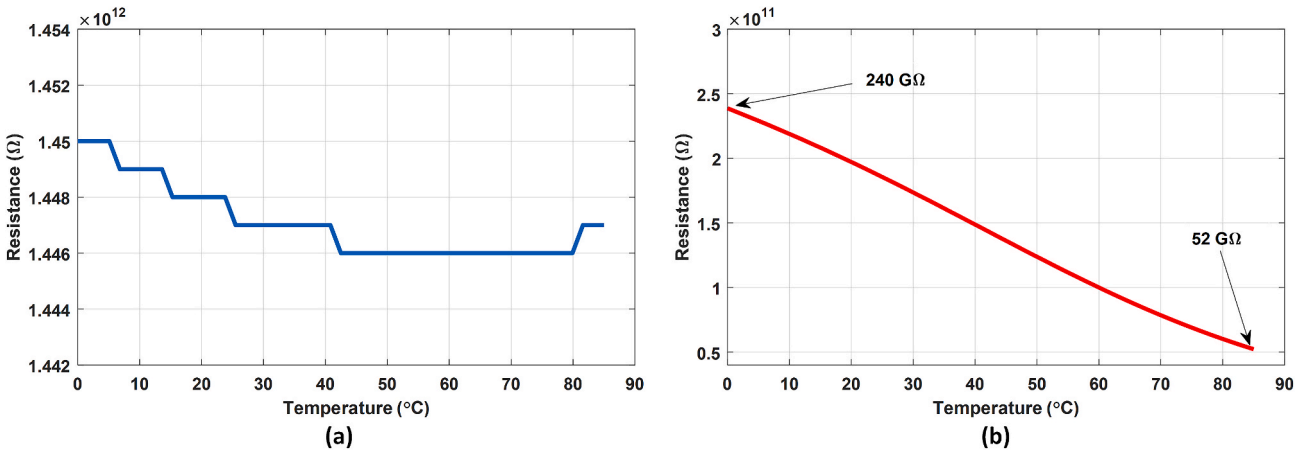

Fig. 12. Resistance value versus temperature variations for (a) the proposed and (b) conventional pseudo-resistors.

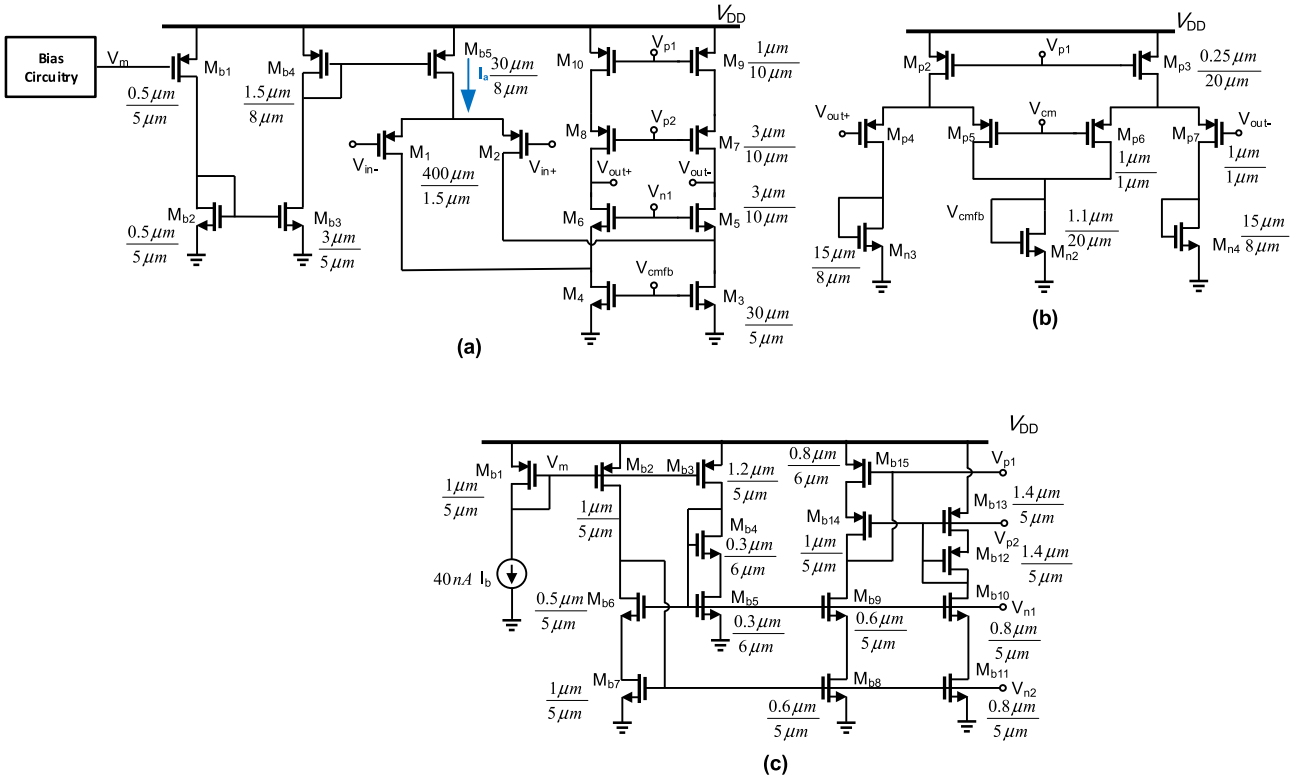

Fig. 13. (a) The folded-cascode amplifier used in the proposed neural LNA, (b) CMFB and (c) bias circuits.

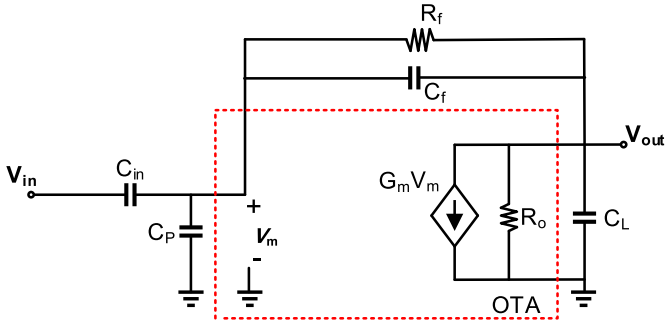

Fig. 14. Small-signal diagram of the proposed neural LNA.

2.2.3. Small-signal analysis

The small-signal analysis is important in the design of the neural recording systems because the bandwidth and input-referred noise are determined by this analysis. The small-signal model for the proposed LNA is shown in Fig. 14 where R_f represents the effective resistance of the series combination of M_{p1}-M_{p2} and M_{n1}–M_{n2} in Fig. 8. R_o and C_p are the equivalent output resistance and input capacitance of the OTA, respectively. Assuming that C_{in} is large enough than C_f and also C_L is larger than C_f and by analysis of the small-signal circuit, we have:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_f C_L (C_{in} + C_f)}{C_f} \cdot \frac{s\left(sC_f - G_m + \frac{1}{R_f}\right)}{(sR_f C_f + 1)\left(sC_L\left(1 + \frac{C_{in}}{C_f}\right) + G_m\right)} \tag{5}$$

In the above relation, due to the small value of parasitic capacitance

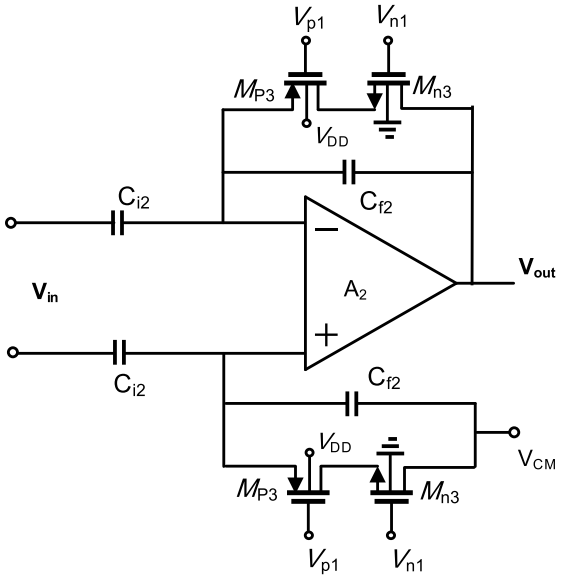

Fig. 15. Structure of band-pass filter.

at the input terminal of OTA and large value of output resistance of the OTA, they are neglected. According to Equation (5), high cut-off frequency of the proposed LNA is approximately obtained as:

$$f_H = \frac{G_m}{2\pi C_L A_v} \tag{6}$$

where G_m and A_v are the transconductance and the mid-band gain of the amplifier, respectively, and C_L is the equivalent capacitance at the LNA output.

The input impedance of the LNA is one of the important parameters in the design of the neural interface. The electrodes between the neural signals and the LNA have a large impedance that reaches several tens of mega ohms. So, to prevent the attenuated input signal, the input impedance of the LNA should be very larger than the impedance of electrodes. According to Fig. 14, the input impedance of proposed LNA is obtained as:

$$Z_{in} = \frac{1}{sC_{in}} + \frac{sR_f(C_f + C_L) + 1}{(sC_fR_f + 1)(G_m + sC_L)} \tag{7}$$

According to the relation (7), the input impedance value increases with decreasing the input capacitor value. The value of input capacitor should be larger than the feedback capacitor to get the sufficient gain. But by reducing the value of the input capacitor in order to increase the input impedance, the value of feedback capacitor should be reduced, which leads to an increase in low cut-off frequency. It can be compensated by using high-value pseudo resistors. But the linearity is an important parameter in the design of these types of pseudo-resistors that should be considered.

2.2.4. Noise analysis

The input-referred noise of the analog front-end is one of the important and critical parameters in the design of the neural recording systems because it is located at the first stage. Therefore, the noise of the analog front-end should be as small as possible. Of course, it should be noted that there is a trade-off between the power consumption and noise. So in this design, the noise should be kept small with low power consumption.

According to the structure shown in Fig. 8, by considering the input-referred noise of the operational amplifier, the PSD of input-referred noise of the proposed LNA is given by Ref. [23]:

$$\overline{V_{n,LNA}^2} = \left|\frac{1 + s(C_{in} + C_f + C_p)}{sC_{in}}\right|^2 . \overline{V_{n,A1}^2} \tag{8}$$

where $V_{n,A1}$ is the input-referred noise of the OTA. At the frequency of $f > 1/2\pi R_f C_f$, it is simplified as [23]:

$$\overline{V_{n,LNA}^2} = \left|\frac{C_{in} + C_f + C_p}{C_{in}}\right|^2 . \overline{V_{n,A1}^2} \tag{9}$$

In order to reduce the input-referred noise of the LNA, the input-referred noise of the operational transconductance amplifier should be reduced. Also, the value of input capacitance C_{in} should be very large compared to the feedback capacitance C_f. Of course, by choosing a larger input capacitor than the feedback capacitor, the closed-loop gain will be increased. But increasing the gain causes large LFP signals to saturate the amplifier output and the result of this is the loss of signal information. The equivalent PSD of input-referred noise of the folded-cascode operational amplifier is given by Ref. [24]:

$$\overline{V_{n,A1}^2}(f) = \frac{K_{F1}}{C_{OX}W_1 f}\left[\frac{1}{L_1} + \left(\frac{K_{F3}\mu_n}{K_{F1}\mu_p}\right)\left(\frac{I_{D3}}{I_{D_1}}\right)\frac{L_1}{L_3^2} + \left(\frac{K_{F9}}{K_{F1}}\right)\left(\frac{I_{D9}}{I_{D_1}}\right)\frac{L_1}{L_9^2}\right] + \frac{4kT\gamma}{g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}}\right) \tag{10}$$

where K_F is the flicker noise coefficient, W is the channel width, L is the channel length, C_{ox} is the gate oxide capacitance per unit area, μ is the effective mobility, I_D is the drain current, and g_m is the transconductance of the MOS transistor. According to the relation (10), the flicker noise can be reduced by choosing the appropriate ratio of the bias currents of the transistors. In this design, the bias current of the input transistors $M_{1,2}$ is greater than the bias currents of active load transistors $M_{9,10}$. For example, the current of each input transistor is 0.9 μA, whereas the current of each active load transistor is 40 nA. In fact, the current of input transistors is 22 times larger than the load transistors. On the other hand, the channel length of M_1 and M_2 input transistors should be smaller than the channel length of the $M_{3,4}$ and $M_{9,10}$ current source transistors. The channel width of the input transistors also should be chosen large enough to reduce the flicker noise of these transistors that have a dominant contribution to the total flicker noise. To reduce the thermal noise, according to relation (10), the transconductance of the input transistors should be greater than the transconductance of the active load transistors. Although this reduces the total noise, the power consumption should be considered in order to not to increase excessively.

2.3. Band-pass filter

Fig. 15 shows the structure of the proposed band-pass filter which is used in the second stage of analog front-end. In this structure, pseudo-resistor bias voltages are generated by the bias circuit of Fig. 8. The gain of this stage is about 3 dB, so a single complementary structure is used for the pseudo-resistor. This filter has been designed to tune the high cut-off frequency of the overall system. Although the high cut-off frequency can be decreased by increasing the value of output capacitor in the AFE, it increases the die area.

As shown in Fig. 16, a single-ended folded-cascode amplifier is utilized to realize the band-pass filter. In this structure, a bias circuit is used to provide the bias current of the input transistors and other transistors. By controlling this bias current, the transconductance of the OTA can be changed, and hence, the change in the bandwidth of the filter is resulted. In the first case, to amplify the low frequency signals like LFPs, the current of the input transistors is in a low state, and it is equal to 10 nA. In this case, the switches S_4 and S_5 are opened. Also, when the interface circuit receives both LFP and AP signals, the switches S_4 and S_5 are closed, and the current is in its highest state which is equal to 210 nA. Changing the current of the input transistors from 210 nA to 10 nA

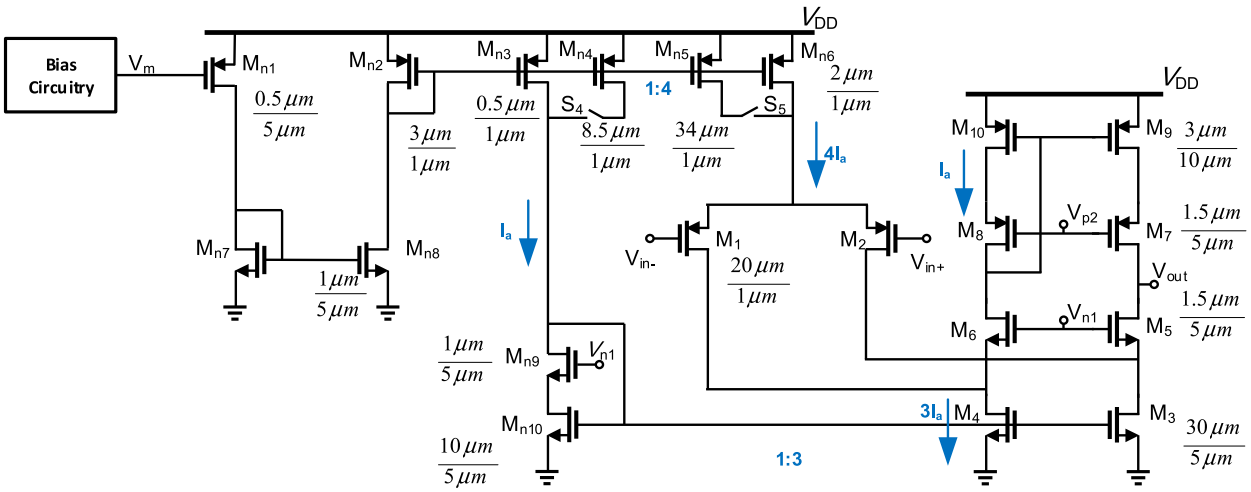

Fig. 16. The operational amplifier used in the band-pass filter for tuning the high cut-off frequency and the power consumption.

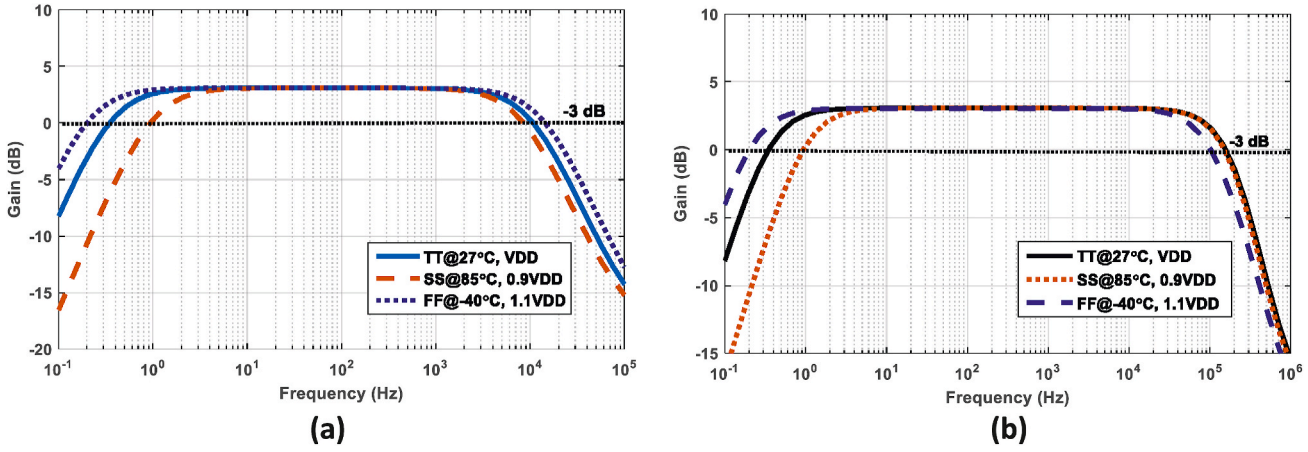

Fig. 17. The frequency response of the band pass filter in PVT variations: (a) low recording mode and (b) high recording mode.

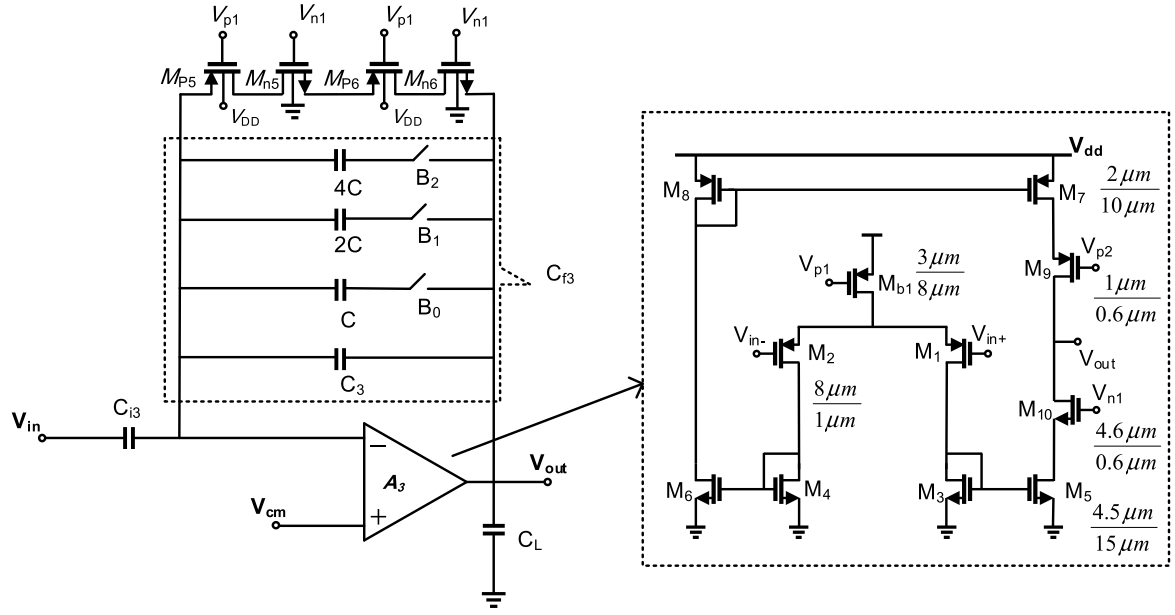

Fig. 18. The VGA structure and its operational amplifier.

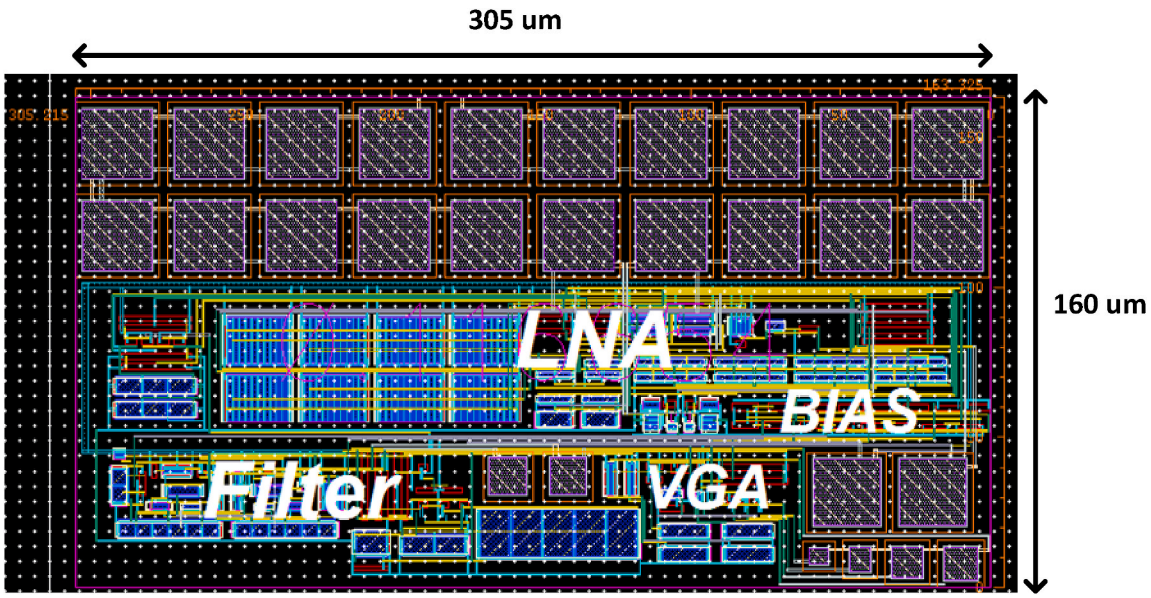

Fig. 19. The layout of the proposed front-end amplifier.

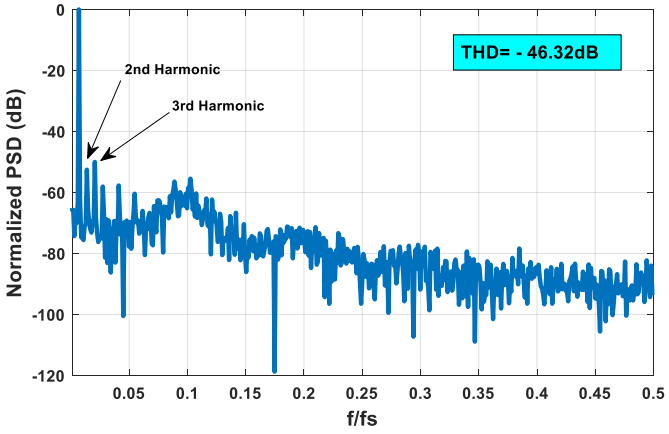

Fig. 20. Simulated output PSD of the proposed analog front-end.

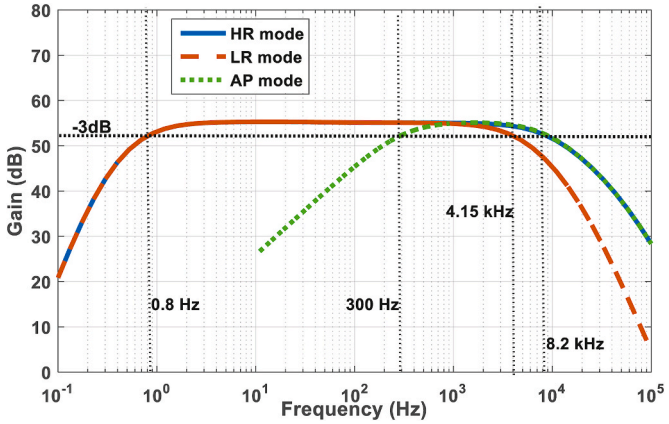

Fig. 21. Frequency response of the front-end amplifier with tuneable low and high cut-off frequencies.

reduces the power consumption of the filter considerably. According to Equation (6), the high cut-off frequency of the amplifier depends on its transconductance. Therefore, by varying the transconductance, the high

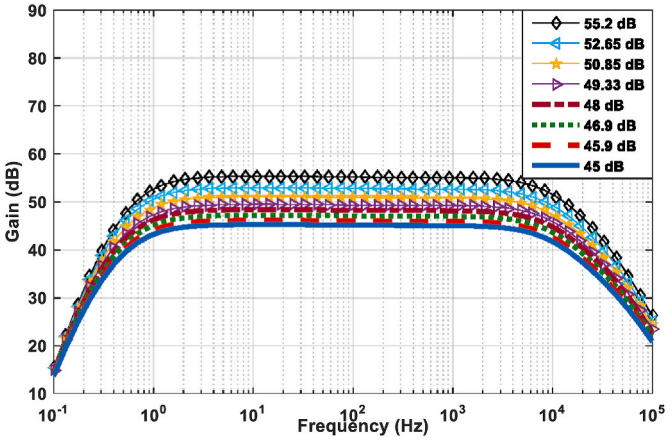

Fig. 22. The frequency response of the AFE with 8 programmable gains.

cut-off frequency can be changed. Overall, with the programmable high and low cut-off frequencies, the front-end amplifier can separate the neural signals. For example, to amplify the AP signals, the low cut-off frequency can be increased up to 300 Hz, and for the LFP signals, the filter can reduce the high cut-off frequency and power consumption to amplify them.

Fig. 17 shows the frequency response of the BPF over PVT variations in the HR and LR modes. As it is seen, the low cut-off frequency of filter has less variation because of the proposed pseudo-resistor. In fact, this figure shows the frequency response of the BPF without LNA and VGA.

2.4. *Variable gain amplifier*

The VGA is utilized at the third stage of the analog front-end just before the analog-to-digital converter (ADC). The VGA relaxes the input dynamic range of the ADC, and hence, the required ADC's resolution. Fig. 18 shows the VGA structure where three binary-weighted capacitors are switched in the feedback path to change the gain as:

$$A_{VGA} = \frac{-C_{f3}}{C_{f3}} \tag{11}$$

where C_{f3} is the equivalent feedback capacitance that is controlled by

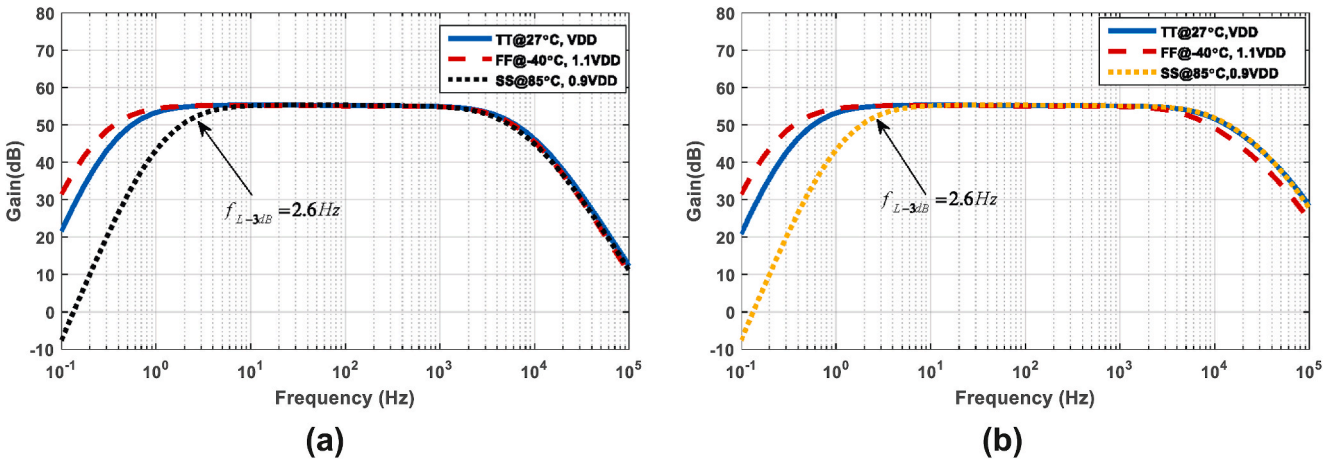

Fig. 23. The frequency response of the front-end amplifier in PVT variations: (a) low recording mode and (b) high recording mode.

Table 2
Performance summary of the front-end amplifier in the HR and LR modes in process corners and power supply variations at 37 °C.

High recording mode			
Parameter	FF (V_{DD} = 1.1 V)	SS (V_{DD} = 0.9 V)	TT (V_{DD} = 1 V)
Midband gain (dB)	55.2	55.2	55.2
Low cut-off frequency (Hz)	1	0.58	0.8
High cut-off frequency (kHz)	6.16	9.1	8.2
Power (μW)	5.85	2.24	3.6
THD (dB)	−43.45	−38.56	−46.32
Input referred noise (μV_{rms})	1.86	2.31	2.1
Low recording mode			
Midband gain (dB)	55.2	55.2	55.2
Low cut-off frequency (Hz)	1	0.58	0.8
High cut-off frequency (kHz)	3.27	4.56	4.15
Power (μW)	4.73	1.3	2.9
THD (dB)	−39.83	−34.32	−43.70
Input referred noise (μV_{rms})	1.51	1.88	1.7

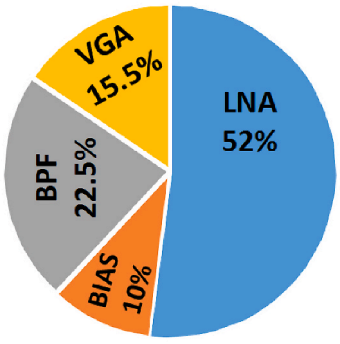

Fig. 24. The distribution of power consumption for the analog front-end.

three bits. As shown in Fig. 18, a single-ended current-mirror OTA with cascode transistors at the output branch is utilized to realize the VGA.

3. Post layout simulation results

The purpose of the design is to realize an analog neural recording circuit that can amplify the neural signals with variable amplitude and

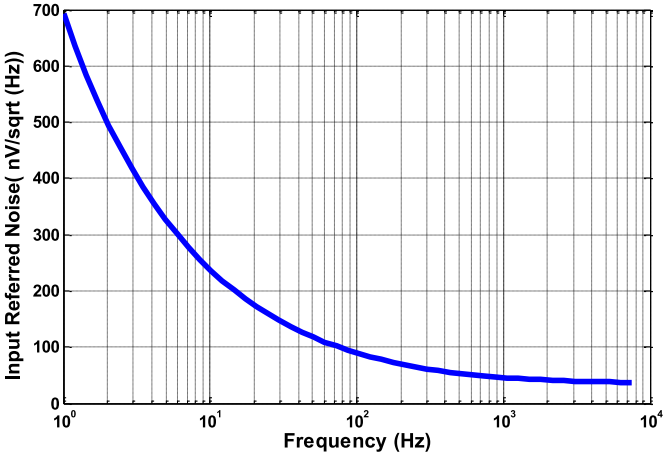

Fig. 25. The input-referred noise of the analog front-end.

frequency. The front-end consists of three main blocks, which are LNA, band-pass filter and VGA. The overall gain is divided into the blocks, so that the LNA has 42 dB gain, the band-pass filter has 3 dB and the VGA has a gain between 0 dB and 10 dB. Due to the fact that neural signals have a background noise between 5 and 10 μV [15], in this design, it has been tried to make the noise less than 5 μV, which ultimately the total input-referred noise of the whole system is 2.1 μV_{rms}. As mentioned earlier, the amplitude of neural signals is very variable, and hence, linearity is very important. On the other hand, in recent works, the reported value of THD is about −40 dB while in this design, the achieved THD value of the whole system is about −46.3 dB. Power consumption should also be as low as possible in implanted systems.

The proposed analog front-end has been designed and simulated in Cadence Spectre RF with TSMC 0.18 μm CMOS process. The layout of the proposed front-end amplifier is shown in Fig. 19 which occupies 305 μm × 160 μm silicon die area. Due to the importance of the symmetry for input transistors of LNA, the fingering method is used in the layout and each transistor is divided into 4 transistors. Metal-insulator-metal (MIM) capacitors have been used to implement to required capacitors. Regular NMOS and PMOS transistors are used with 1 V supply voltage. All device parameters are also shown in their related circuit schematics.

Fig. 20 shows the simulated normalized output power spectral density (PSD) of the proposed analog front-end. The THD value is −46.32 dB and the input signal is a sinusoidal with amplitude of 1 mV_{pp} at 1 kHz frequency, and f_s is the sampling frequency. When the 1 mV_{pp} input signal is applied, the output voltage swing is about 0.6 V_{pp}. In large

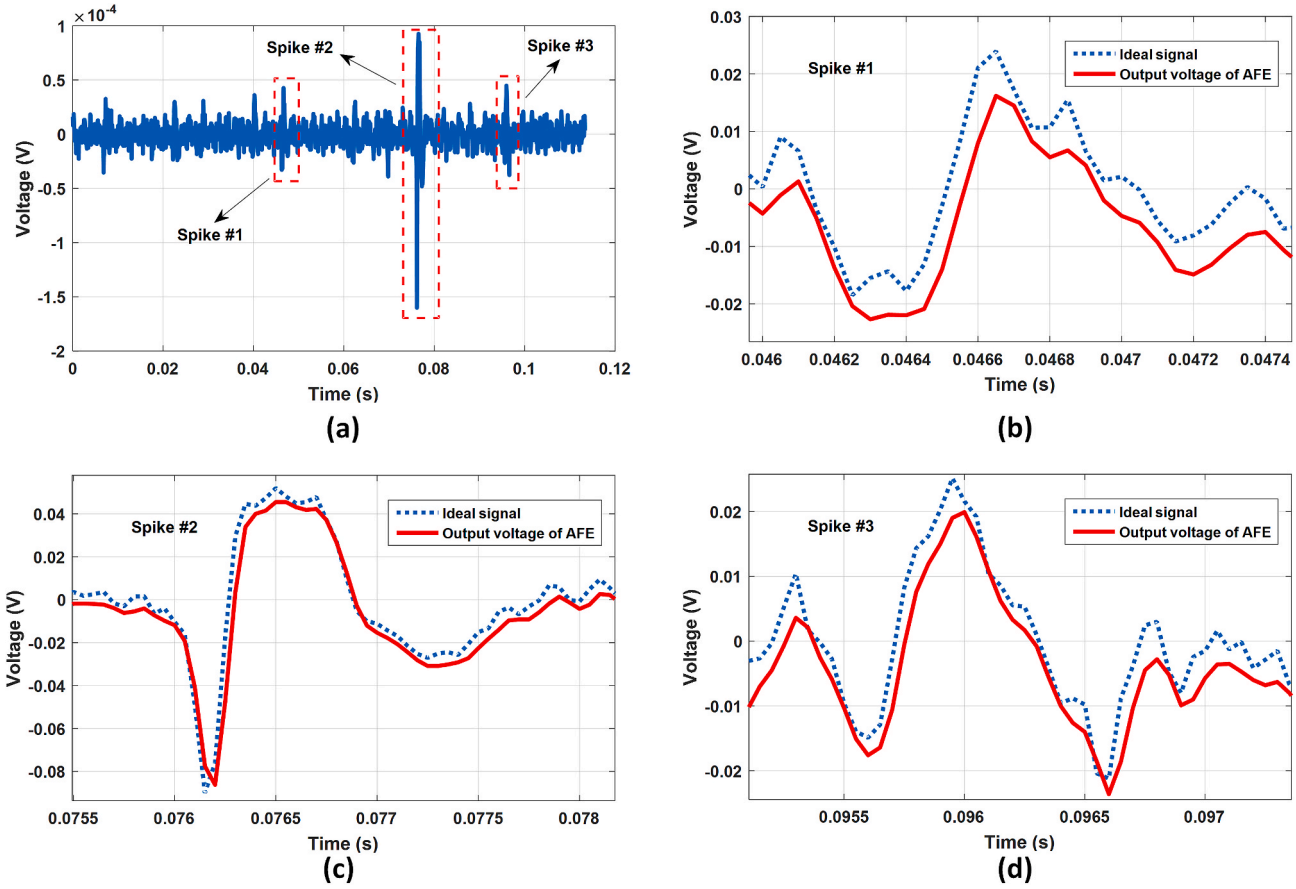

Fig. 26. (a) The real neural signal as input signal for the AFE and (b, c, d) comparison of output voltage of the AFE with the ideal signal.

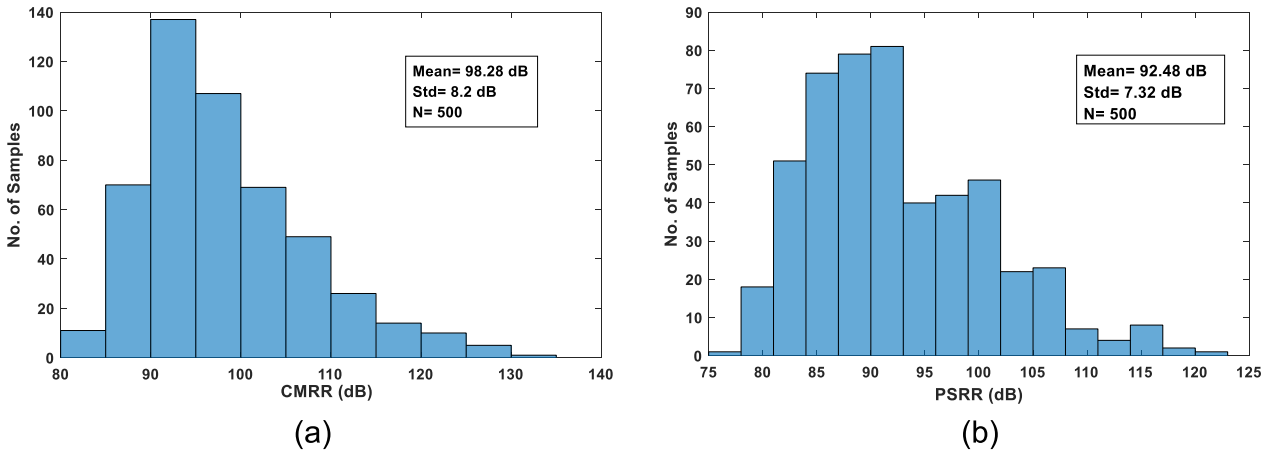

Fig. 27. Monte Carlo simulation results for (a) CMRR and (b) PSRR at the frequency of 50 Hz.

output voltage swing mode which is about 0.8 V_{pp} (80% of V_{DD}), the analog front-end still has a high linearity and the achieved THD is about −42.7 dB.

Fig. 21 shows the frequency response of the front-end amplifier with tuneable low and high cut-off frequencies. The low cut-off frequency is adjustable to 0.8 and 300 Hz. According to the figure, in the high recording mode, the whole neural signals such as LFP and AP can be amplified simultaneously. In the low recording mode, the filter can also reduce the high cut-off frequency and power consumption to amplify the signals at low frequencies like LFPs. Finally, in the AP mode, the low cut-off frequency is increased to 300 Hz to amplify the signals with high frequencies like AP.

Fig. 22 shows 8 programmable gains of the proposed AFE. The gain added by the VGA is between 0 dB and 10 dB. So the gain of the entire system is between 45 dB and 55 dB. Fig. 23 shows the frequency response of the overall system over PVT variations in the LR and HR modes. Table 2 has been provided to evaluate the AFE characteristics in process corners and power supply variations. Assuming ±10% variations in the supply voltage with a value of 1 V, values of 0.9 V and 1.1 V have been applied to the supply voltage. According to this table, by decreasing the supply voltage, the bandwidth decreases and the noise also increases, but by evaluating the circuit characteristics provided in

Table 3
Performance comparison of the proposed front-end amplifier with some state-of-the-art works.

Reference	Tech. (μm)	Supply Voltage (V)	Power Consumption (μw)	Midband Gain (dB)	Low-pass f_{-3dB} (Hz)	High-pass f_{-3dB} (kHz)	THD (dB) ($1mV_{pp}$ @ 1 kHz)	Input-referred Noise (μV_{rms})	NEF	CMRR (dB)	PSRR (dB)	$(NEF)^2 V_{dd}$	Area (mm^2)
JSSC′03 [9]	1.5	±2.5	80	39.5	0.025	7.2	−40[a]	2.2	4	>83	>85	80	0.16
TBCAS′11 [23]	0.18	1.8	10.15	49/66	0.12/350	0.29/12	–	5.4–11	4.4–5.9	62	72	52	0.033
JETCAS′11 [8]*	0.18	1.8	20.8	52–57	4/300	10	−46.24[b]	2.6	3.38	88	85	20.5	0.0611
TCASI′13 [34]	0.18	1.8	11	48–60	1	9	−38.4	5	4.6	48	55	38.1	0.065
TBCAS′15 [32]	0.35	3	12.9	53	10	5	−41.9	7.99	8.9	60	–	237	0.035
TCASII′15 [31]	0.09	1	2.85	58.7	0.49	10.5	−35.9	3.04	1.93	>45	>50	3.72	0.137
TCASII′17 [28]	0.13	1	11	44	20	15	−41.9	3	–	–	–	–	0.07
LASCAS′17 [29]*	0.18	1	2.2	49–55	0.5	7	−40	3.1	2	–	–	4	–
JSSC′18 [33]	0.13	1.2	11.2	46	0.5/400	7	−40.4[c]	3.2	2.3	71.7	–	6.35	0.03
JSTS′18 [13]	1	0.18	2.28	43–61	1/220	0.53/8.9	–	4.74	2.91	90.2	77.8	8.46	0.16
ISCAS′19 [12]	0.065	0.35/0.7	0.34	40–54		6.5	–	6.7	2.75	78	74	3.49	0.04
LASCAS′19 [10]	0.18	1	0.815	40.4	1/200	0.7/0.95/5	−40	4.1	–	68	–	–	–
MWSCAS′19 [30]	0.5	3.3	4.12	52.53	0.1	5	–	3.16	2.53	97.1	84.4	32.95	0.28
AEU′18 [27]*	0.065	1	1.12	40	0.66	5	–	8.1	4.62	124	88	21.34	0.065
CSSP′20 [35]*	0.35	3	28.8	34	0.05	8.8	−40	3	3.81	118	119	43.55	0.053
AEU′18 [3]*	0.18	1	0.963	62–74	0.232	0.235	−41.27	1.33	3.34	88	101	9.06	3.04
MEJO′20 [36]	0.18	1	2.82	45–63	1/800/1000	0.5/5.8/8/9	−41	3.6	2.04	80	70	4.16	0.21
MEJO′20 [11]*	0.13	+1.2	1.9	58.4–79.5	0.36/480	0.33/8.7	–	1.1	1.47	110	87	2.593	0.01
MEJO′19 [5]*	0.18	±1.2	7.68	59.7	102	10	–	3.87	2.65	50	53	16.854	0.021
This work*	0.18	1	3.6	45–55	0.8/300	4.15/8.2	−46.32	2.1	1.7	98.28	92.48	2.89	0.048

* Simulation results.
[a] 16.7 mV_{pp} @ 1 kHz.
[b] Output voltage swing 1 V_{pp} (0.55% of V_{DD}) @ 300 Hz
[c] 5 mV_{pp} @ 1 kHz.

the table, the proposed AFE is almost robust to process and voltage variations.

Fig. 24 shows pie diagram of the power consumption for the proposed blocks in the AFE. The total power consumption is 3.6 μW and according to this figure, the LNA consumes more than half of the total power consumption because the input-referred noise contribution of this block is more than the other blocks in the total input-referred noise of the AFE. Fig. 25 shows the PSD of the input-referred noise of the front-end amplifier. The total input-referred noise is 2.1 μV_{rms} over the 0.5 Hz-8.2 kHz frequency range for the HR mode, and it is 1.7 μV_{rms} over the 0.5 Hz-4.15 kHz frequency range for the LR mode.

To evaluate the performance of the AFE, a real pre-recorded neural signal is applied to the electrodes that are located before the input of the LNA. This real neural signal is shown in Fig. 26(a), and it has the sampling frequency of 20 kS/s. These samples belong to a guinea pig that has been recorded intracortically from its auditory cortex [6]. Fig. 26(b, c, d) shows the output voltage waveform of the AFE and the ideal signal. In fact, the ideal signal is the product of the real neural signal multiplied by the gain of AFE. According to this figure, the AFE is able to amplify the real neural signal as well.

Fig. 27 shows Monte Carlo simulation results of CMRR and PSRR with considering both the device mismatches and process variations. The mean value and standard deviation of CMRR are 98.28 dB and 8.2 dB, respectively, for 500 runs at the frequency of 50 Hz. The mean value and standard deviation of PSRR are also 92.48 dB and 7.32 dB, respectively.

The trade-off between noise and power consumption is a challenge in the neural recording design. The important figure of merit to compare noise, bandwidth and current supply is the noise efficiency factor (NEF) and it is defined as [25]:

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi . V_T . 4kT . BW}} \tag{12}$$

where $V_{ni,rms}$ is the input-referred noise, I_{tot} is the total current consumption and V_T is the thermal voltage, k is the Boltzmann constant, BW is the bandwidth of amplifier over which the noise is integrated. Also, the power efficiency factor (PEF) is a figure of merit to compare the amplifiers with different supply voltages. It is given by Ref. [26]:

$$PEF = (NEF)^2 V_{dd} \tag{13}$$

where V_{dd} is the supply voltage. In this work, the achieved NEF and the PEF are 1.7 and 2.89, respectively. In order to compare the achieved specifications of the proposed structure with the state-of-the-art works, Table 3 is presented. For a fair comparison, some references with simulation results such as [3,5,8,11,27,29], and [35] are included in this

table. One of the most important design specifications is the amount of linearity that should be taken into account along with other design parameters such as power consumption, bandwidth, and input-referred noise. For example, the linearity has not been considered in some references such as [5,11–13,27], and [30]. On the other hand, some references such as [3,5,27], and [35] don't have tunable low and high cut-off frequencies to program their AFEs according to the neural signals. The parameters NEF, PEF, and the THD of this work have been improved compared to the references [3,5,27,35]. The THD value of the references such as [3,29], and [35,36] is about −40 dB, while the THD value of proposed AFE is −46.3 dB. Moreover, The THD in Ref. [8] is equal to −46.24 dB, but its pseudo-resistor value is not large enough, and its low cut-off frequency is about 4 Hz. In this work, the pseudo-resistors have large resistance values, and the low cut-off frequency is below 1 Hz.

4. Conclusion

In this paper, an analog front-end has been designed for implantable neural recording applications. The proposed amplifier consists of three stages. In designing these blocks, optimization of important parameters such as power consumption, input-referred noise, linearity, and bandwidth has been considered. The gain and bandwidth of the system can be changed to amplify the neural signals as well. The total gain is between 45 dB and 55 dB. A programmable pseudo-resistor is used for the LNA to tune the low cut-off frequency of the system. Also, by changing the transconductance of the OTA with the band-pass filter, the high cut-off frequency of the system is variable to program the power consumption. The low cut-off frequency is adjusted to 0.8 and 300 Hz and the high cut-off frequency is able to separate the neural signals. The high cut-off frequency in the low and high recording modes is 4.15 kHz and 8.2 kHz, respectively.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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