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A 4-channel neural amplifier employing partial OTA sharing structure with variable gain and bandwidth for implantable neural recording applications

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ABSTRACT

Objective: The design of a low-noise low-power 4-channel neural amplifier with variable bandwidth and gain for multi-channel electrode arrays is presented with application in recording of neural signals.
Methods: To amplify neural signals with low amplitudes and frequencies, pseudo-resistors are used in the neural amplifier, creating a small low cut-off frequency. The neural amplifier is designed to amplify wide range of neural signals, including Local Field Potential (LFP) and Active Potential (AP) signals, with sufficient gain. In the design process of the proposed amplifier, important parameters such as noise, power consumption, and linearity have been considered and improved to make the proposed structure efficient. The suggested amplifier utilizes an OTA sharing structure where the common parts of amplifiers in distinct channels are shared. The advantage of this structure is that it minimizes the die area and power dissipation of the neural recording system to a significant extent. In addition, the attenuator circuit used in the feedback path can increase the mid-band gain for amplifying low-amplitude neural signals such as LFPs. This avoids the need to increase the value of the input capacitor in order to enhance the mid-band gain, preventing the increase in die area and the decrease in the input impedance of the amplifier. The 4-channel neural amplifier is designed and simulated in 180 nm TSMC CMOS technology.
Results: The neural amplifier has a mid-band gain of 47 dB with 3 Hz to 10.8 kHz bandwidth without using an attenuator circuit, and by using the attenuator, the mid-band gain is increased to 55 dB and the bandwidth is decreased to 4 kHz. The power dissipation of each channel is 2.4 μW from 1-V supply voltage. The input-referred noise is 1.9 μV_{rms} over the 3 Hz-10.8 kHz frequency range, and it is 1.45 μV_{rms} over the 11 Hz-4 kHz frequency range when the attenuator circuit is active in the feedback path.

1. Introduction

Neurological disorders have affected a great number of people's lives throughout history, regardless of their gender, age, and even geographical region [1]. Treatment methods like pharmacy and brain surgery have been utilized for some disorders, including Epilepsy and Alzheimer's disease [2,3]. Nevertheless, drugs have side effects, and patients would become resistant to them after a while. Brain surgery can be effective in some cases, but in many cases, the origin of neurological disorders is near a significant part of the brain where brain surgery can cause harmful consequences due to the sensitivity of neurons [4,5].

In recent decades, thanks to technological advancements, recording brain activities and monitoring neurological disorders have been introduced as promising methods for people who suffer from such brain-related disorders. In order to have proper diagnostics, a high amount of data received from the brain should be gathered, which requires a high amount of power consumption by circuits implemented in the brain, including recording channels, stimulation channels, signal processing units, and wireless power/data section [6,7]. However, there is a serious limitation in terms of power since the temperature of implanted

Abbreviations: AP, Action Potential; ADC, Analog-to-Digital Converter; AFE, Analog Front-End; BPF, Band Pass filter; CMFB, Common-Mode Feedback Circuit; CMRR, Common-Mode Rejection Ratio; DAC, Digital-to-Analog Converter; DR, Dynamic Range; FoM, Figure of Merit; LFP, Local Field Potential; LNA, Low Noise Amplifier; MIM, Metal Insulator Metal; NEF, Noise Efficiency Factor; OTA, Operational Transconductance Amplifier; PEF, Power Efficiency Factor; PSD, Power Spectral Density; PSRR, Power Supply Rejection Ratio; THD, Total Harmonic Distortion.

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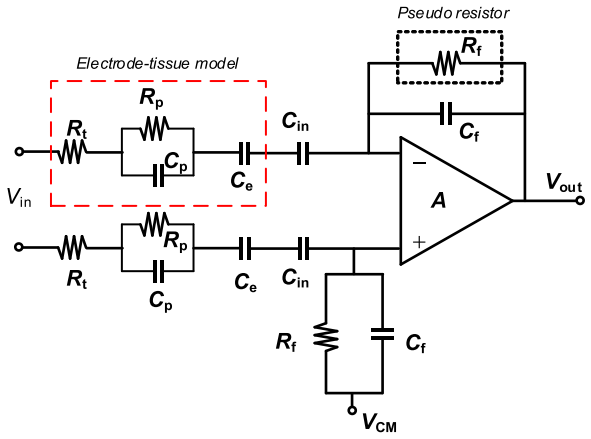

Fig. 1. The conventional structure of a neural amplifier with equivalent circuit of electrode-tissue interface [8].

devices should not exceed 1°C more than that of nearby tissues [4,8]. Otherwise, tissues in the brain would be negatively affected and even damaged due to the heat dissipated by the device inside the brain. In other words, the maximum power density should be less than 0.8 mW/mm^2 to prevent such a negative effect [3,9].

Many authors have developed and introduced a variety of structures regarding analog front-end (AFE) for implantable recording systems during recent decades. In [10], a new active ground is utilized to maintain the input common-mode voltage near the analog ground, which can enhance the common-mode rejection ratio (CMRR) value of the system to a significant extent. However, adding such an active ground at the input of the amplifier not only generates extra noise besides the noise introduced by the electrodes but also increases the silicon area. In [11], an operational transconductance amplifier (OTA) sharing structure is used in an active integration circuit without using large DC blocking capacitors at the input of the amplifier. But it has several feedback amplifiers, resulting in enhancing the complexity of circuit implementation and power dissipation.

Implantable recording systems transmit data wirelessly through a telemetry system, paving the way for high transmitted data rate. In [12–14], implantable antennas are presented that are not only compact, flexible, and biocompatible but also transmit data over a wide range of frequencies. Implantable antennas have also beneficial applications in healthcare. In [15], a new antenna design for cancer detection is proposed. It uses a new type of medical imaging technique, and the antenna design is a key part of this imaging system.

In [16], a 32-channel neural recording system is implemented, and the gain and bandwidth of each amplifier can be tuned based on the type of neural signals, including local field potentials (LFPs) and action potentials (APs). However, the system is tunable by changing the capacitance value of the input capacitor and feedback capacitor, which enhances the die area due to the use of large capacitors. In [9], a neural amplifier using an OTA sharing architecture is presented. Based on the theoretical analysis of the circuit, this method results in improvements in the efficiency of the system in terms of linearity, channel crosstalk, and noise efficiency factor (NEF) values. However, the amplifier in this reference is telescopic-cascode, which has a limited output swing range. Moreover, it needs different input and output common-mode voltages to improve the voltage headroom at the output of the amplifier.

In this paper, a neural amplifier with an OTA sharing structure is presented, which has variable bandwidth and gain by means of an attenuator circuit used in the feedback path in series with feedback capacitors. Without any needing to the change of the capacitance value, the gain and bandwidth are tuned. The rest of this paper is arranged as follows. In Section 2, the design, analysis, and structure of the suggested neural recording amplifier are demonstrated. The detailed post-layout simulation results are presented in Section 3. Finally, the conclusion is given in Section 4.

2. Suggested neural recording amplifier

2.1. Conventional structure

Neural signals should be amplified to be processed in the next blocks, like an analog-to-digital converter (ADC). The frequency content of these signals is located in a few Hz to several kHz. Neural signals are divided into two types: local field potential and action potential [17,18]. The frequency range of LFPs is less than a few hundred Hz, while it is usually between 300 Hz and 10 kHz for APs [8,18].

Fig. 1 depicts the conventional architecture of a neural amplifier, where C_{in} and C_f are input and feedback capacitors that set the mid-band gain of the amplifier. R_f is the equivalent resistance of the pseudo-resistor. It has a high resistance value and can be implemented by using non-tunable and tunable structures. Unlike passive resistors, this diode-connected structure can easily be implemented with a minimum occupied silicon area and add a small amount of noise to the output of the amplifier. However, when the amplitude of the input signal enhances, the voltage changes on the transistors used in pseudo resistors are increased, which can negatively affect the linearity of the system. The equivalent circuit of the electrode-tissue interface is also shown in Fig. 1. Through extracellular recording, a great number of electrodes, known as microelectrode arrays, can be placed near neurons without penetrating their cells. This is a safe method for large-scale recording that is suitable to acquire a large amount of data [4]. Given that the impedance of electrodes varies according to their positions in the nerve, there would be an impedance mismatch at the input of the amplifier, which can result in a decrease in the CMRR value [19]. The mid-band gain of the amplifier is given by the ratio of the input capacitor to the feedback capacitor. Therefore, to have a sufficient gain, the input capacitor should be larger than the feedback capacitor. However, the increase in the input capacitor can reduce the input impedance of the amplifier, which is not desirable since the input impedance of the amplifier should be larger than that of the electrodes to avoid signal attenuation [20].

The low cut-off frequency of the amplifier relies on the value of pseudo resistor and feedback capacitor and is given by

$$f_L = \frac{1}{2\pi C_f R_f} \tag{1}$$

When the capacitance value of input capacitor and output capacitor of the amplifier is larger than that of feedback capacitor, the high cut-off frequency is approximately obtained as

$$f_h = \frac{G_m}{2\pi C_L A_v} \tag{2}$$

where G_m and A_v are the transconductance of the OTA and its mid-band gain, respectively. Based on the above equation, the bandwidth can be enhanced if the transconductance is increased, requiring a high amount of power consumption. This amplifier is called a capacitive-feedback amplifier and acts like a band-pass filter. It has a very small low cut-off frequency due to the large resistance value of pseudo-resistors. Consequently, neural signals with low frequencies can be amplified properly, and the large DC offset voltage introduced by the electrodes can be eliminated at the same time, preventing amplifier saturation and signal distortion. Nonetheless, the conventional structure shown in Fig. 1 is not suitable for multi-channel electrode arrays given that each amplifier needs two large input capacitors, and the part of the reference electrode would consume a significant amount of power [9,11]. Thus, the complexity of design, power consumption, and occupied silicon area would increase by using such a structure for multi-channel electrodes where a high number of channels are needed.

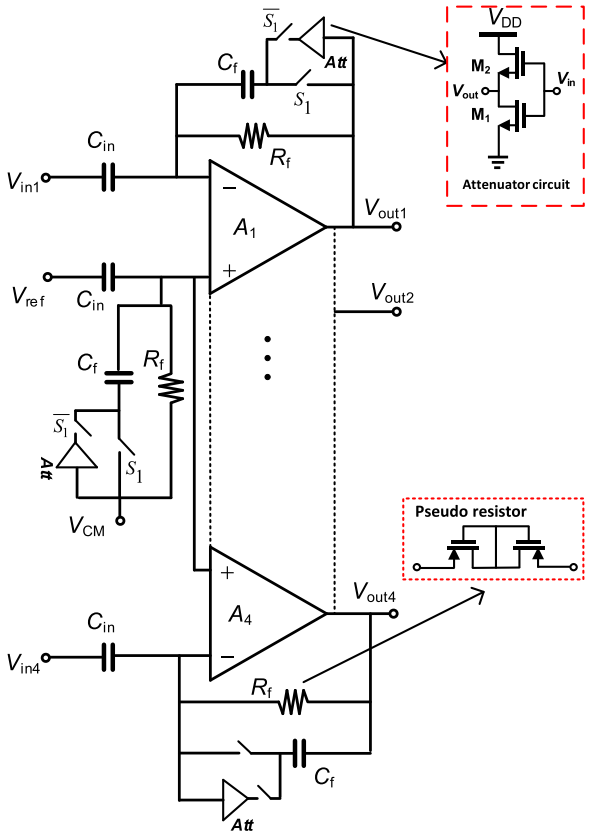

Fig. 2. The proposed neural amplifier with OTA sharing structure.

2.2. Proposed neural amplifier

The structure of the suggested neural amplifier is shown in Fig. 2. The partial OTA sharing method is used for the entire structure where the common parts of amplifiers are shared, meaning that multiple amplifiers can have the same passive parts corresponding to the reference electrode. As a result, this structure just needs one single input capacitor related to the passive part for all amplifiers, which can reduce the power consumption and die area to a significant extent. This is suitable for multi-channel electrode arrays where a large number of neural recording amplifiers are needed to amplify neural signals. In fact, OTA sharing architecture can help to develop the number of recording amplifiers with a limited power budget that exist for the design of neural recording systems.

Four amplifiers are used in the proposed structure, and only one input capacitor is used for all amplifiers. The non-tunable pseudo-resistors structure implemented by two series PMOS transistors is parallel with feedback capacitors, creating the low cut-off frequency of the amplifier. Each channel has an attenuator circuit that can be utilized for changing the mid-band gain and bandwidth. When $S_1 = 1$, the attenuator circuit is located in the feedback path, increasing the mid-band gain and decreasing the bandwidth at the same time. This is beneficial for the amplification of neural signals with low frequencies and amplitudes like LFPs since these signals need a higher gain. Although the mid-band gain and bandwidth can be changed by changing the capacitance values that exist at the output and input of amplifiers, this method can increase the die area and reduce the input impedance of the amplifier, which is not a proper solution for increasing the mid-band gain given that it also leads to the attenuation of neural signals at the input. Adding an attenuator to the feedback path cannot affect the die area because it is implemented with NMOS transistors. As mentioned in the previous section, the mid-band gain is set by the ratio of the input capacitor and the feedback capacitor. In this design, the input and feedback capacitors are 50 pF and 0.2 pF, respectively.

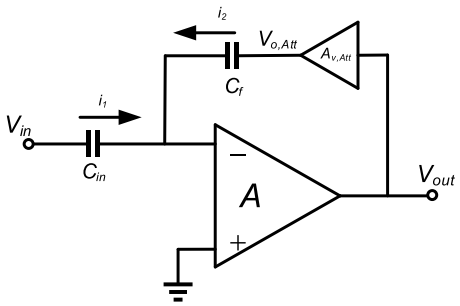

Fig. 3. The structure of neural recording amplifier using the attenuator circuit in series with feedback capacitor.

Fig. 3 shows the neural amplifier when the attenuator circuit is in series with the feedback capacitor. The voltage gain of the attenuator circuit is approximately obtained as [21]

$$A_{v,att} = 1 - \sqrt{\frac{(W/L)_{M1}}{(W/L)_{M1} + (W/L)_{M2}}} \tag{3}$$

where W/L refers to the aspect ratio of M_1-M_2 transistors used in the attenuator circuit. The mid-band gain of the amplifier is given by

$$A_V = \frac{-C_{in}}{C_f A_{v,Att}} \tag{4}$$

where $A_{v,att}$ is the gain of the attenuator circuit. Therefore, the attenuator circuit can increase the mid-band gain of the amplifier. Additionally, the attenuator block can change the bandwidth of the amplifier. The low cut-off frequency and high cut-off frequency are obtained, respectively, as

$$f_L = \frac{1}{2\pi R_f C_f A_{v,att}} \tag{5}$$

$$f_h = \frac{G_m C_f A_{v,att}}{2\pi C_L C_{in}} \tag{6}$$

Based on the above equations, the bandwidth of amplifier can be reduced when the attenuator circuit is added into the feedback path, which is proper for amplification of neural signals with low frequencies and low amplitudes like LFPs that need a larger gain.

2.2.1. Proposed low noise amplifier

Fig. 4 shows the schematic circuit of the low noise amplifiers (LNAs) used in the structure illustrated in Fig. 2. A single-ended folded-cascode OTA has been used for each channel. Fully-differential amplifiers have better performance in terms of CMRR, but these amplifiers require a common-mode feedback (CMFB) circuit, that increases the total power dissipation and occupied die area. Three main single-stage OTAs including telescopic-cascode, current mirror, and folded-cascode architectures can be used for implementing an amplifier in neural recording systems. Compared to the folded-cascode OTA, although the telescopic-cascode amplifier has better performance in terms of power consumption and input-refereed noise, it has limited output swing and needs a larger power supply voltage to provide sufficient voltage headroom for biasing [19]. In neural recording systems, the folded-cascode OTA is mainly utilized since it has larger output swing, CMRR, and linearity, which are required for amplifying wide range of neural signals with different amplitudes in the presence of large common-mode interferences [8,11,22,23]. As a result, the single-ended folded-cascode OTA is a proper structure for neural recording systems.

Fig. 5 shows the bias circuit of the main amplifier. Wide-swing cascode current mirrors are utilized to properly generate the bias voltages of the main amplifier. Actually, there is a current mirror ratio between

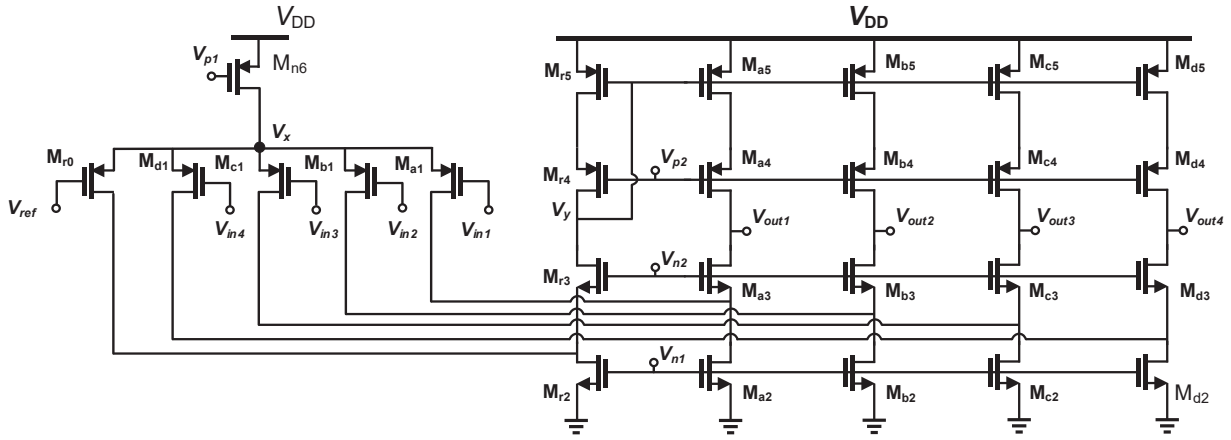

Fig. 4. The proposed neural LNA with OTA sharing method.

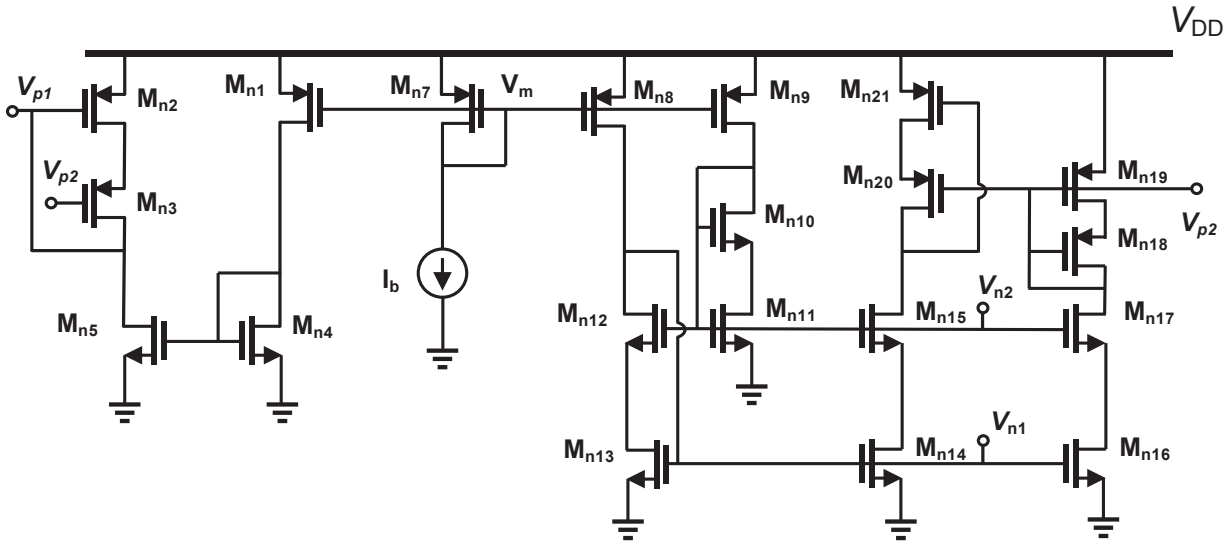

Fig. 5. Bias circuit of the folded-cascode OTA.

Table 1
Sizing of the OTA and the bias circuit.

Transistors	W/L	Transistors	W/L
M_{r0}, M_{a0}, M_{b0}, M_{c0}, M_{d0}	300 μm/ 1 μm	M_{n7}	1 μm/ 5 μm
M_{r2}, M_{a2}, M_{b2}, M_{c2}, M_{d2}	30 μm/ 1 μm	M_{n8}	1 μm/ 5 μm
M_{r3}, M_{a3}, M_{b3}, M_{c3}, M_{d3}	1.1 μm/ 0.3 μm	M_{n9}	1 μm/ 5 μm
M_{r4}, M_{a4}, M_{b4}, M_{c4}, M_{d4}	7 μm/ 0.3 μm	M_{n10}	0.3 μm/ 6 μm
M_{r5}, M_{a5}, M_{b4}, M_{c4}, M_{d4}	3.5 μm/ 10 μm	M_{n11}	0.3 μm/ 6 μm
M_1	1 μm/ 5 μm	M_{n12}	0.5 μm/ 5 μm
M_2	2 μm/ 5 μm	M_{n13}	1 μm/ 5 μm
M_{n1}	3.2 μm/ 5 μm	M_{n14}	0.6 μm/ 5 μm
M_{n2}	5 μm/ 1 μm	M_{n15}	0.6 μm/ 5 μm
M_{n3}	5 μm/ 0.5 μm	M_{n16}	0.9 μm/ 5 μm
M_{n4}	1.2 μm/ 2.8 μm	M_{n17}	0.9 μm/ 5 μm
M_{n5}	4.2 μm/ 2.8 μm	M_{n18}	1.4 μm/ 5 μm
M_{n6}	100 μm/ 1 μm	M_{n19}	1.4 μm/ 5 μm
M_{n6}	100 μm/ 1 μm	M_{n20}	1 μm/ 5 μm

the corresponding MOS transistors in the main amplifier and its bias circuit, and hence, the drain current in OTA transistors are defined by properly selecting the ratio of these current mirrors. In order to reduce the power consumption of the biasing circuit, the current mirror ratio between the corresponding transistors in the main amplifier and its bias circuit is selected to be large which is around 5–20 times in this design. It is worth mentioning that in the utilized bias circuit, the drain current of MOS transistors is constant and it is determined by a constant bias current denoted by I_b in Fig. 5. The size of bias transistors is included in Table 1.

The open-loop gain of the LNA is approximately given by:

$$A_v = g_{ma1}R_{out} = g_{ma1}\left[g_{ma3}r_{dsa3}(r_{dsa2}||r_{dsa1})\right||\left|g_{ma4}r_{dsa4}r_{dsa5}\right] \quad (7)$$

where g_{ma1} is the transconductance of input transistor and r_{ds} is the drain-source resistance of MOS transistors. Table 1 demonstrates the component values used in the simulated amplifier.

2.2.1.1. Input-referred noise analysis. The input-referred noise of the neural amplifier is one of the most important factors in designing AFE since the neural signals have small amplitudes of about several tens of microvolts. As mentioned in the introduction section, due to neuronal activity around recording sites, a background noise is introduced at the input of recording circuits. The value of such a noise increases to 10 μV_{rms}, so the input-referred noise of recording circuits should be smaller than this value [4]. In addition, electrodes also add noise at the input of amplifiers. However, given that the resistance of electrodes varies from several kΩ to several MΩ at different frequencies, the introduced noise by electrodes is not considerable compared to the noise of amplifiers since the electrode impedance is lower than that of the input of the amplifiers. In fact, the noise of the amplifier consists of thermal and

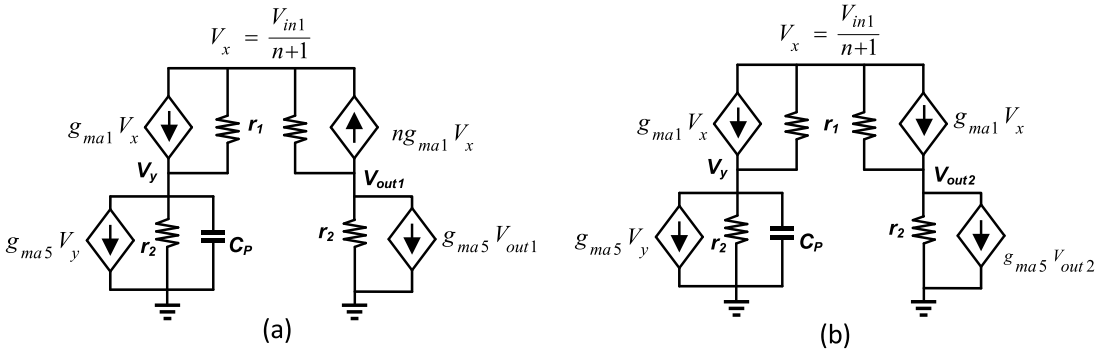

Fig. 6. Small-signal model of channels (a) 1 and (b) 2 when all input signals (except channel 1) are off.

flicker noises generated by transistors. The flicker noise has a high value at lower frequencies, and increasing the size of differential pair input transistors reduces this noise, which depends on the size of transistors. The contribution of these transistors is higher than that of other transistors because the noise source of these transistors is amplified by the amplifier and would then appear at the output. According to Fig. 4, the noise contribution of M_{a3} and M_{a4} cascode transistors is negligible because their noise appears at the output with a small term and then will be divided by the gain of the amplifier. Hence, by neglecting the noise contribution of cascode transistors and considering the effect of both flicker and thermal noise of MOS transistors, the input-referred noise power spectral density (PSD) of the folded-cascode OTA shown in Fig. 4 is given by [24]

$$\overline{V_{n,A1}^2}(f) = \frac{2K_{Fa1}}{C_{OX}W_{a1}f}\left[\frac{1}{L_{a1}} + \left(\frac{K_{Fa2}\mu_n}{K_{Fa1}\mu_p}\right)\left(\frac{I_{Da2}}{I_{Da_1}}\right)\frac{L_{a1}}{L_{a2}^2} + \left(\frac{K_{Fa5}}{K_{Fa1}}\right)\left(\frac{I_{D_{a5}}}{I_{D_{a1}}}\right)\frac{L_{a1}}{L_{a5}^2}\right] + \frac{8kT\gamma}{g_{ma1}}\left(1+\frac{g_{ma2}}{g_{ma1}}+\frac{g_{ma5}}{g_{ma1}}\right) \quad (8)$$

where L is the channel length, W refers to the channel width, K_F is the flicker noise coefficient, C_{ox} refers to the gate oxide capacitance density, μ is the effective mobility, I_D refers to the drain current, and g_m is the transconductance of the MOS transistors. The relation (8) demonstrates that the gm of input differential pair transistors should be larger than that of other transistors, which requires a high amount of power consumption. In this design, the current of the input transistors is 1.8 μA, while the current of the load transistors is 0.2 μA. To decrease the flicker noise, the channel length of other transistors should be larger than that of the input transistors.

2.2.1.2. Transfer function and channel crosstalk analysis. One of the main drawbacks of the partial OTA sharing architecture is the channel crosstalk that should be properly addressed. In fact, the common-source signal of input differential pair transistors is the sum of the attenuated signals of all channels. Consequently, the input signal of one channel can leak to the output of other channels, which can negatively affect the quality of the output signal of other channels. So, the channel crosstalk value should be as low as possible.

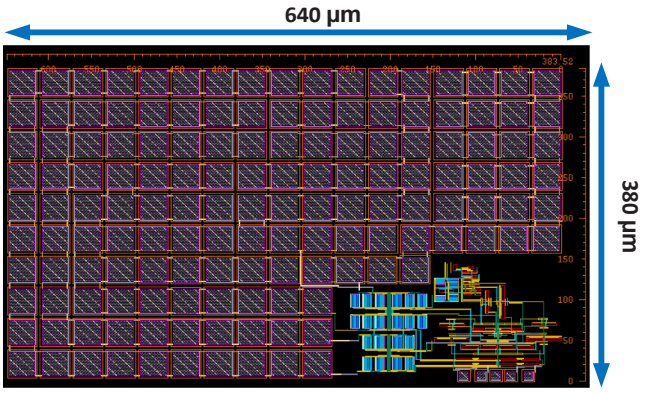

Fig. 7. The layout of the suggested neural amplifier.

To obtain the channel crosstalk, we first need to calculate the transfer function of a channel. Fig. 6(a) shows the small-signal model of one channel (channel 1) when the effect of other channels is not considered, meaning that they are off. Therefore, the V_x voltage is obtained as

$$V_x = \frac{V_{in1}}{n+1} \quad (9)$$

where n is the number of channels. The open-loop transfer function of channel 1 is expressed as

$$T_d(s) = A_v\frac{\left(1-\frac{\omega}{\omega_z}\right)}{\left(1+\frac{\omega}{\omega_{p1}}\right)\times\left(1+\frac{\omega}{\omega_{p2}}\right)} \quad (10)$$

where

$$\omega_z = \frac{2g_{ma5}}{nC_p}, \qquad \omega_{p1} = \frac{1}{C_L R_{out}}, \qquad \omega_{p2} = \frac{1}{\left(n+1\right)C_P\left(\left(n-1\right)r_1 + \frac{1}{g_{ma5}}\right)} \quad (11)$$

The dominant pole is actually located at the output node, and C_P refers to the equivalent capacitance of node y, which is the sum of the parasitic gate capacitance of transistors at V_y. Fig. 6(b) illustrates the small-signal model of channel 2 when the input signal of channel 1 is active. The open-loop transfer function at the output of channel 2 versus the input signal of channel 1 is given by:

$$T_c(s) = \frac{g_{ma1}}{(n+1)g_{ma5}}\times\frac{\left(1-\frac{\omega}{\omega_{zc}}\right)}{\left(1+\frac{\omega}{\omega_{pc1}}\right)\times\left(1+\frac{\omega}{\omega_{pc2}}\right)} \quad (12)$$

where

$$\omega_{zc} = \frac{2g_{ma5}}{nC_p}, \qquad \omega_{pc1} = \frac{1}{C_L R_{out}}, \qquad \omega_{pc2} = \frac{1}{C_P\left(\left(n-1\right)r_1 + \frac{1}{g_{ma5}}\right)} \quad (13)$$

Based on the Eqs. (12) and (13), the crosstalk between these two channels can be obtained as

$$crosstalk_{1-2}(s) = 20\log\left|\frac{T_c(s)}{T_d(s)}\right| = 20\log\left|\frac{1}{(n+1)g_{ma5}.R_{out}}\times\frac{1+\frac{\omega}{\omega_{p2}}}{1+\frac{\omega}{\omega_{pc2}}}\right| \quad (14)$$

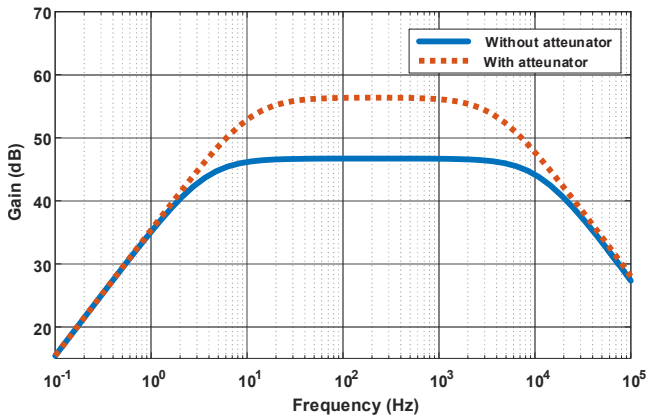

Fig. 8. Frequency response of the suggested amplifier with variable bandwidth and gain.

The relation (14) illustrates that the transconductance of transistor M_{a5} should be large to decrease the channel crosstalk, which can enhance the input-referred noise of the channel according to the relation (8). Thus, there is a compromise between noise and channel crosstalk.

3. Post layout simulation results

The proposed neural amplifier is designed and simulated in Cadence Spectre RF with TSMC 180 nm CMOS technology for multi-channel electrode arrays. The layout of the suggested neural amplifier is illustrated in Fig. 7, which consists of 4 channels as well as related bias circuits with a 640 μm × 380 μm die area. In order to make the overall structure more symmetric, the common-centroid method is utilized by dividing input differential pair transistors into smaller-sized ones. Through current-mirror bias circuits, proper bias currents and voltages are provided for the amplifiers. Metal-insulator-metal (MIM) capacitors are used in the layout for the implementation of capacitors.

Fig. 8 shows the frequency response of one channel with and without the attenuator circuit. According to Fig. 8, the mid-band gain, low cut-off frequency, and high cut-off frequency are 47 dB, 3 Hz, and 10.8 kHz, respectively, without the attenuator. On the other hand, using the attenuator circuit, these parameters are 55 dB, 11 Hz, and 4 kHz, respectively. In addition, Fig. 9 shows the frequency response of the suggested amplifier in process corner cases and power supply voltage changes at 37°C, which illustrates that the structure is well robust over these variations. The temperature variations can be ignored due to the fact that the chip would be implanted inside the brain where the temperature is almost constant. Other simulation results listed in Table 2 provide the characteristics of the proposed neural amplifier in distinct process corner cases and power supply changes. ±10 % changes in supply voltage have been applied, and by reducing the supply voltage, the noise level increases and the bandwidth also decreases. According to Table 2, the achieved performance is almost robust in process corners

Table 2
Performance summary of the proposed amplifier in two recording modes in distinct process corner cases and power supply variations at 37°C.

Without attenuator			
Parameters	FF (V_{DD} = 1.1 V)	SS (V_{DD} = 0.9 V)	TT (V_{DD} = 1 V)
Mid-band gain (dB)	47	46	47
Low cut-off frequency (Hz)	5.4	3.39	1.7
High cut-off frequency (kHz)	9.8	13.8	11.1
Power dissipation (μW)	3.8	1.3	2.4
Total input-referred noise (μV_{rms})	1.73	2.23	2
With attenuator			
Mid-band gain (dB)	55	53.5	55
Low cut-off frequency (Hz)	12.44	4	10
High cut-off frequency (kHz)	3.9	7.6	4.25
Power dissipation (μW)	3.8	1.3	2.4
Total input-referred noise (μV_{rms})	1.34	1.76	1.5

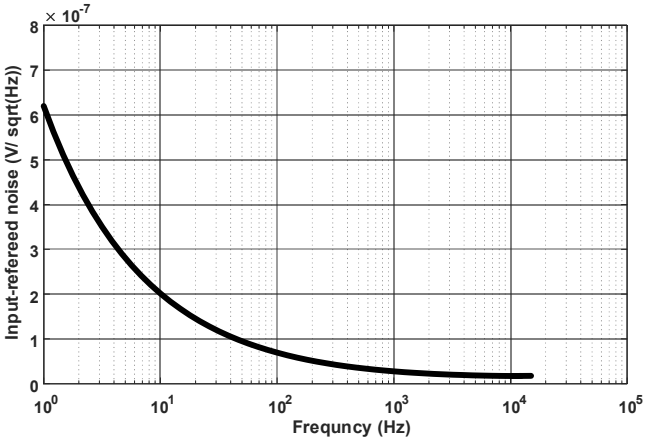

Fig. 10. The simulated input-referred noise of the amplifier.

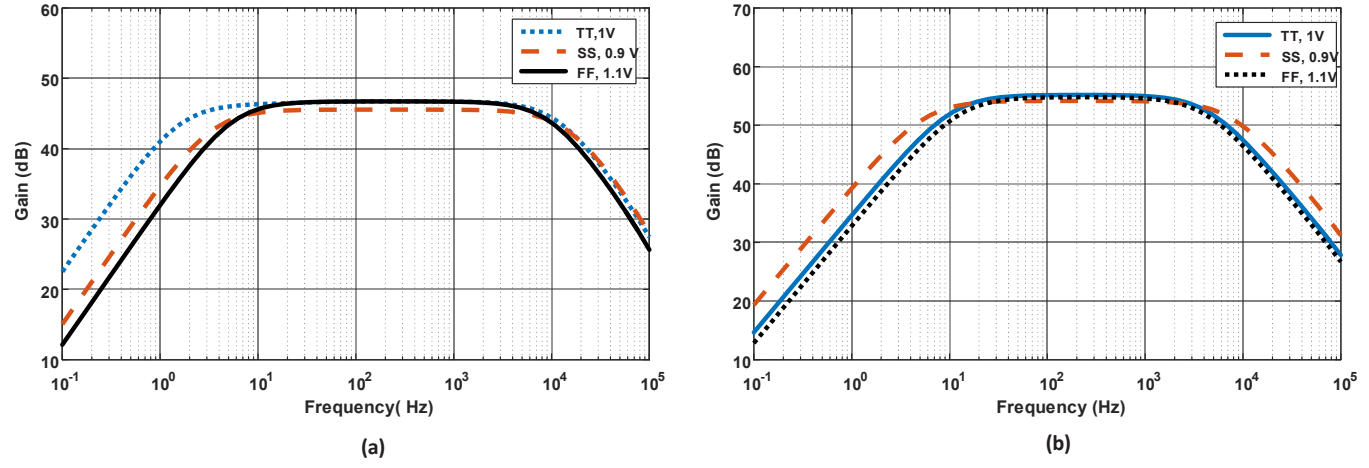

Fig. 9. The frequency response of the suggested amplifier in distinct process corner cases and power supply changes at 37 °C: (a) without the attenuator and (b) with the atteunator.

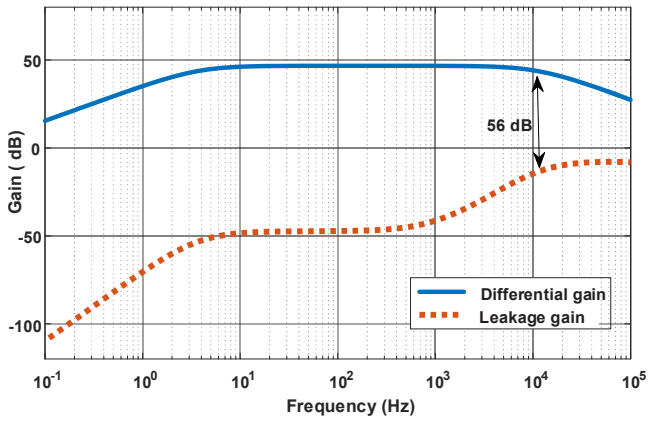

Fig. 11. The crosstalk between channels 1 and 2 versus frequency.

and power supply voltage variations indicating enough supply voltage stability.

Fig. 10 shows the power spectral density (PSD) of the input-referred noise of the proposed neural amplifier. It is 1.9 μV_{rms} over 3 Hz-10.8 kHz frequency range without the attenuator circuit, and with the attenuator, it is 1.45 μV_{rms} over 11 Hz - 4 kHz frequency range. The channel crosstalk between channels 1 and 2 is depicted in Fig. 11 where the input signal of other channels except channel 1 is off. In fact, the crosstalk is the difference between the gain of channel 1 versus input signal and the gain of channel 2 versus the input signal of the channel 1, and its value is 56 dB. As mentioned in the section of Channel Crosstalk Analysis, there is a tradeoff between channel crosstalk and the input-referred noise of the amplifier.

Fig. 12 shows the Monte Carlo simulation results of CMMR and power supply rejection ratio (PSSR) with applying the process variations and device mismatches. According to this figure, the mean value and standard deviation of CMMR are 74.19 dB and 9.88 dB, respectively, at the frequency of 50 Hz for 500 runs. The mean value and standard deviation of PSSR are 70.9 dB and 5.7 dB, respectively.

Two important figure of merits exist to assess the performance of AFE in neural recording amplifiers [18]. Noise efficiency factor (NEF) can provide a proper insight when it comes to compare the noise, bandwidth, and power dissipation of the OTA. Its value is given by

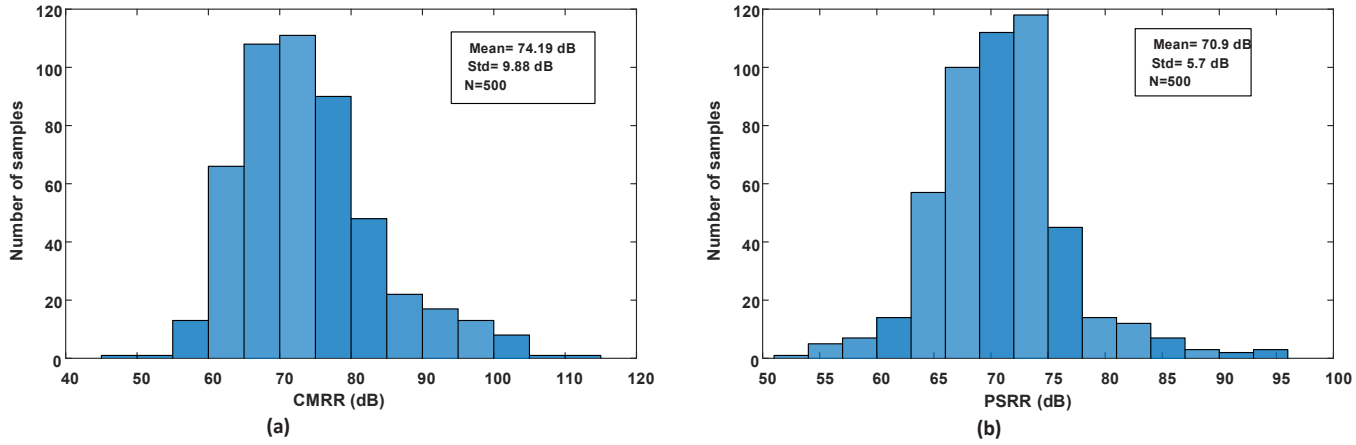

Fig. 12. The results of Monte Carlo simulation for (a) CMRR and (b) PSRR at the frequency of 50 Hz.

Table 3
Performance comparison of the suggested AFE with several state-of-the-art works.

Reference	Process (μm)	V_{DD} (V)	Power dissipation (μw)	Mid-band Gain (dB)	Low-pass $f_{-3\,dB}$ (Hz)	High-pass $f_{-3\,dB}$ (kHz)	THD (dB) (1 mV_{pp} @ 1 kHz)	Input-referred noise (μV_{rms})	NEF	CMRR (dB)	PSRR (dB)	PEF = $(NEF)^2 V_{dd}$
TBCAS'11 [32]	0.18	1.8	7.92	39.4	10	7.2	−40	3.5	3.35	70.1	63.8	20.2
VLSIC'22 [27]	0.13	1.2	4.5	54–60	10	5	-	6.5	7.2	75	-	62.2
AEUE'18 [28]*	0.065	1	1.12	40	0.66	5	-	8.1	4.62	124	88	21.34
SENSORS'23 [10]*	0.028	1	48	26–46	20	2	-	7.6	14.12	105	-	199.3
MEJO'22 [26]*	0.18	1	3.6	45–55	0.8/300	4.15/ 8.2	−46.32	2.1	1.7	98.28	92.48	2.89
TBCAS'15 [31]	0.35	3	12.9	53	10	5	−41.9	7.99	8.9	60	-	237
CSSP'20 [23]*	0.35	3	28.8	34	0.05	8.8	−40	3	3.81	118	119	43.55
JSSC'03 [29]	1.5	±2.5	80	39.5	0.025	7.2	−40[a]	2.2	4	>83	>85	80
TCASI'13 [30]	0.18	1.8	11	48–60	1	9	−38.4	5	4.6	48	55	38.1
AEUE'18 [25]*	0.18	1	0.963	62–74	0.232	0.235	−41.27	1.33	3.34	88	101	9.06
IA'23 [16]	0.18	1.8	1.87	48/59	350	10	-	0.89	1.2	86	83	2.59
MEJO'19 [11]*	0.18	±1.2	7.68	59.7	102	10	-	3.87	2.65	50	53	16.854
This work*	0.18	1	2.4	47/55	3	4/10.8	−42.1	1.9	1.1	74.19	70.9	1.21

* Simulation results

$$NEF = V_{in,rms}\sqrt{\frac{2I_{tot}}{\pi.\ V_T.\ 4kT.\ BW}} \tag{15}$$

where $V_{\mathrm{ni,rms}}$ denotes the input-referred noise, I_{tot} refers to the total current drawn from the supply voltage, V_{T} denotes the thermal voltage, k refers to the Boltzmann's constant, BW refers to the −3 dB bandwidth of amplifier. Through power efficiency factor (PEF), the performance of amplifiers with different supply voltage can be evaluated properly. Its value is expressed as

$$PEF = (NEF)^2 \times V_{DD} \tag{16}$$

The resulted NEF and PEF in this work are 1.1 and 1.21, respectively. Table 3 provides the detailed information related to the specifications of the suggested AFE in comparison with other state-of-the-art works, where some simulation-based results are also included for a fair comparison. Simulation results have been obtained at the TT process corner case and 27°C a 1-V supply voltage. The suggested amplifier has one of the best NEF and PEF compared to other references. The bandwidth of the system can be increased, but this comes at the expense of increased power consumption and input-referred noise. Therefore, the bandwidth of the system is tuned to around 10 kHz, which is suitable for amplification of neural signals with a higher frequency range like APs. As mentioned earlier in the conventional structure, the maximum frequency of a neural signal, belonging to AP signals, is about 10 kHz. The amplifier presented in [16] has a proper input-referred noise, NEF, and PEF, but the low cut-off frequency of this structure is large, which is more than 300 Hz, and hence, it is not appropriate for amplification of neural signals with low frequency contents like LFPs. In [11], an OTA sharing structure is utilized in an active integration structure to prevent using large DC blocking capacitors at the input of the amplifier. However, this structure has a feedback amplifier, requiring more power consumption and also has large input-referred noise. In [26], a novel structure is used for increasing the linearity and the resistance value of pseudo resistors. But the overall structure has three stages that increase not only the complexity of the system in terms of implementation but also power consumption.

4. Conclusion

In this paper, a neural amplifier with partial OTA sharing structure is designed for implantable neural recording applications. The OTA sharing architecture can decrease the power dissipation and die area given that each amplifier shares the passive part related to the reference electrode. The gain and bandwidth of each channel is changed by an attenuator circuit used in the feedback path in series with the feedback capacitor. This is proper for neural signals that have different amplitudes and frequencies, particularly for neural signals with low amplitudes that need a higher gain to be amplified. Important parameters related to designing a neural amplifier have been considered such as total input-referred noise, power dissipation, bandwidth, and linearity. The analysis on noise and channel crosstalk is done to make the system more efficient. The mid-band gain and bandwidth of each amplifier are 47 dB and 10.8 kHz, respectively. By using the attenuator circuit, the gain is increased to 55 dB, and the bandwidth is decreased to 4 kHz. The input-referred noise is 1.9 μVrms over 3 Hz−10.8 kHz frequency range, and it is 1.45 μVrms over 11 Hz−4 kHz frequency range. The total power consumption is 2.4 μW from a single 1-V supply voltage. The obtained NEF and PEF are 1.1 and 1.21, respectively. The 4-channel neural amplifier is designed and simulated in 180 nm TSMC CMOS technology. The neural amplifier has a mid-band gain of 47 dB and bandwidth from 3 Hz to 10.8 kHz without using attenuator circuit, and by using the attenuator, the mid-band gain increases to 55 dB and the bandwidth decreases to 4 kHz. The power dissipation of each channel is 2.4 μW from 1-V supply voltage. The input-referred noise is 1.9 μVrms over 3 Hz-10.8 kHz frequency range, and it is 1.45 μVrms over 11 Hz-4 kHz frequency range when the attenuator is active in the feedback path.

CRediT authorship contribution statement

Mehdi Ashayeri: Conceptualization, Formal analysis, Methodology, Visualization, Writing – original draft. **Mohammad Yavari:** Investigation, Project administration, Supervision, Validation, Writing – review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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