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An IIP3 enhancement technique for CMOS active mixers with a source-degenerated transconductance stage

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ABSTRACT

In this paper, a new third-order input intercept point (IIP3) enhancement technique is introduced for CMOS active mixers with a source-degenerated transconductance stage. In the proposed technique, the third-order Volterra kernel of the output current of the transconductance stage is significantly attenuated by producing a new interaction term which is in an equal magnitude but an opposite phase related to the stage's total third-order intermodulation (IM3) current. For this end, a second-order intermodulation (IM2) current with an adjustable magnitude and phase is produced and injected to the transconductance stage. The proposed mixer has been designed for IEEE 802.11 applications with input frequency and output bandwidth equal to 2.4 GHz and 20 MHz, respectively, and simulated using a 90 nm RF-CMOS technology. Spectre-RF simulation results reveals that the IIP3 improves about 17.5 dB and 18.2 dB compared to the conventional mixers with source-degenerated and fully-differential transconductance stages, respectively, while only 1.2 mA extra current is drawn from a single 1.2 V power supply. In addition, the proposed technique has no effect on other parameters of the mixer such as the noise figure and conversion gain.

1. Introduction

In modern CMOS technologies, the power supply voltage is reduced by the process scaling. CMOS technology scaling improves the noise performance of the radio frequency (RF) circuits by the scaling of R_n [1,2] resulting in the decreased minimum noise figure (NF_{min}) according to the relation given in [3]. This also increases the cut-off frequency (f_T) of MOS transistors. Nonetheless, the linearity performance and intrinsic dc gain in MOS transistors are degraded by technology scaling. So, using some linearization techniques to realize highly linear RF receivers are needed. On the other hand, in a receiver chain, the linearity of the whole system is usually limited by the linearity of the down-conversion mixer [4]. The output nonlinear current of the transconductance stage is the most dominant source of distortion in CMOS low-noise amplifiers (LNAs) and active mixers. The IM2 and IM3 are the most important parts of the nonlinear current limiting the second-order input intercept point (IIP2) and IIP3, respectively. These two parts mainly originate from the first- and second-order derivatives of the transistor transconductance (g'_m and g''_m), respectively.

Several approaches have been introduced to cancel the IM3 current of the transconductance stage [2,5–10]. In [2,5,7,8], an auxiliary transistor is employed in parallel with the main transistor and it works in the triode or weak inversion region. The g''_m of the auxiliary transistor is in an equal magnitude but an opposite phase related to the main transistor resulting in the cancellation of the stage's total IM3 current. The post-distortion technique to cancel the IM3 current of the input transistor is realized by using a diode-connected nMOS transistor at the output in [6]. In [10], a nonlinear circuit with an adjustable second-order Volterra kernel in magnitude and phase is employed prior of the conventional mixer. The third-order Volterra kernel of the conventional mixer is canceled by tuning the magnitude and phase of the added nonlinear circuit.

However in [2,5,8], the IIP3 improvement is limited due to the interaction between the input signal and the second-order distortion at the output of the transconductance stage. This problem is alleviated in [8,9] by employing an LC filter to attenuate the output second-order nonlinearity. Nevertheless, in [2,7–9], the g''_m of the main transistor is canceled in a narrow bias point range by the auxiliary transistor [11]. Also, the proposed method in [6] decreases the gain of the stage. Moreover, all of these techniques increase the noise figure of the circuit.

In this paper, a new IIP3 improvement technique by canceling the output IM3 current of the transconductance stage is proposed without affecting the other parameters of the mixer such as the

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conversion-gain and noise figure. The paper organized as follows. The proposed IIP3 enhancement technique is introduced in Section 2. Section 3 presents the Spectre-RF simulation results using a 90 nm RF-CMOS technology. Finally, the conclusions are given in Section 4.

2. Proposed IIP3 enhancement technique

There are several conventional topologies to realize the transconductance stage in RF circuits such as the pseudo-differential, fully-differential, and source-degenerated schemes. The pseudo-differential topology, shown in Fig. 1(a), in comparison with the other schemes, owing to having lower number of the stacked transistors between the power rails, is a good solution to realize the transconductance stage in low voltage applications. Moreover, this topology provides a high IIP3 [12]. However, the pseudo-differential approach suffers from the large amount of common-mode second-order distortion leading to a lower IIP2.

On the other hand, in the fully-differential topology which is shown in Fig. 1(b), the tail current source provides a high impedance node at the source of the input transistors. This makes the common-mode second-order nonlinearity current of the input transistors to be significantly attenuated. But, an interaction term in the third-order kernel of the transconductance stage output current is produced. This term is originated from the interaction between the input signal and the second-order nonlinear component at the source node of the input transistors. This interaction term increases the IM3 current of the stage making its IIP3 performance to be degraded in comparison with the pseudo-differential and source-degenerated transconductance stages [13].

The source-degenerated transconductance stage shown in Fig. 1(c) is one of the ways to provide both high IIP2 and IIP3 [13,14]. But, the interaction term still exists in the IM3 current of this type of transconductor and the IIP3 of the mixer is limited in comparison with the pseudo-differential transconductor.

Fig. 2 shows the first proposed transconductance stage where M_1–M_2 with M_{deg} and C_{deg}, M_{1a}–M_{2a} transistors along with R_D, L_D, C_D (RLC network) and C_C (ac coupling capacitor) form the source-degenerated transconductance and the proposed IM3 cancellation circuit, respectively. In the conventional source-degenerated transconductor, M_{deg} transistors degenerate the input transistors (M_1 and M_2) making low gain at the IM2 frequency. Also at the IM3 current frequency, the capacitors $C_{\rm deg}$ ground M_{deg} transistors, and hence, the IM3 current is reduced resulting in an increment in the value of IIP3 [13].

In this circuit, the transistors M_{1a} and M_{2a} are similar and they are used to convert the input signal voltage to a nonlinear current.

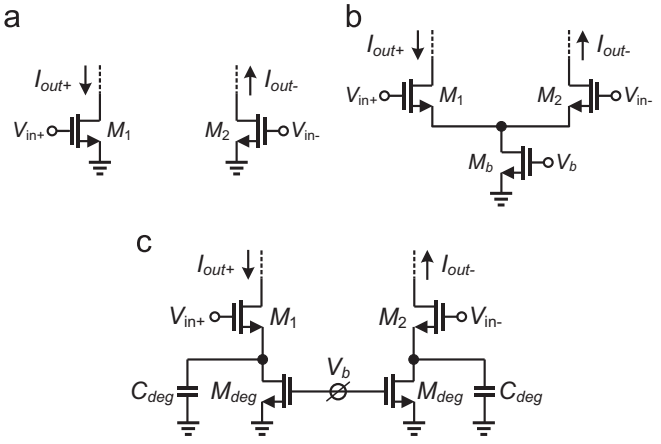

Fig. 1. Transconductance stages: (a) pseudo-differential; (b) fully-differential; and (c) source-degenerated.

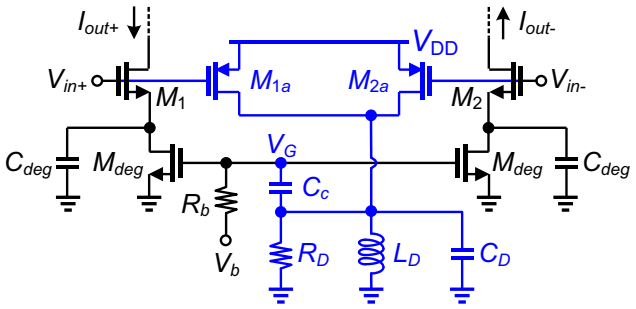

Fig. 2. The first proposed transconductance stage.

Since the drain of these two transistors are connected together, the differential components (odd-order terms) of their currents are removed and the common-mode components (even-order terms) are summed up in the output current ($I_{\rm IM2}$). This current then appears at the source of M_1 and M_2 as a voltage while flowing from the RLC network and being amplified by M_{deg} transistors. Here, only the second-order Volterra kernel of this voltage is considered and higher order kernels are neglected. Finally, due to the nonlinear I–V characteristic of an MOS transistor, this voltage (IM2 voltage) is multiplied with the input signal and produces a new interaction term in the IM3 current of M_1 and M_2. It will be proved that the total IM3 current of the transconductance stage can be reduced by changing the values of RLC network components.

The small-signal drain current of transistors M_1, M_2, M_{1a}, M_{2a} and M_{deg} can be expressed by Taylor series expansion as

$$i_{d1} = i_{out+} = g_{m1}(v_{in+} - v_{s1}) + g'_{m1}(v_{in+} - v_{s1})^2 + g''_{m1}(v_{in+} - v_{s1})^3 + \ldots \quad (1)$$

$$i_{d2} = -i_{out-} = g_{m2}(v_{in-} - v_{s2}) + g'_{m2}(v_{in-} - v_{s2})^2 + g''_{m2}(v_{in-} - v_{s2})^3 + \ldots \quad (2)$$

$$i_{d1a} = g_{m1a}v_{in+} + g'_{m1a}{v_{in+}}^2 + g''_{m1a}{v_{in+}}^3 + \ldots \quad (3)$$

$$i_{d2a} = g_{m2a}v_{in-} + g'_{m2a}{v_{in-}}^2 + g''_{m2a}{v_{in-}}^3 + \ldots = -g_{m1a}v_{in+} + g'_{m1a}{v_{in+}}^2 - g''_{m1a}{v_{in+}}^3 + \ldots \quad (4)$$

The gate voltage of the M_{deg} transistors, the drain current (I_{out+}) and the source voltage (V_S) of M_1 can be defined as

$$V_G = D_2(\pm\omega_1, \mp\omega_2)\circ V_{in+}^2 + \ldots \quad (5)$$

$$I_{out+} = H_1(\omega)\circ V_{in+} + H_2(\omega_1,\omega_2)\circ V_{in+}^2 + H_3(\omega_1,\omega_2,\omega_3)\circ V_{in+}^3 + \ldots \quad (6)$$

$$V_{S1} = A_1(\omega)\circ V_{in+} + A_2(\omega_1,\omega_2)\circ V_{in+}^2 + A_3(\omega_1,\omega_2,\omega_3)\circ V_{in+}^3 + \ldots \quad (7)$$

where D_2 and H_1, H_2, H_3 and A_1, A_2, A_3 are the second-order kernel of V_G, first-, second- and third-order kernels of I_{out+} and V_S, respectively.

By writing the KCL at the drain of M_{1a} and M_{2a} we have

$$\frac{1}{L_D}\int_0^t v_G(t)dt + C_D\frac{dv_G(t)}{dt} + \frac{v_G(t)}{R_D} - i_{d1a} - i_{d2a} = 0 \quad (8)$$

By using the relations (3) and (4) for a pMOS transistor, the relation (5) and the frequency domain representation of (8), the second-order kernel of V_G is obtained as

$$D_2(\pm\omega_1, \mp\omega_2) = \frac{(\pm j\omega_1 \mp j\omega_2)R_D L_D \times 2(1/2!)g'_{m1a}}{R_D + (\pm j\omega_1 \mp j\omega_2)L_D - (\pm\omega_1 \mp\omega_2)^2 R_D L_D C_D} \quad (9)$$

On the other hand, by writing the KCL at the source of M_1 we have

$$i_{d,deg}+\frac{v_S}{r_{ds,deg}}+C_{deg}\frac{dv_S}{dt}-i_{out+}=0 \tag{10}$$

The second-order kernel of V_S and the first- and third-order kernels of I_{out+} are calculated by using (9) and substituting (1), (2), (6) and (7) into the frequency domain representation of (10) and assuming that $(\omega_{1,2}r_{ds,deg}C_{deg})$, $(|2\omega_1-\omega_2|r_{ds,deg}C_{deg}) \gg 1+g_{m1}r_{ds,deg}$ as follows:

$$A_2(\pm\omega_1,\mp\omega_2)=\frac{r_{ds,deg}\left[g'_{m1}-g_{m,deg}D_2(\pm\omega_1,\mp\omega_2)\right]}{1+g_{m1}r_{ds,deg}+(\pm j\omega_1\mp j\omega_2)r_{ds,deg}C_{deg}} \tag{11}$$

$$H_1(\omega)=\frac{g_{m1}(1+j\omega r_{ds,deg}C_{deg})}{1+g_{m1}r_{ds,deg}+j\omega r_{ds,deg}C_{deg}}\approx g_{m1} \tag{12}$$

$$\begin{aligned}H_3(\pm\omega_1,\pm\omega_1,\mp\omega_2)&\approx g''_{m1}-\frac{2}{3}g'_{m1}(2A_2(\pm\omega_1,\mp\omega_2)\\&\quad+A_2(\pm\omega_1,\pm\omega_1))\\&=g''_{m1}-\frac{2}{3}g'^2_{m1}r_{ds,deg}\left(\frac{2}{1+g_{m1}r_{ds,deg}+(\pm j\omega_1\mp j\omega_2)r_{ds,deg}C_{deg}}\right.\\&\quad\left.+\frac{1}{1+g_{m1}r_{ds,deg}\pm 2j\omega_1 r_{ds,deg}C_{deg}}\right)\\&\quad+\frac{2}{3}g_{m,deg}g'_{m1}r_{ds,deg}\left(\frac{2D_2(\pm\omega_1,\mp\omega_2)}{1+g_{m1}r_{ds,deg}+(\pm j\omega_1\mp j\omega_2)r_{ds,deg}C_{deg}}\right.\\&\quad\left.+\frac{D_2(\pm\omega_1,\pm\omega_1)}{1+g_{m1}r_{ds,deg}\pm 2j\omega_1 r_{ds,deg}C_{deg}}\right)\end{aligned} \tag{13}$$

In the second-order kernel of V_S given in (11), the first term in the numerator bracket is the intrinsic second-order nonlinearity of the input transistor (M_1) and the second term originates from the proposed IM2 generator circuit (M_{1a}, M_{2a} and RLC network). As it is seen from (12), the total transconductance of the stage is approximately equal to the transconductance of the input transistors due to the frequency pole generated by C_{deg} and $r_{ds,deg}$ at the operating frequency. In relation (13), the first term is the intrinsic third-order transconductance nonlinearity of M_1 and M_2 input transistors and the second term is the interaction term of the conventional source-degenerated transconductor as well as the third term is the added interaction term by the proposed technique.

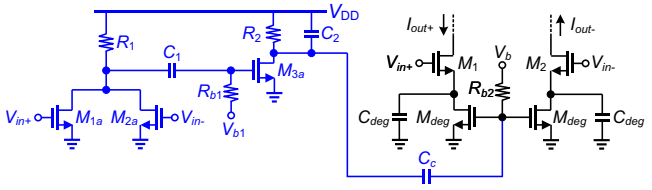

Fig. 3. The second proposed transconductance stage.

As it is seen from (9) and (11), the magnitude and phase of the added interaction term in (13) can be changed by the values of R_D, L_D and C_D, and hence, the third-order kernel of I_{out+} could be attenuated accordingly resulting in an enhancement in the value of IIP3 as

$$A_{IIP3}=\sqrt{\frac{4}{3}\frac{H_1(\omega)}{H_3(\pm\omega_1,\pm\omega_1,\mp\omega_2)}} \tag{14}$$

Eqs. (11) and (13) state that H_3 can be canceled resulting in an infinite A_{IIP3} provided that the following condition is satisfied:

$$2A_2(\pm\omega_1,\mp\omega_2)+A_2(\pm\omega_1,\pm\omega_1)=\frac{3}{2}\frac{g''_{m1}}{g'_{m1}} \tag{15}$$

The circuit shown in Fig. 2 is the simplest way to realize the proposed idea. However, it has a drawback which affects the performance of the mixer at SF, FS, TF, FT, TS and ST process corner cases. In this circuit, because the nonlinearities of the input nMOS transistors have been compensated by using pMOS transistors, at SF, FS, TF, FT, TS and ST corner cases, where pMOS and nMOS are fast and slow and vice versa, the obtained relation in (15) cannot be satisfied properly resulting in the degraded IIP3. To solve this problem, the added circuit is realized by using only nMOS transistors and also the inductor is removed. The second proposed transconductance is shown in Fig. 3. Moreover, in this circuit the L_d inductor has been removed and an extra capacitor (C_2) is added to better tune the injected IM2 signal to the gate of M_{deg} transistors. It can be shown that for this circuit, the equated relation in (9) is changed as

$$\begin{aligned}D_2(\pm\omega_1,\mp\omega_2)&=2g_{m3a}2g'_{m1a}\\&\times\left(\frac{(\pm j\omega_1\mp j\omega_2)(R_2||R_{b2})R_{b1}R_1C_1}{[1+(\pm j\omega_1\mp j\omega_2)C_1(R_{b1}+R_1)](1+(\pm j\omega_1\mp j\omega_2)C_2(R_2||R_{b2}))}\right)\end{aligned} \tag{16}$$

As it is seen from (16), although changing the value of R_2, R_{b2} and C_2 can change the magnitude and phase of D_2 resulting in an improved IIP3, however these components should form a low-pass filter to attenuate the out-of-band nonlinearities generated by M_{1a} and M_{2a} which fall in the IF band (20 MHz). So, and their values are determined by the low-pass filter characteristics.

Since the value of all bias resistances are fixed in this design, only R_1 and C_1 can be used to change the magnitude and phase of D_2. So, according to (15), the third-order kernel of the transconductance stage output current in (13) can be canceled.

Due to the increased number of transistors at the RF port of the proposed mixer, the parasitic capacitance seen from the RF port is also increased. In addition, the proposed IMD cancellation technique is based on a perfect phase opposition of the original and

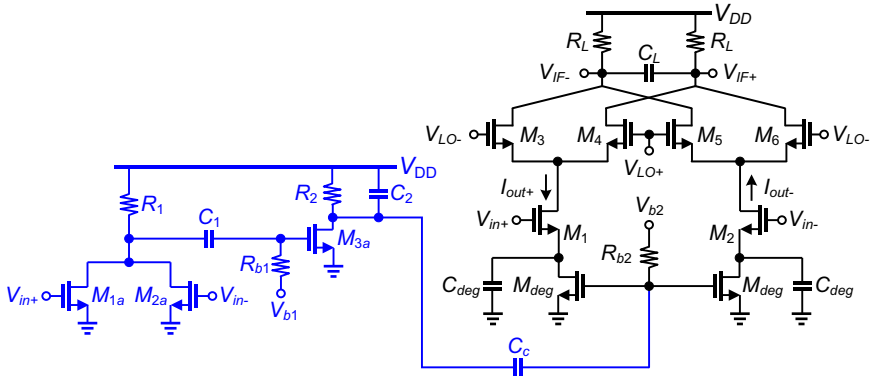

Fig. 4. Proposed CMOS active mixer.

the compensating IMD product. As a result, by considering the relations (9), (11), (15) and (16), this technique is frequency dependent and this will be satisfied for a narrow bandwidth of input signal. So, this technique is not appropriate for ultra-wide band (UWB) applications. In addition, in the proposed mixer, since several large capacitors (C_1, C_2 and C_c) are added, the occupied silicon area is increased due to the added circuit and the total power consumption is increased as well in comparison with the conventional mixer. Also, in the proposed technique, there is a tradeoff between the power consumption and silicon die area. In order to decrease the power consumption, the current of M_{1a-3a} transistors should be decreased which results in a lower magnitude of D_2. To compensate the magnitude reduction of D_2, the value of resistors R_{1-2} and R_{b1-b2} should be increased. On the other hand, increasing the resistors (R_{1-2} and R_{b1-b2}), changes the phase of the injected IM2 signal to the gate of M_{deg} transistors. To compensate this phase variation, the value of the capacitors (C_1, C_2 and C_c) should be increased which results in larger die area.

As it is seen from Fig. 3, the device noise of added circuit appears at the right and left sides similarly, and hence, their noise produce a common-mode term at the output of the mixer. So, the added circuit in Fig. 3 does not increase the noise of the differential output, and hence, the noise figure of the proposed mixer is not affected compared to the conventional source-degenerated mixer. Besides, since the fundamental current of

Table 1
Device parameters used in the simulation of the mixers.

Parameter	Proposed mixer	Source-degenerated mixer	Fully-differential mixer
$(W/L)_{1,2}$	90 × 0.5 μm/0.08 μm	90 × 0.5 μm/0.08 μm	90 × 0.5 μm/0.08 μm
$(W/L)_{3-6}$	124 × 0.5 μm/0.08 μm	124 × 0.5 μm/0.08 μm	124 × 0.5 μm/0.08 μm
$(W/L)_{deg}$	90 × 0.5 μm/0.08 μm	90 × 0.5 μm/0.08 μm	–
$(W/L)_b$	–	–	180 × 0.5 μm/0.08 μm
$(W/L)_{1a,2a}$	4 μm/0.1 μm	–	–
$(W/L)_{3a}$	8 μm/0.1 μm	–	–
R_L	560 Ω	560 Ω	560 Ω
R_1	5 kΩ	–	–
R_2	4.7 kΩ	–	–
$R_{b1,\ b2}$	10 kΩ	–	–
C_1	2 pF	–	–
C_2	1.5 pF	–	–
C_{deg}	5 pF	5 pF	–
C_L	17.8 pF	17.8 pF	17.8 pF

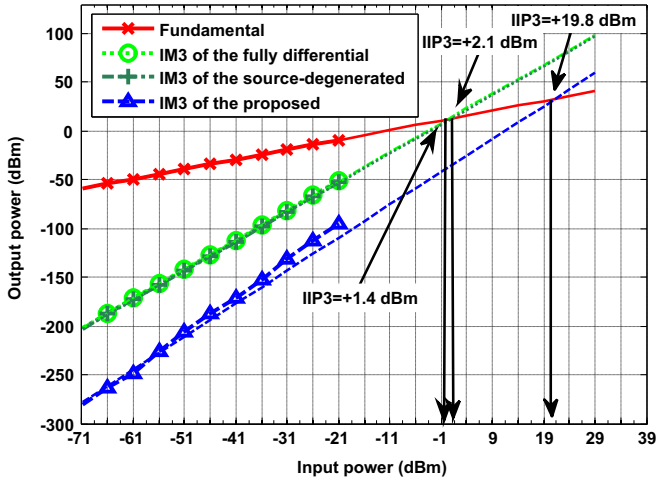

Fig. 5. Simulated IIP3 of the proposed, source-degenerated, and fully-differential CMOS active mixers.

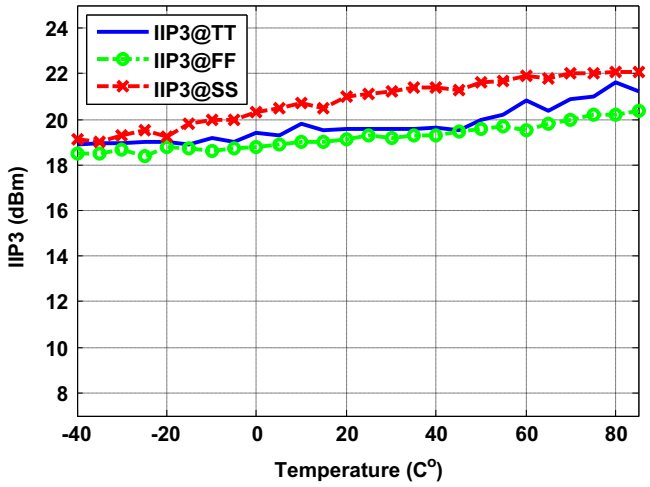

Fig. 6. Simulated IIP3 at different process corner cases versus the temperature.

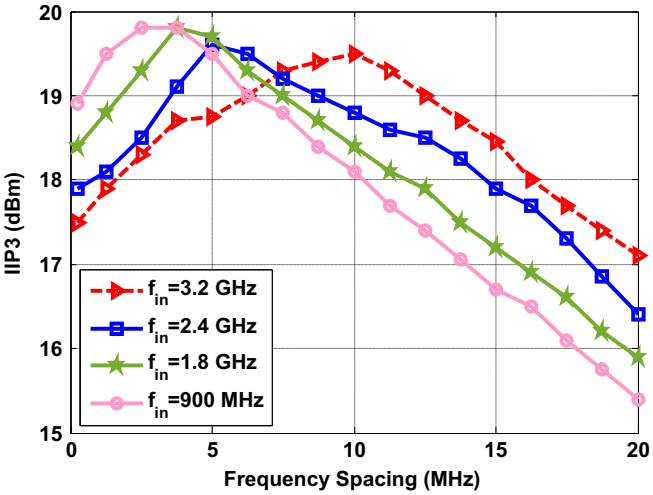

Fig. 7. Simulated IIP3 of the proposed mixer versus the two-tone frequency spacing.

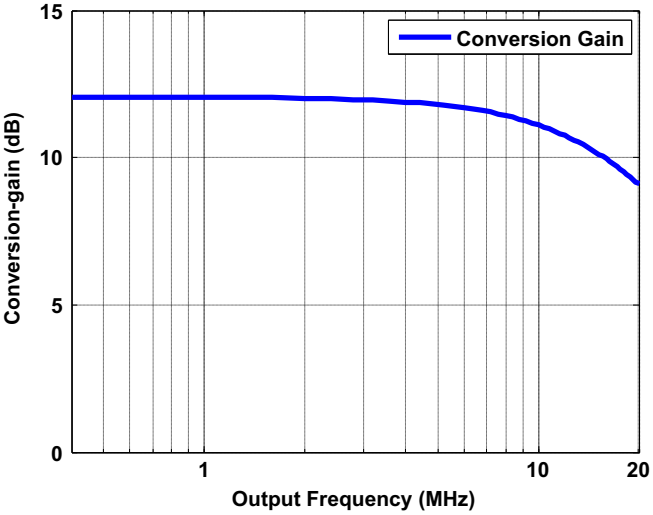

Fig. 8. Simulated voltage conversion-gain of the proposed mixer.

M_{1a} and M_{2a} transistors cancels each other, the conversion-gain of the proposed mixer is the same as the conventional source-degenerated mixer.

3. Simulation results

The proposed mixer shown in Fig. 4 has been simulated using a 90 nm CMOS process with Spectre-RF along with the conventional fully-differential and source-degenerated active mixers. It has been designed for IEEE 802.11 applications with input frequency and output bandwidth equal to 2.4 GHz and 20 MHz, respectively. The switching stage is driven by a local oscillator with +3 dBm power. The device parameters used in the simulation of the mixers are summarized in Table 1. To calculate the IIP3, a two-tone test with 5 MHz spacing is employed.

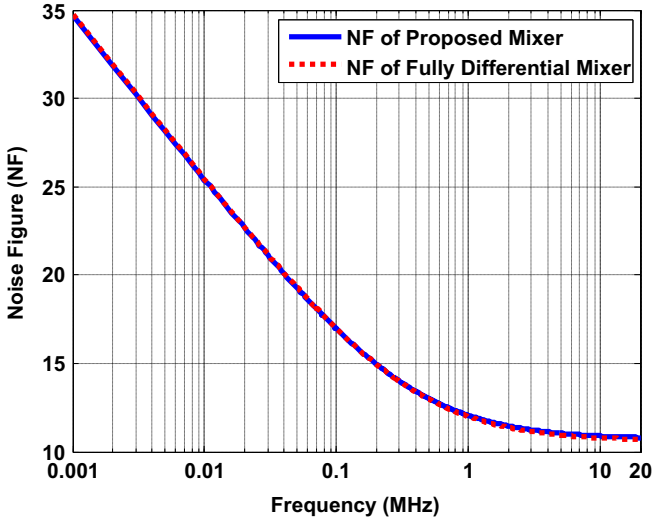

Fig. 9. Simulated noise figure.

Table 2
Simulation results of the proposed mixer in different process corner cases and temperature variations.

Parameter	FF @ −40 °C	TT @ 27 °C	SS @ 85 °C
IIP3 (dB m)	+18.5	+19.6	+22.1
Conversion gain (dB)	13.2	12	10.9
Average in-band NF (dB)	10.8	11.4	12
Power (mW)	4.7	4.4	4
Power supply voltage	1.2 V		
Process	90 nm CMOS		

The IIP3 simulation results of the proposed and conventional mixers are illustrated in Fig. 5. The proposed mixer has an IIP3 of +19.6 dBm which is improved by approximately 17.5 dB and 18.2 dB in comparison with the conventional source-degenerated and fully-differential mixers, respectively. Moreover, to evaluate the robustness of the proposed technique, the simulated IIP3 at different process corner cases versus the temperature is shown in Fig. 6. As it is shown, the variation of the IIP3 is small indicating the usefulness of the proposed technique. In order to investigate the performance of the proposed IM3 cancellation technique, IIP3 has been simulated versus the two-tone frequency spacing and the results are shown in Fig. 7. As it is seen, IIP3 of the proposed mixer varies versus the frequency spacing indicating that the proposed IM3 cancellation scheme depends on the frequency.

To provide a fair comparison in IIP3, the same conversion-gain is considered in the proposed and two conventional mixers. The simulated conversion-gain of the proposed mixer in the output bandwidth is shown in Fig. 8. As it is seen, the value of the conversion-gain is approximately equal to 12 dB which has not been changed in comparison with the fully-differential and source-degenerated mixers.

The simulated noise figure of the proposed and conventional fully-differential mixers is shown in Fig. 9. The noise figure of the proposed mixer is increased about 0.1 dB compared to the fully-differential mixer due to the noise of M_{deg} transistors. The simulation results in different process corner cases and temperature variations are summarized in Table 2. This table shows that the parameters of the mixer have small variations in the corner cases, and consequently, the proposed technique is almost robust. Table 3 summarizes the simulation results and compares the proposed mixer with several reported works [15–19] using the following figure-of-merit (FoM) [20]:

$$\mathrm{FoM} = 10\log\left(\frac{10^{\frac{\mathrm{CG(dB)}}{20}} \times 10^{\frac{\mathrm{IP3(dBm)}-10}{20}}}{10^{\frac{\mathrm{NF(dB)}}{10}} \times P(\mathrm{mW}) \times V_{DD}(\mathrm{V})}\right) \tag{17}$$

As it is seen, the proposed mixer achieves a high IIP3 and results in an outstanding FoM indicating the effectiveness of the proposed IIP3 enhancement technique.

4. Conclusions

In this paper, a new technique based on the IM2 injection technique is proposed to enhance the value of IIP3 in CMOS active mixers by producing a new interaction term with an adjustable magnitude and phase in the IM3 current of the transconductance stage. The magnitude and phase of the produced interaction term are tuned by changing only the value of several resistors and capacitors. It is realized in a source-degenerated transconductance stage and results in the attenuation of the total output IM3 current. The proposed

Table 3
Simulation results summary.

Parameter	Proposed mixer	Source-degenerated mixer	Fully-differential mixer	[15]	[16]	[17]	[18][a]	[19]
Frequency (GHz)	2.4	2.4	2.4	2.1	3.1–4.8	2.4	0.9	2.1
IIP3 (dB m)	+19.6	+2.1	+1.4	6	+24	−16.1	+11.8	+15
Conversion-gain (dB)	12	12	12	12	12	9	17.6	15
NF (dB)	11.4	11.4	11.3	17.5	13	6.37	10.1[b]	14
Power supply (V)	1.2	1.2	1.2	1	1.2	1	1.8	1.8
Power (mW)	4.64	3.2	3.2	6	3	2.97	19.62	8
Process (nm)	90	90	90	65	130	90	160	180
FoM	−8	−15.2	−15.4	−21.28	−5.56	−19.74	−15.9	−15.6

[a] Measurement results.
[b] Average of IIP3 in input bandwidth.

technique can also be utilized in CMOS low noise amplifiers with a source-degenerated transconductance stage.

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