Using interaction between two nonlinear systems to improve IIP3 in active mixers

M. Asghari and M. Yavari

A new linearisation technique for active mixers is introduced to enhance the third-order input intercept point (IIP3). This technique is based on the cancellation of the third-order Volterra kernel in the output current of the transconductance stage by using the interaction between two nonlinear systems. In this scheme, a nonlinear circuit is employed prior to the conventional mixer to improve the total IIP3 by adjusting its second-order Volterra kernel magnitude and phase. Moreover, the added circuit increases the conversion gain of the mixer. The simulation results show that both the IIP3 and the conversion gain simultaneously improve by 13 and 11.4 dB, respectively, compared with the conventional active mixer.

Introduction: Linearity and noise figure are the most important parameters in the design of radio frequency (RF) receivers. Recently, the CMOS technology scaling has led to a better noise figure, but with degraded linearity performance and intrinsic DC gain in the MOS transistors [1]. Moreover, since the technology scaling decreases the power supply voltage, the voltage headroom in the load stage is reduced, resulting in the decreased maximum gain of the designed circuit. Mixers are one of the important blocks in the RF receivers due to their frequency translation capability. The linearity of the mixers has a considerable influence on the total linearity of an RF receiver. It is usually characterised with second-order input intercept point (IIP2) and IIP3 parameters among which the IIP3 has a great significance in the design of the CMOS RF receivers. Several techniques have been introduced to enhance the IIP3 [1-3]. An auxiliary transistor, to form a multiple gated transistor, is employed in [1, 2] to cancel the third derivative of the main transistor's drain current in the transconductance stage. In [3], the third-order distortion of the transconductance stage has been cancelled by using the second-harmonic injection technique. However, due to an interaction term caused by the feedback, the IIP3 improvement is limited in [1, 2] and also the method in [3] is not applicable in low-voltage designs because of needing an extra headroom voltage in its tail transistor. In this Letter, a new IIP3 improvement technique based on the interaction between two nonlinear is presented which also improves the conversion gain significantly.

Proposed IIP3 enhancement technique: The general block diagram of the proposed linearisation technique is shown in Fig. 1 where two non-linear subsystems named A and B are utilised. The Volterra kernels of the total system output current ($I_{out,B}$) can be defined as follows:

$$I_{\text{out, }B} = H_1(s_1) V_{\text{in}} + H_2(s_1, s_2) V_{\text{in}}^2 + H_3(s_1, s_2, s_3) V_{\text{in}}^3 + \cdots$$
(1)

where H_1 , H_2 and H_3 are the first-, second- and third-order Volterra kernels of the system, respectively. The first- and the third-order kernels of the cascaded system can be obtained according to the kernels of the subsystems *A* and *B* as [4]

$$H_1(s_1) = A_1(s_1)B_1(s_1)$$
(2)

$$H_{3}(s_{1}, s_{2}, s_{3}) = B_{3}(s_{1}, s_{2}, s_{3})A_{1}(s_{1})A_{1}(s_{2})A_{1}(s_{3}) + B_{1}(s_{1} + s_{2} + s_{3})A_{3}(s_{1}, s_{2}, s_{3}) + \frac{2}{3} \Big[B_{2}(s_{1}, s_{2} + s_{3})A_{1}(s_{1})A_{2}(s_{2}, s_{3}) + B_{2}(s_{2}, s_{1} + s_{3})A_{1}(s_{2})A_{2}(s_{1}, s_{3}) + B_{2}(s_{3}, s_{1} + s_{2})A_{1}(s_{3})A_{2}(s_{1}, s_{2}) \Big]$$
(3)

where A_1 , A_2 , A_3 and B_1 , B_2 , B_3 are the kernels of the subsystems A and B, respectively. Since the first-order kernel of a system is the same as its transfer function (TF), H_1 is obtained from the system TF. As is seen, if $|A_1| > 1$, the gain of the system will be increased. In (3), the first and the second terms of H_3 originate from the third-order nonlinearities of the subsystems A and B and the terms in the brackets originate from the interaction between the two nonlinear subsystems. Assuming A_1 , $B_3 < 0$ and A_3 , $B_1 > 0$, if $B_2A_2 < 0$ the third-order kernel in (3) could be

cancelled, resulting in an improvement in the total system $A_{\rm IIP3}$ according to

$$A_{\rm IIP3} = \sqrt{\frac{4}{3} \frac{H_1(s_1)}{H_3(s_1, s_2, s_3)}} \tag{4}$$

Fig. 1 Block diagram (system level) of proposed technique

In practice, producing the second-order nonlinearity and controlling its magnitude and phase is straightforward. As a result, it is easy to improve the IIP3 of a system with the second-order nonlinearity generation. To realise this method, a nonlinear circuit is needed to change the magnitude and the phase of its second-order kernel without affecting the other kernels. In this work, in addition to the main path, a separate path from the input to the output in subsystem A is designed with only even-order nonlinear signals. By using this extra path, the magnitude and the phase of the second-order kernel can be changed without any effect on the first- and the third-order kernels.

Fig. 2 shows the proposed mixer based on this linearisation method. In this Figure, $M_{1a} - M_{6a}$ with R_d , L_d and C_d , $M_1 - M_2$, $M_3 - M_6$ and the RC network (R_l and C_l) at the output are the added circuit (subsystem A), the transconductance stage of the conventional mixer (subsystem *B*), the switching stage and the IF stage, respectively. Also, all the parasitic capacitances at the output of subsystem A are modelled by $C_{\rm P}$. The transistors M_{1a} , M_{2a} , M_{5a} and M_{6a} along with the RLC network (R_d , L_d and C_d) make an auxiliary path for the even-order nonlinear signals. In this path, M_{1a} and M_{2a} convert the input signal voltage to a nonlinear current and since the drains of these transistors are connected together, their even-order nonlinear terms are summed up and the odd-order terms are cancelled because of their opposite signs. This current then appears at the output as a voltage while flowing from the RLC network and being amplified by M_{5a} and M_{6a} . Here, only the second-order nonlinear term of this voltage is considered and the other terms are neglected. Moreover, the second-order terms appear at the output through the main path, M_{3a} and M_{4a} . Unlike the auxiliary path that only produces the second-order terms, the main path (M_{3a}) and M_{4a}) also produces the first- and the third-order terms. A_1 , A_2 and A_3 , respectively, being the kernels of the added circuit, are obtained as

$$A_1(\omega_1) = -\frac{g_{m,3a}R_{\text{out},A}}{1 + j\omega_1 R_{\text{out},A}C_p}$$
(5)

$$A_{2}(\pm\omega_{1}, \ \mp\omega_{2}) = \frac{(1/2!)g'_{m,3a}R_{\text{out},A}}{1+j(\Delta\omega)R_{\text{out},A}C_{\text{p}}} - \frac{j(\Delta\omega)R_{d}L_{d} \times 2(1/2!)g'_{m,1a} \times g_{m,5a}R_{\text{out},A}}{(R_{d}+j(\Delta\omega)L_{d}-(\Delta\omega)^{2}R_{d}L_{d}C_{d})(1+j(\Delta\omega)R_{\text{out},A}C_{\text{p}})}$$
(6)

$$A_{3}(\pm\omega_{1}, \pm\omega_{1}, \mp\omega_{2}) = -\frac{(1/3!)g_{m,3a}^{"}R_{\text{out},A}}{1+j(\pm\omega_{1}\pm\omega_{1}\mp\omega_{2})R_{\text{out},A}C_{p}}$$
(7)

where $\Delta \omega = \pm \omega_1 \mp \omega_2$ and $R_{\text{out},A} = r_{ds,3a} || r_{ds,5a}$.



Fig. 2 Proposed mixer

In the above-mentioned equations, $g_{m,3a}$, $g'_{m,3a}$ and $g''_{m,3a}$ are the first-, the second- and the third-order derivatives of the M_{3a} drain current, respectively. In (5), the first-order kernel is calculated that is the same as the voltage TF of subsystem A. In this equation, the

ELECTRONICS LETTERS 16th January 2014 Vol. 50 No. 2 pp. 76–77

magnitude of A_1 is >1, and consequently, the conversion gain will be increased by $20 \times \log |A_1|$. Also, relation (7) shows the third-order kernel. As expected, both these kernels have been formed by only one term due to the transistors in the main path $(M_{3a}$ and $M_{4a})$, whereas the second-order kernel in (6) consists of two terms. The first term originates from the main path and the second term from the auxiliary path. Here, the second term is designed so that it has the most important role in A_2 . As is seen, the magnitude and the phase of this term change according to the values of the RLC network components. Therefore, according to (3), H_3 can be cancelled resulting in an increased A_{IIP3} in (4). Also, the kernels of subsystem B are obtained as follows:

$$B_{1}(\omega_{1}) = g_{m,1}, \quad B_{2}(\pm \omega_{1}, \ \mp \omega_{2}) = \frac{1}{2!}g'_{m,1},$$

$$B_{3}(\pm \omega_{1}, \ \pm \omega_{1}, \ \mp \omega_{2}) = \frac{1}{3!}g''_{m,1}$$
(8)

Simulation results: To evaluate the effectiveness of the proposed technique, the mixer shown in Fig. 2 has been simulated by using a 90 nm CMOS process with Spectre-RF along with the conventional active mixer. It was designed for a 2.4 GHz input signal frequency. A local oscillator with +3.5 dBm power drives the switching transistors. The IIP3 simulations have been conducted by applying a two-tone test with a 5 MHz spacing. The IIP3 results of the proposed and the conventional mixers are illustrated in Fig. 3. This Figure indicates that the proposed mixer has a 17.1 dBm IIP3 which is an improvement by about 13 dB. The simulated conversion gain has been also improved considerably and it is 22.1 dB as shown in Fig. 4. Table 1 summarises the simulation results and compares the proposed mixer with several state-of-the-art linearised mixers [3, 5, 6] with the following figure-of-merit (FoM) [7]:

FoM = 10 log
$$\left(\frac{10^{\text{CG(dB)}/20} \times 10^{(\text{IIP3(dBm)}-10)/20}}{10^{\text{NF(dB)}/10} \times P(\text{mW}) \times V_{\text{DD}}(V)}\right)$$
 (9)



Fig. 3 Simulated IIP3 of proposed and conventional mixers

As is seen, the proposed mixer achieves a high IIP3 and results in an outstanding FoM verifying the usefulness of the proposed linearisation technique as well as the conversion gain improvement.



Fig. 4 Conversion gain of conventional and proposed mixers

Table 1: Simulation results summary

Parameters	Proposed mixer	Conventional mixer	[3]	[<mark>5</mark>] ^a	[<mark>6</mark>] ^a
Frequency (GHz)	2.4	2.4	2.1	1–3	0.3-12
IIP3 (dBm)	17.1	4.1	15	10	-0.8
Conversion gain (dB)	22.1	10.7	15	9.5	8.8
Noise figure (dB)	13.2	12.6	14	16.5	4.8
Power supply (V)	1	1	1.8	1.5	0.9
Power (mW)	4	1.7	8	5.4	24
Process (nm)	90	90	180	180	130
FoM	-4.6	-12.5	-15.6	-20.8	-19.1

^aMeasurement result

Conclusion: Based on the interaction between the two nonlinear systems, a new technique is proposed to improve the value of the IIP3 as well as the conversion gain in the active mixers. The proposed method can also be utilised in CMOS low-noise amplifiers.

© The Institution of Engineering and Technology 2014 23 September 2013

doi: 10.1049/el.2013.3164

One or more of the Figures in this Letter are available in colour online.

M. Asghari and M. Yavari (Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology, 424 Hafez Avenue, Tehran 15914, Iran) E-mail: myavari@aut.ac.ir

References

- Jin, T.H., and Kim, T.W.: 'A 5.5-mW+9.4-dBm IIP3 1.8-dB NF CMOS 1 LNA employing multiple gated transistors with capacitance desensitization', IEEE Trans. Microw. Theory Tech., 2010, 58, (10), pp. 2529-2537
- Wu, C.-L., Yun, Y.H., Yu, C., and O, K.K.: 'High linearity 23-33 GHz SOI CMOS downconversion double balanced mixer', Electron. Lett., 2011, 47, (23), pp. 1283-1284
- 3 Mollaalipour, M., and Miar-Naimi, H.: 'An improved high linearity active CMOS mixer: design and Volterra series analysis', IEEE Trans. Circuits Syst. I, Reg. Pprs., 2013, 60, (8), pp. 2092-2103
- Wambacq, P., and Sansen, W.: 'Distortion analysis of analog integrated circuits' (Kluwer Academic, the Netherlands, 1998), pp. 85-88
- 5 Shi, L.X., Chen, C., Wu, J.H., and Zhang, M.: 'A 1.5-V current mirror double-balanced mixer with 10-dBm IIP3 and 9.5-dB conversion gain', IEEE Trans. Circuits Syst. II, Express Briefs, Reg. Pprs., 2012, **59**, (4), pp. 204–208
- He, S., and Saavedra, C.E.: 'Design of a low-voltage and low-distortion 6 mixer through Volterra-series analysis', IEEE Trans. Microw. Theory Tech., 2012, 61, (1), pp. 177-184
- Vidojkovic, V., van der Tang, J., Leeuwenburgh, A., and van Roermund, A.: 'Mixer topology selection for a 1.8-2.5 GHz multi-standard front-end in 0.18 µm'. IEEE Int. Symp. Circuits and System, Bangkok, Thailand, May 2003, Vol. 2, pp. 300-303