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LETTER

Second-order intermodulation cancelation and conversion-gain enhancement techniques for CMOS active mixers

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SUMMARY

In this paper, two new techniques are proposed to improve the second-order input intercept point (IIP2) and conversion-gain in double-balanced Gilbert-cell complementary metal-oxide semiconductor (CMOS) mixers. The proposed IIP2 improvement technique is based on canceling the common-mode second-order intermodulation (IM2) component at the output current of the transconductance stage. Additionally, the conversion-gain is improved by increasing the fundamental component of the transconductance stage output current and creating a negative capacitance to cancel the parasitic capacitors. Moreover, in the proposed IM2 cancelation technique, by decreasing the bias current of the switching transistors, the flicker noise of the mixer is reduced. The proposed mixer has been designed with input frequency and output bandwidth equal to 2.4 GHz and 20 MHz, respectively. Spectre-RF simulation results show that the proposed techniques simultaneously improve IIP2 and conversion-gain by approximately 23.2 and 5.7 dB, respectively, in comparison with the conventional mixer with the same power consumption. Also, the noise figure (NF) at 20 kHz, where the flicker noise is dominant, is reduced by 4.9 dB. The average NF is increased nearly 0.9 dB, and the value of third-order input intercept point (IIP3) is decreased approximately 1.8 dB. Copyright © 2014 John Wiley & Sons, Ltd.

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KEY WORDS: second-order input intercept point; second-order intermodulation; conversion-gain; CMOS active mixers; flicker noise; direct-conversion receivers

1. INTRODUCTION

CMOS direct-conversion receivers (DCRs) are more attractive rather than other receivers because of their high integration level, low cost, and simplicity of baseband circuitry, and they are widely used in modern wireless terminals. In the realization of some low power applications, such as the emerging Digital Video Broadcasting Handheld standard and cellular code division multiple access, the DCR is a well solution leading to an improved power efficiency and reduced chip area [1]. However, even-order nonlinearities, DC offset, LO leakage, and the flicker noise are the main challenging issues in the design of DCRs affecting their linearity and NF [2–5]. CMOS technology scaling allows to further reduce the area and cost of the chip and makes the realization of the radio frequency (RF) system to be feasible in a single chip [6]. On the other hand, as discussed in [7, 8], the unity current gain frequency (f_T) of MOS transistors is increased by CMOS technology scaling resulting in the reduced minimum noise figure ($NF_{\min}$)

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in RF amplifiers [7]. However, the linearity performance and intrinsic dc gain in MOS transistors are degraded with process scaling [8, 9].

Mixers are one of the important blocks in RF receivers because of their frequency translation capability. The linearity and noise of the mixer have a considerable influence on the total linearity and noise of an RF receiver [10]. It is usually characterized with IIP2 and IIP3 parameters. The double-balanced Gilbert-cell mixer, because of its high port-to-port isolation and high integration level, has been widely used as a down-converter in DCRs. In a perfectly balanced mixer, even-order nonlinearities would not appear at the output. However, in practice, because of the mismatch between the local oscillator (LO) signals, load resistances, and switching transistors, even-order nonlinearities appear at the signal path [11]. The even-order nonlinearities can be attenuated using fully-differential topologies and symmetric layouts. However, the required performance especially for cellular phone applications cannot be often satisfied by these approaches. Therefore, in order to meet the required IIP2 performance for cellular phone applications, it is necessary to use other on-chip schemes such as analog techniques or calibration circuits [11].

Several calibration techniques have been presented to address the IIP2 problem. However, they are often complex and power hungry [12, 13]. Using analog techniques and optimizing the mixer for an improved IIP2 performance are other approaches [14, 15]. The generation of intermodulation products in the switching transistors of a Gilbert-cell mixer has been discussed, and an LC filter to cancel the parasitic capacitance at the output nodes of the transconductance stage is proposed in [14]. However, this mixer employs an on-chip inductor, which occupies a large silicon die area and has the radiation effect in the other parts of the receiver [16]. Several analog techniques based on the feedback loop are presented in [11,17, 18]. However, the study of Vahidfar and Shoaei [17] is not appropriate for wide channel bandwidth applications such as UMTS and IEEE 802.11, and the studies of Vahidfar and Shoaei [11,18] are sensitive to the mismatch between the corresponding devices and need more power [19].

In this paper, two new techniques are proposed to improve the IIP2 and conversion-gain in CMOS active mixers. In the first technique, an IM2 current with an equal magnitude but an opposite phase is generated by employing two auxiliary transistors in parallel with the main transistors of the transconductance stage and two active current mirrors. The very same current is subtracted from the output current of this stage resulting in the cancelation of the IM2 current of the transconductor. In the second technique, the conversion-gain is improved by using the fundamental current of the auxiliary transistors and creating a negative capacitance to cancel the parasitic capacitors caused by the auxiliary transistors. Also, the NF at low frequencies, where the flicker noise is dominant, is reduced by decreasing the dc current in the switching transistors.

The paper is organized as follows. The proposed IM2 cancelation and the conversion-gain improvement techniques along with the noise analysis are explained in Section 2. The Spectre-RF simulation results are provided in Section 3, and finally, the conclusions are presented in Section 4.

2. SECOND-ORDER INPUT INTERCEPT POINT AND CONVERSION-GAIN IMPROVEMENT TECHNIQUES

The conventional double-balanced Gilbert-cell mixer is shown in Figure 1. It is comprised of three transconductance, switching, and load stages. By assuming the switching stage is ideal, the transistors of the transconductance stage are the most dominant sources of distortion. The second-order and third-order intermodulations are the most important parts of the distortion in the transconductor current limiting the IIP2 and IIP3 of the mixer, respectively. This paper is focused to improve both the value of IIP2 and conversion-gain. To do so, two new techniques are introduced to cancel the IM2 and increase the fundamental components in the output current of the transconductance stage. To investigate the mechanism of the aforementioned methods, the Volterra series analysis is employed.

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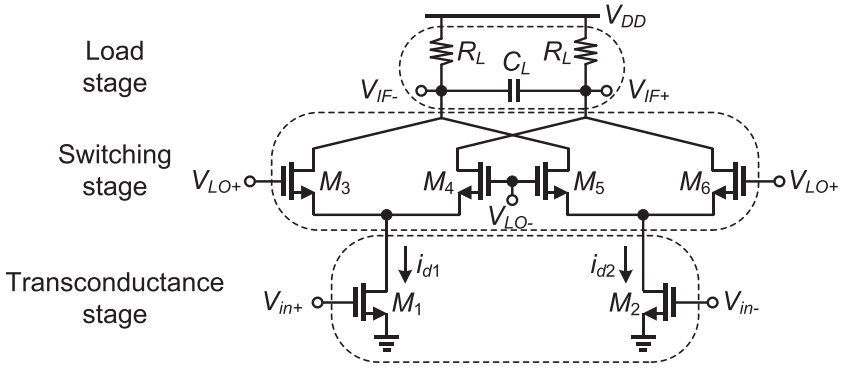

Figure 1. Conventional double-balanced CMOS active mixer.

2.1. *Second-order input intercept point enhancement technique*

A significant portion of the distortion in an active mixer is due to the nonideality in the transistors of the transconductance stage. The distortion in the current of an MOS transistor mainly comes from the nonlinear transconductance (G_m) [20, 21]. Because the high-order coefficients of G_m are negligible, the nonlinear small-signal drain current of an MOS transistor can be expressed by Taylor series expansion as follows:

$$i_d(t) = g_m\big(v_g(t) - v_s(t)\big) + g_m^{'}\big(v_g(t) - v_s(t)\big)^2 + g_m^{''}\big(v_g(t) - v_s(t)\big)^3 + \ldots \tag{1}$$

where g_m is the transconductance, $g_m^{'}$ and $g_m^{''}$ are the first-order and second-order derivatives of the transistor transconductance, respectively. In the aforementioned equation, the first term is the transistor's transconductance, which converts the input voltage signal to a linear current signal. The second and third terms are the sources of distortion in the drain current and are, respectively, the most dominant sources of the second-order and third-order intermodulation components.

In a perfectly balanced transconductor, like the transconductance stage of the conventional mixer shown in Figure 1, the IM2 current, originated from $g_m^{'}$, appears as the common mode at the output current. In practice, when there is a mismatch between the corresponding devices, the IM2 current of each transistor consists of two common mode and differential parts. The common-mode part of the IM2 current is more important than its differential part as shown in the following equation [4,22]:

$$\frac{I_{IM2,diff}}{I_{IM2,CM}} = \frac{3\sigma_{V_{TH}}}{2(V_{GS} - V_{TH})} << 1 \tag{2}$$

where V_{GS}, V_{TH}, and σ_{VTH} are the gate-source voltage, threshold voltage, and standard derivation of the threshold voltage, respectively. The amplitude of IIP2 in the conventional mixer is given by Manstretta *et al.* [4]:

$$A_{IIP2} = \frac{2}{\pi}\frac{g_{m,RF}v_{RF}^2}{\sqrt{L^2\left(I_{IM2,diff}^2 + I_{IM2,CM}^2\right) + \left(\frac{\sigma_R}{R_L}\right)^2 I_{IM2,CM}^2}} \tag{3}$$

where $g_{m,RF}$, L, and σ_R are the total transconductance of the RF stage, low-frequency leakage of the switching transistors, and the standard deviation of mismatch in the load resistances, respectively. As it is seen from Eqs. (2) and (3), the common-mode part cancelation of the IM2 current can be an effective way to improve the IIP2 in an active mixer as it is used in this paper.

The proposed IM2 cancelation circuit in the transconductance stage is shown in Figure 2. In this figure, M_{1a} and M_{2a} convert the input signal voltage to a nonlinear current, and because the drain of these two transistors are connected together, their even-order nonlinear terms are summed up and the odd-order terms are canceled because of their opposite sign. This current is then injected to the

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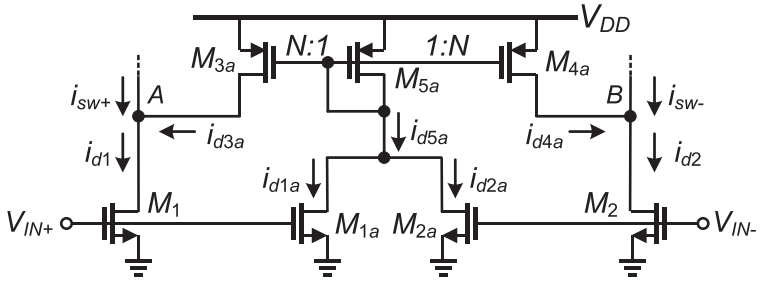

Figure 2. The proposed IM2 cancelation circuit.

drains of M_1 and M_2 (main transistors) while flowing from the diode-connected transistor (M_{5a}) and being amplified N times by M_{3a} and M_{4a} transistors. By assuming M_{1a} and M_{2a} are similar, the injected currents (i_{d3a} and i_{d4a}) are obtained as follows:

$$i_{d3a} = i_{d4a} = \frac{(W/L)_{3a,4a}}{(W/L)_{5a}} \times i_{d5a} = N \times \left(g'_{m1a} v^2_{in+} + g'_{m2a} v^2_{in-}\right) \quad = 2N g'_{m1a} v^2_{in+} \tag{4}$$

By writing Kirchhoff's current law (KCL) at the drains of M_1 and M_2, the output currents of the transconductance stage versus the input signal voltage are obtained as

$$i_{sw+} = i_{d1} - i_{d3a} \quad = g_{m1} v_{in+} + \left(g'_{m1} - 2N g'_{m1a}\right) v^2_{in+} + g''_{m1} v^3_{in+} + \ldots \tag{5}$$

$$i_{sw-} = i_{d2} - i_{d4a} \quad = g_{m2} v_{in-} + \left(g'_{m2} - 2N g'_{m1a}\right) v^2_{in-} + g''_{m2} v^3_{in-} + \ldots \tag{6}$$

According to the relations (5) and (6), the IM2 component in the output current of the transconductance stage can be canceled if the following condition is satisfied:

$$N = \frac{g'_{m1}}{2g'_{m1a}} \tag{7}$$

This condition can be well satisfied by changing the value of N and choosing a proper aspect ratio for M_{1a}. Therefore, the value of A_{IIP2} is considerably enhanced.

2.2. *Conversion-gain improvement technique*

In a Gilbert-cell mixer such as the mixer shown in Figure 1, the input voltage signal is firstly converted to the current by the transconductance stage, and then, this current is commutated to the right and left branches by the switching stage. Finally, the commutated current is converted to the voltage, and the desired signal component (down-converted version of the input signal) is selected by the RC low-pass filter in the load stage. Hence, the voltage conversion-gain of the mixer is obtained as

$$A_V = \frac{2}{\pi} G_m R_L \tag{8}$$

where G_m is the total transconductance of the transconductor. According to the aforementioned equation, the voltage conversion-gain can be enhanced by increasing either the load resistance or the total transconductance of the transconductor. However, the maximum value of the load resistance is limited by the power supply voltage. Here, in order to enhance the conversion-gain, the second way

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is utilized. For this end, the circuit shown in Figure 3 is proposed. In this circuit, the transconductance of the switching pairs (M_3–M_4 and M_5–M_6) with the output conductance of M_1 and M_{3a} (M_2 and M_{4a}), the output conductance of M_{1a} and M_{6a} (M_{2a} and M_{5a}) and the total parasitic capacitance at the nodes A and C, (B and D) are modeled by G_1, G_2, C_{P1}, and C_{P2}, respectively. In this technique, by using a cross-coupled structure, the fundamental component at the drain current of M_{1a} and M_{2a} is used to increase the total transconductance. By applying the Kirchhoff's law at the drains of M_1 and M_2, the output currents of the transconductance stage versus the input voltage are obtained as

$$\begin{aligned} i_{sw+} &= i_{d1} - i_{d3a} \\ &= \left(g_{m1}v_{in+} - Ng_{m2a}v_{in-}\right) + \left(g'_{m1}v_{in+}^2 - Ng'_{m2a}v_{in-}^2\right) + \left(g''_{m1}v_{in+}^3 - Ng''_{m2a}v_{in-}^3\right) + \ldots \\ &= \left(g_{m1} + Ng_{m2a}\right)v_{in+} + \left(g'_{m1} - Ng'_{m2a}\right)v_{in+}^2 + \left(g''_{m1} + Ng''_{m2a}\right)v_{in+}^3 + \ldots \end{aligned} \tag{9}$$

$$\begin{aligned} i_{sw-} &= i_{d2} - i_{d4a} \\ &= \left(g_{m2}v_{in-} - Ng_{m1a}v_{in+}\right) + \left(g'_{m2}v_{in-}^2 - Ng'_{m1a}v_{in+}^2\right) + \left(g''_{m2}v_{in-}^3 - Ng''_{m1a}v_{in+}^3\right) + \ldots \\ &= -\left(g_{m2} + Ng_{m1a}\right)v_{in+} + \left(g'_{m2} - Ng'_{m1a}\right)v_{in+}^2 - \left(g''_{m2} + Ng''_{m1a}\right)v_{in+}^3 + \ldots \end{aligned} \tag{10}$$

The first parenthesis of the aforementioned equations is the total transconductance of the mixer. As is seen, this term is increased by Ng_{m1a}, which is the amplified fundamental current of the auxiliary transistors (M_{1a} and M_{2a}). However, this structure suffers from a drawback. The transfer function of the added path (M_{1a}, M_{6a}, M_{4a} and M_{2a}, M_{5a}, M_{3a}) is given by

$$\frac{I_{d4a}(s)}{V_{in+}(s)} = \frac{g_{m1a}g_{m4a}}{\left(g_{m6a} + G_2\right) + sC_{P2}} \tag{11}$$

which has an extra frequency pole as

$$\omega_p = -\frac{g_{m6a} + G_2}{C_{P2}} \tag{12}$$

This pole, which is caused by the C_{P2} parasitic capacitance, creates a phase lag in the auxiliary paths (M_{1a}, M_{4a}, M_{6a} and M_{2a}, M_{3a}, M_{5a}) and, hence, decreases the amount of the transconductance improvement. In order to reduce the effect of C_{P2}, it can be canceled by two ways. Firstly, an on-chip inductor can be utilized in parallel with C_{P2} so that to resonate it at the working frequency. Secondly, a negative capacitor can be paralleled with C_{P2}. On-chip inductors have a low quality factor (typically, Q is lower than 10) and occupies a large die area. The low Q results in a significantly large series equivalent resistance, which increases the NF and the large area decreases the yield and increases the cost [23]. Additionally, the inductors have the radiation effect in the other parts of the receiver [16]. For these reasons, the second way is utilized here.

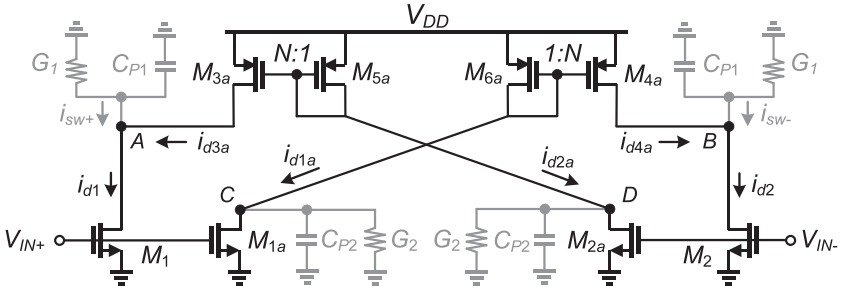

Figure 3. The proposed transconductance stage.

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In order to realize a negative capacitor, the Miller concept is employed. In the circuit shown in Figure 3, the magnitude of the fundamental component in node A is greater than node C, and consequently, by placing a capacitor (C_N) between these two nodes, a negative capacitance can be realized. By assuming the voltage of node A to be K times that of node C (i.e., $v_a = Kv_c$) and placing C_N between these two nodes, the equivalent capacitance seen from the node C can be calculated as follows:

$$q_c = C_N(v_c - v_a) = C_N v_c(1-K) \quad => \quad C_C = \frac{q_c}{v_c} = C_N(1-K) \tag{13}$$

As it is seen, because the value of K is greater than 1 ($K > 1$), the equivalent capacitance seen from the node C will be negative resulting in the parasitic capacitance in the auxiliary path (C_{P2}) to be reduced. However, the equivalent capacitance seen from the node A, caused by C_N, will be positive, and hence, it loads the transconductance stage. Nevertheless, the amount of the fundamental current reduction by this positive capacitance is negligible in comparison with the increasing amount achieved by the negative capacitance, and in overall, the Miller capacitor (C_N) increases the total transconductance of the proposed mixer.

The complete schematic of the proposed mixer is shown in Figure 4. In this circuit, M_1–M_2 with M_{1a}–M_{6a} and C_N, M_3–M_6 and R_L with C_L form the proposed transconductance, switching, and load stages, respectively. To more investigate the IM2 cancelation and conversion-gain improvement mechanisms and considering the impact of the energy storage elements (capacitors), the transconductance stage of the proposed mixer is analyzed using Volterra series. This analysis indicates how the IM2 current of the transconductance stage is attenuated to improve the IIP2 and how it gives the transfer function (the first-order kernel) of the proposed transconductance stage.

The drain voltage of M_1 in Figure 4 can be expressed as follows:

$$V_A = A_1(\omega) \circ V_{in+} + A_2(\omega_1, \omega_2) \circ V_{in+}^2 + A_3(\omega_1, \omega_2, \omega_3) \circ V_{in+}^3 + \ldots \tag{14}$$

where A_1, A_2, and A_3 are the first-order, second-order, and third-order kernels of V_A, respectively. The currents flowing from the switching pairs can be expressed versus the kernels of V_A as

$$\begin{aligned} i_{s+} &= H_1(\omega) \circ V_{in+} + H_2(\omega_1, \omega_2) \circ V_{in+}^2 + H_3(\omega_1, \omega_2, \omega_3) \circ V_{in+}^3 + \ldots \\ &= 2g_{m,sw}\left[A_1(\omega) \circ V_{in+} + A_2(\omega_1, \omega_2) \circ V_{in+}^2 + A_3(\omega_1, \omega_2, \omega_3) \circ V_{in+}^3 + \ldots\right] \end{aligned} \tag{15}$$

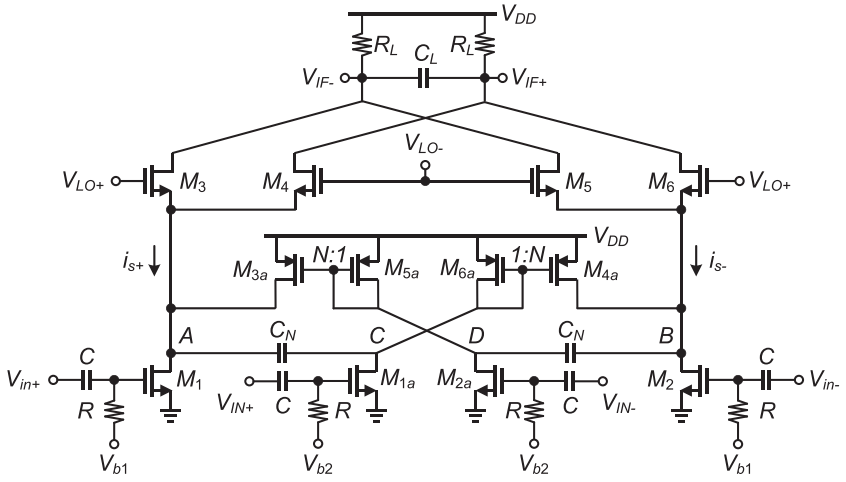

Figure 4. Complete schematic of the proposed mixer.

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$$\begin{aligned} i_{s-} &= H_1(\omega)\circ V_{in-} + H_2(\omega_1,\omega_2)\circ V_{in-}^2 + H_3(\omega_1,\omega_2,\omega_3)\circ V_{in-}^3 + \ldots \\ &= 2g_{m,sw}\left[-A_1(\omega)\circ V_{in+} + A_2(\omega_1,\omega_2)\circ V_{in+}^2 - A_3(\omega_1,\omega_2,\omega_3)\circ V_{in+}^3 + \ldots\right] \end{aligned} \tag{16}$$

where $g_{m,sw}$ is the transconductance of the switching transistors. By assuming $C_N >> C_{P2}$ and $N >> 1$, the first-order and second-order kernels of V_A are given by (the detailed calculations are presented in Appendix A)

$$A_1(\omega) \approx -\frac{[g_{m1} - D_1(\omega)g_{m3a}] + j\omega C_N[(g_{m1} + g_{m1a}) - ND_1(\omega)g_{m6a}]}{G_1 + j\omega\left[C_N\left(1 + \frac{G_1}{G_2}\right) + C_{P1}\right] - \omega^2 C_N\left(\frac{C_{P1}+C_{P2}}{G_2}\right)} \tag{17}$$

$$A_2(\pm\omega_1, \mp\omega_2) = \frac{\begin{pmatrix} -\left(G_2 g'_{m1} + j(\pm\omega_1 \mp \omega_2)\left(C_N\left(g'_{m1} + g'_{m1a}\right) + C_{P2}g'_{m1}\right)\right) \\ -\left(D_1(\omega_1)D_1(\omega_2)g'_{m6a} + D_2(\pm\omega_1, \mp\omega_2)g_{m6a}\right)\left(j(\pm\omega_1 \mp \omega_2)(C_N(N+1) + NC_{P2}) - NG_2\right) \end{pmatrix}}{G_1G_2 + j(\pm\omega_1 \mp \omega_2)(G_1(C_N + C_{P2}) + G_2(C_N + C_{P1})) - (\pm\omega_1 \mp \omega_2)^2(C_N(C_{P1} + C_{P2}) + C_{P1}C_{P2})} \tag{18}$$

In the numerator of Eq. (17), the first and second terms in the first bracket stands for A_1 raised by the transconductance of the main transistors (M_1 and M_2) and the injected fundamental current by M_{3a} (and M_{4a}), respectively, and the second bracket is resulted from the realization of the negative capacitance.

Figure 5 shows the theoretical and simulated magnitude of H_1 versus the values of C_N in the range of 0 to 2 pF. According to this figure, the simulated magnitude of H_1 for $C_N = 0$, when the negative capacitance realization is not used, is equal to −48.5 dB and for $C_N > 1.1$ pF, it is approximately equal to −43.2 dB, which shows that the total transconductance is improved by nearly 5.7 dB. Moreover, as it is seen, by increasing the value of C_N and providing the assumption that $C_N >> C_{P2}$, a good agreement between the simulated and theoretical magnitude of H_1, the behavior of C_N in increasing the magnitude of H_1, is observed. As a result, the effectiveness of the proposed technique is evident.

As can be seen from the relations (15), (16), and (18), by choosing a proper aspect ratio for M_{1a} (and M_{2a}) and tuning the value of N (M_{3a}, M_{5a} and M_{4a}, M_{6a}), one can attenuate H_2 and, hence, improve the IIP2 according to Eq. (3). Equations (15) and (18) state that H_2 can be canceled resulting in an infinite A_{IIP2} provided that the following condition is satisfied (by assuming $C_N >> C_{P2}$ and $N >> 1$):

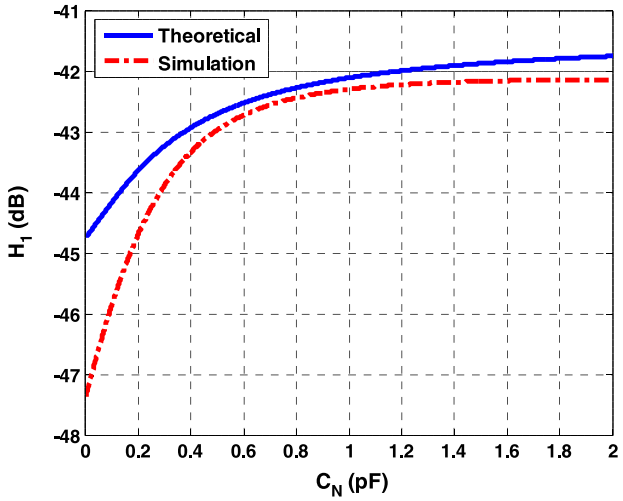

Figure 5. H_1 versus C_N.

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$$N=\frac{G_2 g_{m1}^{'}+j(\pm\omega_1\mp\omega_2)C_N\left(g_{m1}^{'}+g_{m1a}^{'}\right)}{\left(D_1(\pm\omega_1)D_1(\mp\omega_2)g_{m6a}^{'}+D_2(\pm\omega_1,\mp\omega_2)g_{m6a}\right)(G_2-j(\pm\omega_1\mp\omega_2)C_N)} \tag{19}$$

The condition in Eq. (19) can be well satisfied by properly choosing the value of N (the relative aspect ratio in M_{3a}–M_{5a} and M_{4a}–M_{6a} transistors) and the aspect ratio of M_{1a} and M_{2a} auxiliary transistors.

2.3. Noise analysis

In a zero-IF double-balanced Gilbert-cell mixer, the transconductance and load stages are the most dominant sources of thermal noise. The noise components of the transconductance stage at the RF input signal bandwidth are translated in frequency like the input signal. So, by assuming a 50% duty cycle square wave in LO, the thermal noise of the transconductance stage at ω_{LO} and its odd harmonics are translated to output IF band, while the flicker noise is upconverted to ω_{LO} and its odd harmonics. As a result, because the proposed mixer is designed for a zero-IF receiver, only the thermal noise of the transconductance stage is important after the frequency translation. This is because the flicker noise corner frequency of MOS transistors is usually much smaller than the LO frequency [2]. On the other hand, both the thermal and flicker noises of the load stage directly appear at the output IF band [2]. Nevertheless, by using the resistor in the load stage, which is free from the flicker noise, the flicker noise of the mixer is mostly originated from the switching stage [2].

In an active mixer, the NF can separately be defined for each transconductance, switching, and load stages. Because, in the proposed mixer, only the transconductance stage is improved and the switching stage is not changed, to compare the noise performance of the proposed and conventional mixers, the NF of their transconductance stage is calculated here. Of course, according to the NF relation of the cascaded stages in [24], the contribution of the load stage in the total NF of the proposed mixer is decreased because of the conversion-gain enhancement in the transconductance stage.

Using the equivalent half-circuit of the proposed transconductance stage shown in Figure 6, the output noise current of the transconductance stage, due to the devices of the circuit, is obtained as follows:

$$\begin{aligned}\overline{i_{n,out}^2}\Big|_{M_{1,1a,4a,6a}} &= \overline{i_{n,M_1}^2}+\overline{i_{n,M_{4a}}^2}+\left(\overline{i_{n,M_{6a}}^2}+\overline{i_{n,M_{1a}}^2}\right)\left(\frac{g_{m4a}}{g_{m6a}}\right)^2\\ &= 4kT\gamma\left[g_{m1}+g_{m4a}+(g_{m6a}+g_{m1a})(g_{m4a}/g_{m6a})^2\right]\end{aligned} \tag{20}$$

where γ is the excess noise coefficient in short channel MOS devices. Also, the output noise current due to R_S is given by

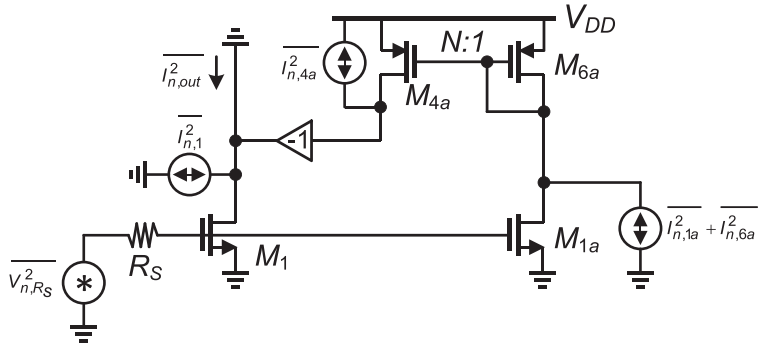

Figure 6. Half-circuit of the proposed transconductance stage for noise analysis.

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$$\overline{i}^2_{n,out}\Big|_{R_S} = \overline{V}^2_{n,R_S}\left[g^2_{m1} + g^2_{m1a}(g_{m4a}/g_{m6a})^2\right] = 4kTR_S\left[g^2_{m1} + g^2_{m1a}(g_{m4a}/g_{m6a})^2\right] \tag{21}$$

Hence, the noise factor of the proposed transconductance stage is obtained as

$$NF_{G_m-stage,\,Proposed} = 1 + \frac{\overline{i}^2_{n,out}\Big|_{M_{1,1a,4a,6a}}}{\overline{i}^2_{n,out}\Big|_{R_S}} = 1 + \frac{\gamma}{R_S} \times \frac{g_{m1} + g_{m4a} + (g_{m1a} + g_{m6a})(g_{m4a}/g_{m6a})^2}{[g_{m1} + g_{m1a}(g_{m1}/g_{m1a})]^2} \tag{22}$$

By assuming $g_{m1} = g_{m4a}$ and $g_{m1a} = g_{m6a}$, the relation (22) is simplified as

$$NF_{G_m-stage,\,Proposed} = 1 + \frac{\gamma}{g_{m1}R_S}\frac{1}{2}\left(1 + \frac{g_{m1}}{g_{m1a}}\right) = NF_{G_m\ stage,\,Conv.} + \frac{1}{2}\frac{\gamma}{g_{m1}R_S}(N-1)\Big|_{N>0} \tag{23}$$

In the aforementioned equation, the first term is the noise factor of the conventional transconductance stage, and the second term is the added noise factor because of the proposed techniques. As it is seen from (23), for $0 < N < 1$, the noise factor of the proposed transconductance stage is lower than the conventional one, and for $N = 1$, they are equal, and finally, for $N > 1$, it is greater than the conventional one. In this work, in order to boost the conversion-gain and reduce the power dissipation (by decreasing the bias current of M_{1a}, M_{2a} and M_{5a}, M_{6a}), $N > 1$ is selected. Consequently, the NF of the proposed mixer, where the thermal noise is dominant, is greater than the conventional mixer.

By considering the thermal noise of the load stage, the noise factor of the proposed mixer by assuming $g_{m1} = g_{m4a}$ and $g_{m1a} = g_{m6a}$ is readily obtained as

$$NF_{Proposed} = NF_{Conv.} + \frac{\pi^2}{8g_{m1}R_S}\left[2\gamma(N-1) - \frac{3}{g_{m1}R_L}\right] \tag{24}$$

In Eq. (24), the first term in the bracket is originated from the noise of the added transistors in the transconductance stage (M_{1a}–M_{6a}). According to $N >> 1$, this term is an additive term that increases the noise factor of the proposed mixer while the second term is negative because of lower thermal noise contribution of the load stage in the proposed mixer compared with the conventional one. Note that the relation (24) gives the single-sideband noise factor of the mixer, and because the proposed mixer is designed for DCRs, its NF is 3 dB less.

As mentioned before, the flicker noise is mostly originated from the switching stage in an active mixer used in a zero-IF receiver. The output flicker noise due to the switching stage in the proposed mixer can be calculated as follows [2]:

$$\begin{aligned} i_{o,n} &= 2\times 4 I_{DC,sw}\frac{V_n}{S\times T} \\ &= 2\times 4\left(I_{DC,sw,conv.} - I_{D,3a}\right)\frac{V_n}{S\times T} = i_{o,n,conv.} - 2\times 4 I_{D,3a}\frac{V_n}{S\times T} \end{aligned} \tag{25}$$

where $I_{DC,sw}$, V_n, S, and T are the bias current of each switching pair (M_3, M_4 and M_5, M_6), low-frequency noise at the gate of switching transistors, slope of the LO signal at the switching time, and the LO period, respectively. As it is seen, because the bias current of the switching stage is reduced, the output flicker noise of the proposed mixer is smaller than that of the conventional one.

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3. SIMULATION RESULTS

The complete schematic of the proposed mixer is shown in Figure 4, and it has been simulated using a 180 nm CMOS process along with the conventional active mixer shown in Figure 1. The mixer is designed to operate in 2.4 GHz input signal and 20 MHz output bandwidth. A LO signal with +5 dBm power drives the switching transistors. The device parameters used in the simulation of the mixers are summarized in Table I.

The complete layout schematic of the conventional and proposed mixers are illustrated in Figure 7, which occupies 430 μm × 195 μm and 480 μm × 277 μm silicon die area, respectively. The following

Table I. Device parameters used in the simulation of the mixers.

Parameter	Proposed mixer	Conventional mixer
$(W/L)_{1,2}$	10 × 2.5 μm/0.18 μm	10 × 2.5 μm/0.18 μm
$(W/L)_{3\text{-}6}$	10 × 2.5 μm/0.18 μm	10 × 2.5 μm/0.18 μm
$(W/L)_{1a,2a}$	2.5 μm/0.18 μm	—
$(W/L)_{3a,4a}$	12 × 2.5 μm/0.18 μm	—
$(W/L)_{5a,6a}$	2.5 μm/0.18 μm	—
R_L	2 kΩ	1.4 kΩ
C_L	2 pF	3.3 pF
C_N	1.2 pF	—

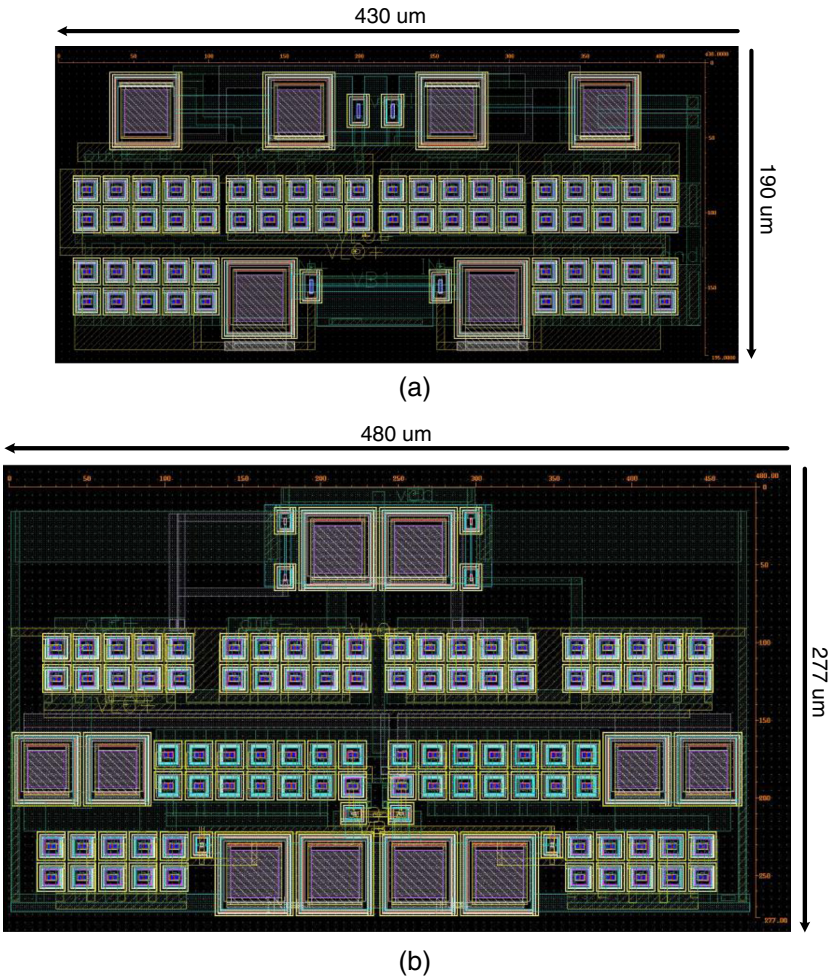

Figure 7. Layout of the (a) conventional and (b) proposed active mixers.

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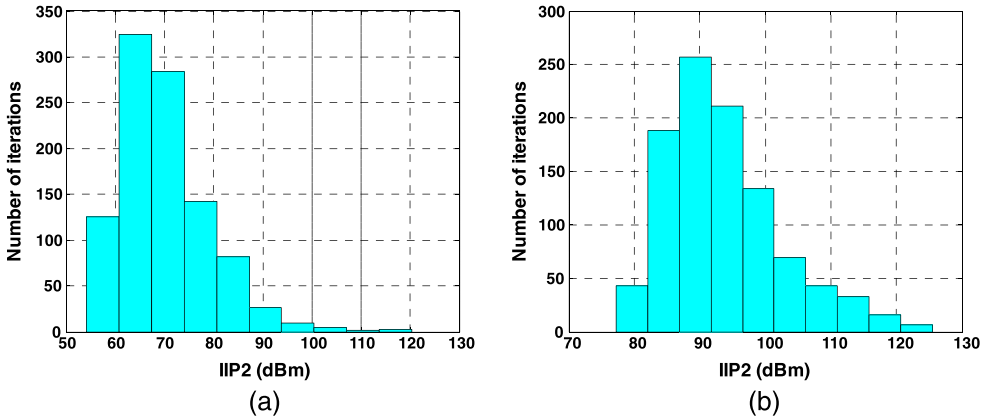

Figure 8. IIP2 Monte-Carlo simulation results of (a) conventional and (b) proposed active mixers.

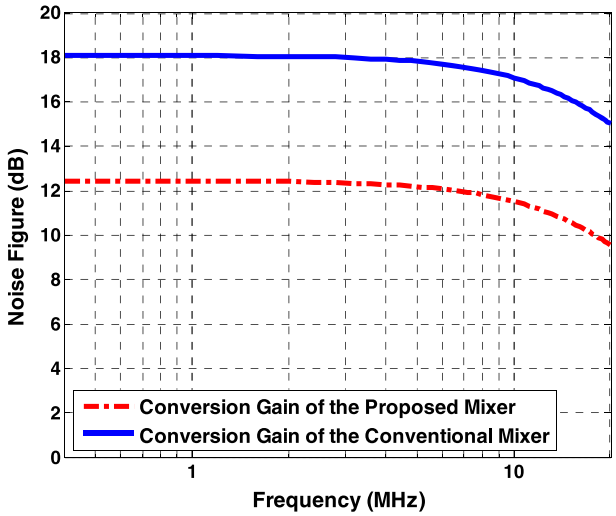

Figure 9. Simulated conversion-gain of the proposed and conventional mixers.

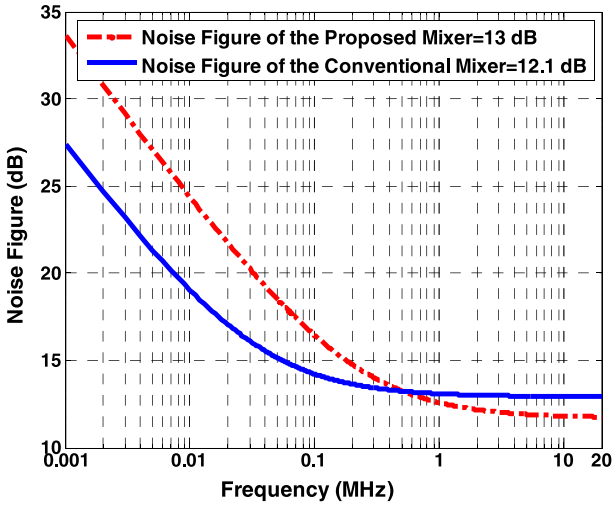

Figure 10. Simulated noise figure of the proposed and conventional mixers.

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Table II. Simulation results of the proposed mixer in different process corner cases and temperature variations.

Parameter	FF at −40 °C	TT at 27 °C	SS at 85 °C
Minimum IIP2 (dBm)	75.7	77.4	78.2
IIP3 (dBm)	−0.5	+0.2	+0.8
Conversion-gain (dB)	19.3	18.1	17.6
Average in-band NF (dB)	12.5	13	13.7
Power supply (V)	1.8	1.8	1.8
Power (mW)	3.9	3.6	3.4

Note: NF = noise figure; FF = Fast Fast; TT = Typical Typical; SS = Slow Slow.

Table III. Performance comparison of the proposed and conventional complementary metal-oxide semiconductor active mixers.

Parameter	Proposed mixer	Conventional mixer
IIP2 (dBm)	77.4	54.2
IIP3 (dBm)	+0.2	+2
Conversion-gain (dB)	18.1	12.45
Average in-band NF (dB)	13	12.1
NF at 20 kHz (dB)	17.1	22
Active area	0.133 mm^2	0.082 mm^2
Power supply (V)	1.8	
Power consumption (mW)	3.6	
Process	180 nm TSMC	

Note: NF = noise figure; TSMC = Taiwan Semiconductor Manufacturing Company.

simulation results are related to the post-layout analysis. To calculate the IIP2 performance, Monte-Carlo simulations with 1000 iterations have been performed by applying a two-tone test with 4 MHz spacing. The Monte-Carlo simulation results of the proposed and conventional mixers are illustrated in Figure 8 indicating that the IIP2 of the mixer, which is improved by the proposed IM2 cancelation technique, is higher than 77.4 dBm while the minimum IIP2 of the conventional mixer is 54.2 dBm, which corresponds to about 23.2 dB improvement.

The simulated conversion-gain for both mixers is depicted in Figure 9. As seen, the conversion-gain of the proposed mixer is 18.1 dB, which is 5.6 dB greater than the conventional mixer. Figure 10 shows the simulated NF. The NF of the proposed mixer due to the flicker noise (NF at 20 kHz) is reduced by nearly 4.9 dB, and the NF at 10 MHz is increased by 0.9 dB. To have a fair comparison in IIP2, conversion-gain, and NF, the same power consumption is used in both proposed and conventional mixers.

The simulation results in different process corner cases and temperature variations are summarized in Table II. This table shows that the parameters of the mixer have small variations in the corner cases, and consequently, the proposed techniques are almost robust. Table III summarizes the simulation results and compares the proposed mixer with the conventional one. As it is seen, the proposed mixer achieves a high IIP2 and conversion-gain while the average NF is increased only by 0.9 dB and the IIP3 is decreased about 1.8 dB compared with the conventional mixer with the same power consumption.

4. CONCLUSIONS

In this paper, two new techniques are proposed to improve the IIP2 and conversion-gain in CMOS active mixers. The first technique removes the output IM2 current of the transconductance stage and, hence, improves the IIP2 by approximately 23.2 dB compared with the conventional mixer. The second technique enhances the conversion-gain of the mixer by increasing the fundamental

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component of the transconductance stage output current along with the realization of a negative capacitance to cancel the parasitic capacitors resulting in about 5.6 dB increased conversion-gain. Also, the proposed transconductance stage decreases the flicker noise of the mixer, and the NF at 20 kHz is reduced about 4.9 dB. In addition, because the proposed techniques are realized in the pseudo-differential transconductance stage, they can be used in low voltage applications as well.

APPENDIX A: THE DERIVATION OF THE VOLTERRA KERNELS FOR THE TRANSCONDUCTANCE STAGE

In this section, the calculation of the Volterra kernels for the transconductance stage of the proposed mixer shown in Figure 4 is presented.

By considering the Taylor series expansion for the drain current of an MOS transistor, the drain current of M_1, M_{1a}, M_{3a}, and M_{6a} can be expressed as

$$I_{d1} = g_{m1}V_{in+} + g_{m1}^{'}V_{in+}^2 + g_{m1}^{''}V_{in+}^3 + \dots \tag{A.1}$$

$$I_{d1a} = g_{m1a}V_{in+} + g_{m1a}^{'}V_{in+}^2 + g_{m1a}^{''}V_{in+}^3 + \dots \tag{A.2}$$

$$I_{d3a} = g_{m3a}(-V_D) + g_{m3a}^{'}(-V_D)^2 + g_{m3a}^{''}(-V_D)^3 + \dots \tag{A.3}$$

$$I_{d6a} = g_{m6a}(-V_C) + g_{m6a}^{'}(-V_C)^2 + g_{m6a}^{''}(-V_C)^3 + \dots \tag{A.4}$$

Also, the drain voltage of M_{1a} and M_{2a} transistors can be defined as follows:

$$V_C = D_1(\omega)\circ V_{in+} + D_2(\omega_1,\omega_2)\circ V_{in+}^2 + D_3(\omega_1,\omega_2,\omega_3)\circ V_{in+}^3 + \dots \tag{A.5}$$

$$\begin{aligned} V_D &= D_1(\omega)\circ V_{in-} + D_2(\omega_1,\omega_2)\circ V_{in-}^2 + D_3(\omega_1,\omega_2,\omega_3)\circ V_{in-}^3 + \dots \\ &= -D_1(\omega)\circ V_{in+} + D_2(\omega_1,\omega_2)\circ V_{in+}^2 - D_3(\omega_1,\omega_2,\omega_3)\circ V_{in+}^3 + \dots \end{aligned} \tag{A.6}$$

where D_1, D_2, and D_3 are the first-order, second-order, and third-order Volterra kernels of V_C (and V_D), respectively. By applying the Kirchhoff's law at the drains of M_1 and M_{1a}, the voltage of nodes A and C are obtained as

$$node\ A:\ v_A(t)G_1 + C_{P1}\frac{dv_A(t)}{dt} + C_N\frac{d(v_A(t)-v_C(t))}{dt} + i_{d1}(t) + i_{d3a}(t) = 0 \tag{A.7}$$

$$node\ C:\ C_N\frac{d(v_C(t)-v_A(t))}{dt} + G_2v_C(t) + C_{P2}\frac{dv_C(t)}{dt} + i_{d1a}(t) + i_{d6a}(t) = 0 \tag{A.8}$$

where

$$G_1 = g_{m3} + g_{m4} + g_{ds1} + g_{ds3a} \tag{A.9}$$

$$G_2 = g_{ds1a} + g_{ds6a} \tag{A.10}$$

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$$C_{P1} \approx C_{db1} + C_{db3a} + C_{gs3} + C_{gs4} + C_{sb3} + C_{sb4} \tag{A.11}$$

$$C_{P2} \approx C_{db1a} + C_{db6a} + C_{gs6a} + C_{gs4a} \tag{A.12}$$

Substituting Eqs. (A.1), (A.2), (A.3), and (A.4) into the frequency domain representation of Eqs. (A.7) and (A.8), the first-order and second-order kernels of V_A are calculated as

$$A_1(\omega) = -\frac{(G_2 g_{m1} + s(C_N(g_{m1a} + g_{m1}) + C_{P2} g_{m1})) - D_1(\omega) g_{m6a}(NG_2 + s(NC_{P2} + (N-1)C_N))}{G_1 G_2 + j\omega(G_1(C_N + C_{P2}) + G_2(C_N + C_{P1})) - \omega^2(C_N(C_{P1} + C_{P2}) + C_{P1}C_{P2})} \tag{A.13}$$

$$A_2(\pm\omega_1, \mp\omega_2) = \frac{\begin{pmatrix} -\left(G_2 g'_{m1} + j(\pm\omega_1 \mp \omega_2)\left(C_N\left(g'_{m1} + g'_{m1a}\right) + C_{P2} g'_{m1}\right)\right) \\ -\left(D_1(\omega_1) D_1(\omega_2) g'_{m6a} + D_2(\pm\omega_1, \mp\omega_2) g_{m6a}\right)\left(j(\pm\omega_1 \mp \omega_2)(C_N(N+1) + NC_{P2}) - NG_2\right) \end{pmatrix}}{G_1 G_2 + j(\pm\omega_1 \mp \omega_2)(G_1(C_N + C_{P2}) + G_2(C_N + C_{P1})) - (\pm\omega_1 \mp \omega_2)^2(C_N(C_{P1} + C_{P2}) + C_{P1}C_{P2})} \tag{A.14}$$

By assuming $C_N >> C_{P2}$ and $N >> 1$, Eq. (A.13) is simplified as

$$A_1(\omega) \approx -\frac{[g_{m1} - D_1(\omega) g_{m3a}] + j\omega C_N[(g_{m1} + g_{m1a}) - N D_1(\omega) g_{m6a}]}{G_1 + j\omega\left[C_N\left(1 + \frac{G_1}{G_2}\right) + C_{P1}\right] - \omega^2 C_N\left(\frac{C_{P1} + C_{P2}}{G_2}\right)} \tag{A.15}$$

where the first-order and second-order Volterra kernels of the V_C (and V_D) are given by

$$D_1(\omega) = -\frac{g_{m1a} G_1 + j\omega[C_N(g_{m1} + g_{m1a}) + C_{P1} g_{m1a}]}{\begin{pmatrix} G_1(G_2 + g_{m6a}) + j\omega[C_N(G_1 + G_2 + g_{m6a}(1-N)) + C_{P1}(G_2 + g_{m6a}) + G_1 C_{P1}] \\ -\omega^2[C_N(C_{P1} + C_{P2}) + C_{P1}C_{P2}] \end{pmatrix}} \tag{A.16}$$

$$D_2(\pm\omega_1, \mp\omega_2) = -\frac{\begin{pmatrix} G_1\left(g'_{m1a} + D_1(\pm\omega_1) D_1(\mp\omega_2) g'_{m6a}\right) \\ +j(\pm\omega_1 \mp \omega_2)\left[C_N\left(g'_{m1} + g'_{m1a} + g'_{m6a}(N+1)\right) + C_{P1}\left(g'_{m6a} + g'_{m1a}\right)\right] \end{pmatrix}}{\begin{pmatrix} G_1(G_2 + g_{m6a}) - (\pm\omega_1 \mp \omega_2)^2[C_N(C_{P1} + C_{P2}) + C_{P1}C_{P2}] \\ +j(\pm\omega_1 \mp \omega_2)[C_N(G_1 + G_2 + g_{m6a}(1-N)) + C_{P1}(G_2 + g_{m6a}) + G_1 C_{P1}] \end{pmatrix}} \tag{A.17}$$

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