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A Fully-Differential Chopper Capacitively-Coupled Amplifier with High Input Impedance for Closed-Loop Neural Recording

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Abstract
In this paper, a chopper capacitively-coupled instrumentation amplifier (CCIA) with high input impedance and low input-referred noise is presented for closed-loop neural recording. A recycling folded-cascode amplifier with an inherent common-mode feedback (CMFB) circuit is proposed as the first stage to tolerate large common-mode and differential in-band artifacts without any extra circuit since this structure has a large input common-mode range. Also, this structure can improve the noise efficiency factor (NEF) due to the smaller current consumption with the same gain and bandwidth than the conventional folded-cascode amplifier. The fully-differential common-source amplifier is used as the second stage for achieving a large output signal swing. Hence, the proposed chopper CCIA has a small total harmonic distortion (THD). The proposed pseudo resistor has a large amount and enough THD with less sensitivity to the PVT variations. It has made the small low cut-off frequency in the proposed chopper CCIA by using small capacitors in the DC servo-loop. Therefore, the total value of the on-chip capacitors is reduced. By reducing the low cut-off frequency in chopper CCIA, the positive feedback loop increases the input impedance at a low frequency more than the previous works using the positive feedback loop, despite the presence of DC servo-loop in the chopper CCIA. The proposed neural recording amplifier has been simulated with Cadence using TSMC 180 nm CMOS process with a 1.8 V power supply.

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1 Introduction

The neural recording is the essential tool for identifying the activity of the brain. The information extracted from the neural recording is used to diagnose Epilepsy and Parkinson's diseases. Neural stimulation is as important as neural recording to treat diseases, especially in resistant patients to drug therapy. Local field potential (LFP) and action potential (AP) are the recorded neural signals that are used in neuroscience research. The amplitude of these signals is about one micro-volt to a few milli-volts. The frequency range of the LFP signals and AP signals are from 1 to 200 Hz and from 200 Hz to 5 kHz, respectively [1, 6, 14, 25]. In the neural recording, the neural signals and background noise of the electrodes are extracted. Several electrodes are used to record neural signals, and each of the electrodes senses the signal of some neurons [2]. The wet electrodes are not appropriate enough for long-term monitoring because of their dependence on the gel. In this case, the equivalent circuit of wet electrode and gel is a parallel resistor and capacitor in series with another resistor whose equivalent impedance can be up to a few kΩ. The dry electrodes have been used instead of wet electrodes because these electrodes can provide long-term neural signal recording and user comfort. However, the drawback of the dry electrode is their high impedance that can be up to a few MΩ at 50/60 Hz. The equivalent circuit of a dry electrode is a parallel resistor and capacitor in which the capacitor and the resistor are 10 nF and 1 MΩ, respectively [33].

In a closed-loop neuromodulation system, the neural signals are simultaneously recorded with stimulation, where information of the stimulation is adopted through the feedback path [8]. This ensures that stimulation is only applied when it is obligatory and with the required intensity. Hence, the unpleasant effects of open-loop stimulation are mitigated, and the treatment advantages are increased in closed-loop neuromodulation [8, 30].

In the neural recording, one of the challenges is the low input-referred noise of the amplifier. The input-referred noise of the analog front-end amplifier, which includes flicker and thermal noises, should be in a few micro-volts ranges [15]. Large input transistors can reduce the flicker noise, but this technique cannot decrease the flicker noise enough, as used in [12, 26]. The chopper is an efficient way to reduce the low-frequency flicker noise of the capacitively-coupled instrumentation amplifier (CCIA).

The input chopper could be used after the input capacitors or before them. In the first case, the low-frequency $1/f^2$ shaped noise is created [29]. Also, in [20], the common-mode rejection ratio (CMRR) due to the mismatch of the input capacitors is decreased because these mismatches along with the desired signal are modulated to the chopping frequency. In [6, 8, 13, 15], the input chopper is placed before input capacitors, so the CMRR is improved, but the input impedance is decreased due to the switched-capacitor equivalent resistance of the chopper switches.

One of the most critical challenges in the neural recording is the offset voltage of the electrodes. The value of this offset voltage depends on the electrode material and contact area, and it is about several mV up to 50 mV [15]. Two main techniques are usually utilized to realize low cut-off frequency in neural amplifiers. In the first scheme, a pseudo resistor is employed parallel with feedback capacitors if the chopper is not around the CCIA, as used in [26, 29]. In the chopper amplifier, for creating the low cut-off frequency, a DC servo-loop, which has consisted of an integrator with a considerable time constant and chopper in the feedback loop, is utilized. In this way, a higher CMRR is achieved with lower flicker noise due to using the chopper. To achieve small low cut-off frequency, the pseudo resistors are utilized that consume smaller area with far more resistance than the passive resistors. However, the pseudo resistors are sensitive to the PVT variations, and they are also nonlinear.

In [12, 28], the pseudo resistors are in the sub-threshold region, and hence, the sensitivity to the process variations is increased. Besides, in [28], the bias circuit for the pseudo resistor is an NMOS transistor that is different from the transistors of the pseudo resistor. Thus, it is more sensitive to the PVT variations. The reported maximum value of this pseudo resistor is about 1 GΩ. In [22], for decreasing the sensitivity to the PVT variations, the transistors of the pseudo resistor and bias circuit are the same type. An operational amplifier is used in this bias circuit for setting the source voltage of the bias circuit. Hence, the power consumption and area of the presented pseudo resistor in [22] are increased. The reported maximum value of this variable pseudo resistor is about 70 GΩ with 54,000 μm^2 area in a 0.35 μm CMOS process.

In the proposed pseudo resistor in [19], instead of the source follower, a differential pair is used as the bias circuit. The pseudo resistor is biased in the sub-threshold region, and the reported maximum value of this pseudo resistor is 18 GΩ.

A duty-cycled resistor (DCR) is utilized in [6], which includes a switch and poly resistor. DCR has a complicated bias circuit. To realize a large resistance, the bias circuit becomes more complex, and the total value of integrator capacitors in DC servo-loop based on the RC integrator in a single-ended circuit is 20 pF. Also, this pseudo resistor suffers from the aliasing issue because it employs the sampling technique. A multi-rate duty-cycled resistor (MDCR) has been used in [8, 13] with series of two DCRs. The value of these pseudo resistors in DC servo-loop has not been increased enough, and the total value of integrated capacitors in DC servo-loop based on the RC integrator are 24 pF and 48 pF in [8, 13], respectively. In these works, since the value of the utilized pseudo resistors is not large enough, a large amount of capacitors are needed to achieve a very large time constant in DC servo-loop. A DC servo-loop based on the Gm-C integrator is used in [15] to reject the DC offset of the electrodes. But, it needs large total integrator capacitors to realize the sub-Hz high-pass corner and the total value of integrated capacitors in DC servo-loop is about 80 pF.

As mentioned, if the input chopper is placed before the input capacitors, the input impedance is reduced. In [6], an auxiliary path is used to increase the input impedance in chopper CCIA. However, due to the limited bandwidth of the buffer, the input impedance is not increased sufficiently. The input-referred noise of the chopper CCIA is also increased by the buffer noise since the flicker noise of the buffer is directly added to the input-referred noise of the total circuit. In [8], a chopper is used in the auxiliary path for alleviating this problem. Moreover, the offset of the buffer is amplified and

saturates the neural recording amplifier. Besides, in this method, by increasing the input capacitors for higher gain, the input resistance is reduced. To alleviate this issue, a current feedback amplifier is proposed in [30]. The auxiliary path is added to the current feedback chopper amplifier, and the gain of the chopper CCIA is independent of the input capacitors, C_{in}, but the gain variation in process mismatches is increased. The other method for increasing the input impedance is the positive feedback loop [13, 15]. However, due to parasitic capacitances, the input impedance increment is limited [10]. The positive feedback loop is disabled at DC frequency because the positive feedback loop is driven by the output of the chopper CCIA and the DC servo-loop attenuates the DC signal at the output [1].

In closed-loop neuromodulation, large stimulation artifacts are generated at the frequency range of the desired signals. Because of the direct paths through the cerebrospinal fluid and capacitive coupling between electrodes and recording electronics, these large stimulation artifacts appear at the recording sites. These artifacts consist of differential and common-mode components. The maximum amplitude of the differential component is about 100 mV and the maximum amplitude of the common-mode artifact is about 500 mV [8].

To preserve the neural signal in the presence of artifacts, the neural recording amplifier, as the first block, should have a high dynamic range. The mid-band gain of the CCIA is usually limited to about 30 dB to prevent the saturation of the closed-loop neural recording [6, 8]. However, by reducing the mid-band gain, the required resolution of the succeeding analog-to-digital converter (ADC) is increased. A low-power ADC with a 15.2 effective number of bits (ENOB) is proposed in [5]. The last block is the adaptive artifact rejection engine that is proposed in [3], which is used to separate the neural signals from large artifacts. In this paper, the focus is on the front-end amplifier.

In [6], a current-reused differential pair is used in the chopper CCIA with small power consumption for achieving the AP band. But the input common-mode range of this circuit is less than the required input common-mode range. An extra circuit has been used in [8] to attenuate large common-mode artifacts. In this circuit, the common-mode artifact is amplified by an amplifier with capacitive feedback. Then, the amplified common-mode artifact is subtracted from the input common-mode artifact through capacitors. Due to using capacitors and amplifier in this extra circuit, both area and power consumption are increased. The structure in [13] as the first stage has sufficient input common-mode range, but its power consumption is large for recording AP signals. Therefore, compared with open-loop neural recording systems, a large dynamic range and large input common-mode range are needed in closed-loop neural recording amplifiers.

In this work, the proposed chopper CCIA is realized by using a two-stage Miller compensated amplifier, the positive feedback loop, a DC servo-loop based on the RC integrator, and ripple reduction capacitors. The first stage is a recycling fully-differential folded-cascode amplifier with an inherent common-mode feedback (CMFB) circuit. The first stage can tolerate large common-mode stimulation artifacts without increasing the input-referred noise and saturating the chopper amplifier. The second stage is a fully-differential common-source amplifier to achieve large output signal swing. Also, a new pseudo resistor with large resistance, high linearity, and a

small area is utilized in DC servo-loop, which reduces the low cut-off frequency with small capacitors in DC servo-loop. By reducing the low cut-off frequency, the positive feedback loop can operate in low frequency with the presence of DC servo-loop in the total circuit.

The rest of the paper is organized as follows. In Sect. 2, the structure of the proposed chopper CCIA and its building blocks are presented. Extensive post-layout circuit-level simulation results are provided in Sect. 3. Finally, Sect. 4 concludes the paper.

2 Proposed Closed-Loop Neural Recoding Amplifier

2.1 Overall Structure

Figure 1 shows the proposed overall system architecture, which consists of a CCIA with a two-stage Miller compensated amplifier (G_{m1} and G_{m2}), a capacitive feedback loop for setting the mid-band gain, a positive feedback loop for increasing the input

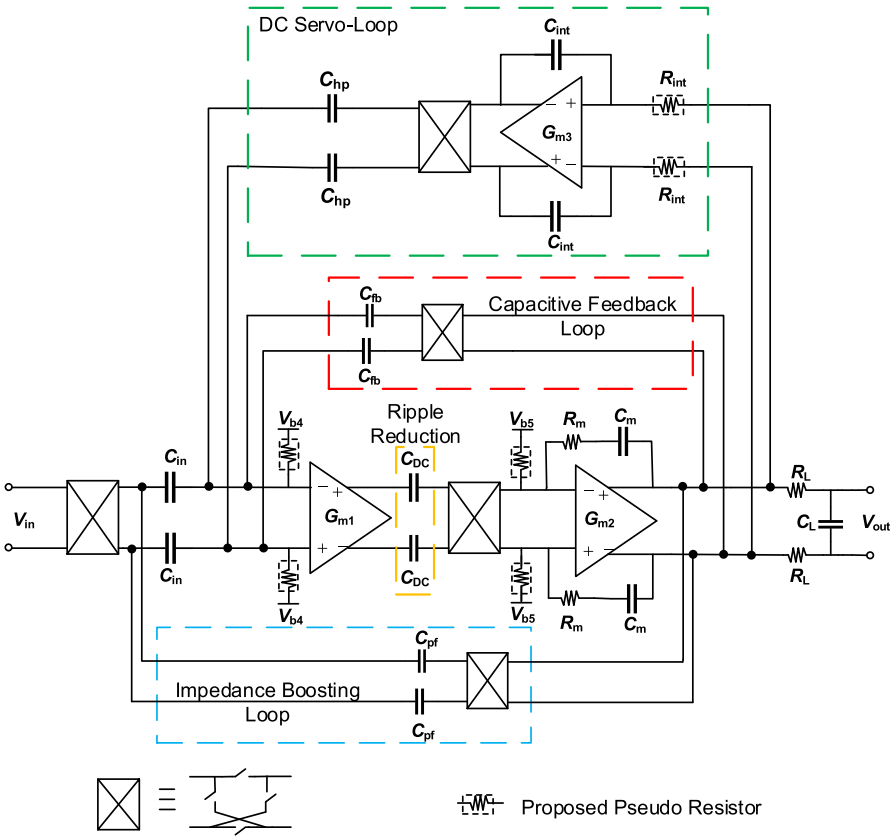

Fig. 1 Structure of the proposed closed-loop neural amplifier

impedance, a DC servo-loop based on the RC integrator for rejecting the large electrode offset, ripple reduction capacitors (C_{DC}), and chopping switches for reducing the flicker noise. G_{m1} can tolerate large common-mode and differential in-band artifacts. G_{m2} has a large output swing to achieve suitable total harmonic distortion (THD). The presented pseudo resistor in DC servo-loop allows achieving small low cut-off frequency. Pseudo resistors have been used to bias the input transistors in G_{m1} and G_{m2}. The closed-loop pass-band gain of the total circuit is determined by the ratio of input and feedback capacitors as $G_V = C_{in} / C_{fb}$. The pass-band open-loop gain of the proposed amplifier is given by:

$$A_V = \left(\frac{2A+1}{A}\right) g_{m1} g_{m14} R_{o1} R_{o2}. \tag{1}$$

where parameter A is shown in Fig. 2 in G_{m1}, g_{m1}, and g_{m14} are transconductances of the transistors M_1 and M_{14} in Figs. 2 and 4, respectively. R_{o1} and R_{o2} are the output resistances of G_{m1} and G_{m2}, respectively. The high cut-off frequency of the total closed-loop structure is given by:

$$f_H = \frac{1}{2\pi} \frac{C_{fb}}{C_{in} + C_{fb}} \left(\frac{2A+1}{A}\right) \frac{g_{m1}}{C_m}. \tag{2}$$

where C_m is the Miller compensation capacitor as shown in Fig. 1.

2.2 Two-Stage Amplifier

The proposed chopper CCIA consists of G_{m1} and G_{m2}. Figure 2 shows the structure of the first stage and its bias circuit. The input common-mode range of the proposed G_{m1} is more appropriate than the current-reused differential pair for closed-loop neural recording. Also, the presented structure has smaller current consumption with the same gain and bandwidth compared to the conventional folded-cascode amplifier.

The transistors $M_{5a,6a}$ are used to create the wide-swing cascode current mirrors to improve the matching [34]. The cross-coupled M_7-M_{12} transistors also realize the inherent CMFB circuit for the recycling folded-cascode amplifier in G_{m1}. To guarantee stability and have less sensitivity to the PVT variations, g_{m9} (transconductance of M_9) is selected to be $0.8g_{m11}$ since in this case, the output resistance will be positive with sufficient margin. The output common-mode voltage is set by M_7-M_{12} transistors due to their small common-mode resistance without needing an explicit continuous-time CMFB circuit and some more power consumption. However, the cross-coupled transistors reduce the output swing, which is not essential in the first stage since its output signal swing is not large. To reduce the input-referred noise and power consumption, the input transistors of G_{m1} and G_{m2} are biased in the sub-threshold region since in this region, the g_m of the transistors is larger than the strong inversion region. Due to the chopper structure, the flicker noise of the chopper CCIA is highly attenuated, and hence, the thermal noise is the essential remained noise source.

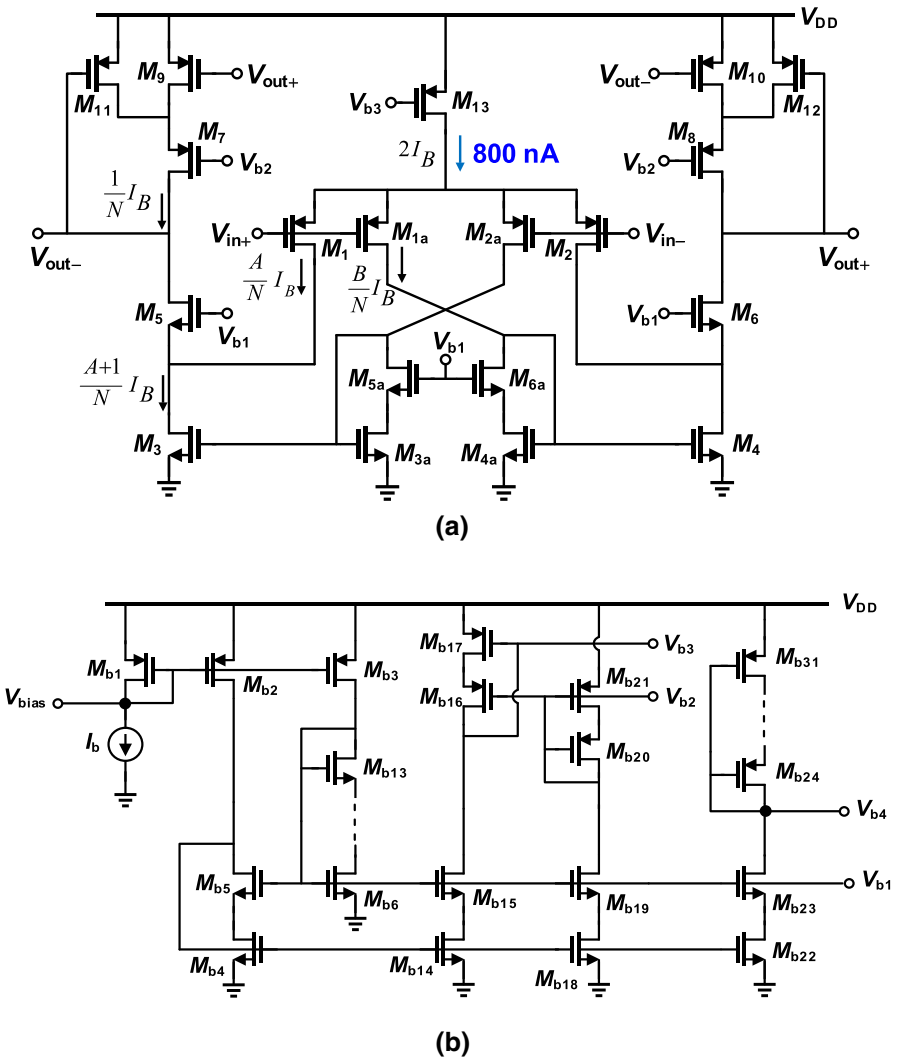

Fig. 2 Schematic of the **a** first-stage (G_{m1}) amplifier and **b** its bias circuit

The current noise power spectral density (PSD) for a sub-threshold MOS transistor is given by [23]:

$$i_n^2 = 4kT\frac{1}{2n}g_m = 2kT\frac{I_D}{V_T}. \tag{3}$$

where k is the Boltzmann's constant, T is the absolute temperature, V_T is the thermal voltage, and n is the sub-threshold slope factor. In this work, to reduce the noise of the first stage, the design method proposed in [23] is utilized. In Fig. 2a, $N = A + B$ and the current of transistors $M_{3,4}$ is decreased compared to the conventional folded-cascode

amplifier. Hence, the current mirror factor is $(A + 1)/B$ in the first-stage amplifier as shown in Fig. 2a.

The input-referred voltage noise PSD of the first-stage amplifier considering $M_{1\text{-}2}$ and $M_{1a\text{-}2a}$ input transistors is obtained as:

$$V_{ni}^2 = \frac{4kTI_B}{V_T}.\left[\frac{A}{N} + \frac{B}{N}\left(\frac{A+1}{B}\right)^2\right].\left[\frac{N}{(2A+1)}.\frac{V_T}{nI_B}\right]^2. \tag{4}$$

On the other hand, the input-referred noise PSD of a simple sub-threshold differential pair is given by:

$$V_{ni,diff}^2 = 2V_{n1}^2 = 4kT\frac{V_T}{n^2 I_B}. \tag{5}$$

By normalizing the input-referred noise PSD of G_{m1} and considering the noise of input transistors by the input-referred noise PSD of a simple sub-threshold differential pair, the following relation is obtained:

$$\frac{V_{ni}^2}{V_{ni,diff}^2} = N\frac{A + (A+1)^2/B}{(2A+1)^2} = N\frac{A + (A+1)^2/(1 - A/N)}{(2A+1)^2} \tag{6}$$

To reduce the power consumption, N is assumed 24 and the current of $M_{7,8}$ transistors are decreased as much as possible. Equation (6) is plotted in Fig. 3. As shown in Fig. 3, with $A = 12$, the amount of the input-referred noise PSD of the input transistors in G_{m1} will be approximately equal with a simple differential pair.

The input common-mode range V_{IC} of the G_{m1} is given by V_{GS4a}—$|V_{GS1a}|$ < V_{IC} < V_{DD}—$|V_{GS1}|$—$|V_{eff13}|$, where V_{DD} is the supply voltage, $V_{GS1,1a,4a}$ are the gate-source voltages of transistors $M_{1,1a,4a}$, and V_{eff13} is the overdrive voltage of the transistor M_{13}. This range is more appropriate than the input common-mode range of

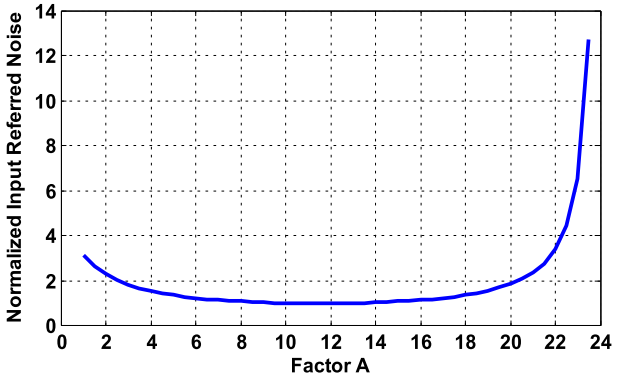

Fig. 3 The normalized input-referred noise of the first-stage amplifier for obtaining the optimal value of A

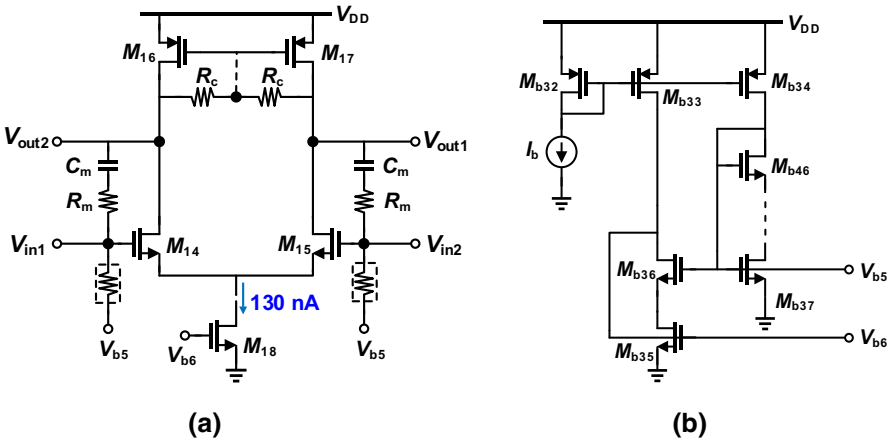

Fig. 4 Schematic of the **a** second-stage (G_{m2}) amplifier and **b** its bias circuit

the current-reused differential pair, and hence, it can tolerate a large input common-mode range.

Figure 4 shows the second-stage amplifier and its bias circuit. R_c is used to define the output common-mode voltage for this stage, and in order not to reduce the output resistance and gain of G_{m2}, pseudo resistors are considered to realize these resistors. The fully-differential common-source amplifier as G_{m2} has a convenient output signal swing, and thus, the overall structure has appropriate THD for neural recording amplifier. The Miller compensation with a nulling resistor provides a dominant pole in the proposed chopper CCIA and makes it stable.

The main noise contributions in the total amplifier are the transistors $M_{1\text{-}4}$, $M_{1a\text{-}4a}$, and $M_{9\text{-}12}$. As shown in relation (6), the noise contribution of the input transistors $M_{1,2}$ and $M_{1a,2a}$ is equal with a simple sub-threshold differential pair. The total input-referred voltage noise PSD of the presented open-loop two-stage amplifier is about:

$$\begin{aligned} V_{ni,amp}^2 &\approx 4kT\frac{V_T}{n^2 I_B} + 2\left[i_{n3,4}^2 + \left(\frac{A+1}{B}\right)^2 .i_{n3a.4a}^2 + i_{n9,10}^2 + i_{n11,12}^2 \right. \\ &\quad \left. +(i_{n14,15}^2 + i_{n16,17}^2).\frac{1}{g_{m14}^2 R_{o1}^2} \right] \frac{A^2}{((2A+1)g_{m1})^2} \\ &\approx 4kT\frac{V_T}{n^2 I_B} + 8kT\gamma \left[g_{m3,4} + \left(\frac{A+1}{B}\right)^2 .g_{m3a,4a} + g_{m9} + g_{m11} \right. \\ &\quad \left. + \frac{1}{g_{m14}R_{o1}^2} + \frac{g_{m16}}{g_{m14}^2 R_{o1}^2} \right] \frac{A^2}{((2A+1)g_{m1})^2} \end{aligned} \tag{7}$$

2.3 Chopper Structure

The current noise PSD produced by the CMOS switches in the chopper is higher than the other chopper switches, but the charge injection of the CMOS switches is lower than the other chopper switches [32]. Besides, the CMOS switches have higher linearity than the other chopper switches. There is a trade-off between the current noise PSD, charge injection, and linearity. Hence, the CMOS switches have been used in this chopper CCIA. To improve the linearity of the CMOS switches, the width of the PMOS transistors of the CMOS switches, M_{ps}, is selected larger than the width of the NMOS transistors of the CMOS switches, M_{ns}, due to the difference in their mobility [24].

There is a trade-off between the total input-referred noise in the base-band and the residual offset with the chopping frequency. Therefore, it is better that the chopping frequency to be equal to the amplifier corner frequency [9, 17]. Also, the chopping frequency should be selected in such a way that after modulating and transmission of the main signal to the chopping frequency, the main signal is still amplified. In this work, considering these conditions, the chopping frequency is selected 25 kHz. As mentioned in the introduction section, for increasing the CMRR, the input chopper is placed before input capacitors (C_{in}).

2.4 Proposed Pseudo Resistor

In the chopper CCIA, due to the large electrode offset, DC servo-loop is utilized to avoid the saturation of the chopper amplifier at low frequency. One of the most critical elements in DC servo-loop is the pseudo resistor.

In this paper, a pseudo resistor with a large value is proposed, and its structure is shown in Fig. 5. Transistors $M_{\mathrm{p1,p2}}$ act as the pseudo resistor and transistors $M_{\mathrm{p3\text{-}p8}}$ are utilized as the bias circuit in this pseudo resistor which two pseudo resistors are used in series to boost the amount of resistance. The proposed pseudo resistor has been forced to be in the cut-off region by the bias circuit which is a differential pair while previous pseudo resistors are biased in sub-threshold region. The sub-threshold region is far more sensitive to PVT variations than the other transistor operating regions. This bias

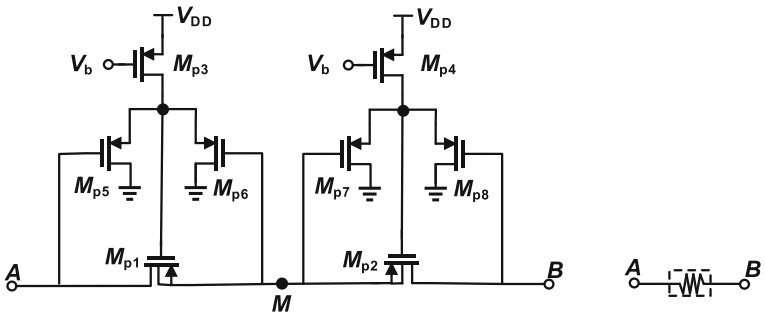

Fig. 5 The proposed pseudo resistor

circuit has created a constant negative voltage for V_{SG} of transistors $M_{p1,p2}$. Hence, the resistance value of the proposed pseudo resistor has been increased, and it has a larger resistance than a variable pseudo resistor in [19] which is biased in sub-threshold region whereas the proposed pseudo resistor in this paper has a fixed amount. Because by changing the V_{AB}, the negative source-gate voltage of $M_{p1,p2}$ transistors changes slightly.

In the proposed structure, the transistors of the bias circuit and pseudo resistors are both PMOS. Hence, the sensitivity to the process and voltage variations is decreased. Therefore, the low cut-off frequency variations in DC servo-loop are decreased in different process corner cases and power supply variations.

In the proposed pseudo resistor, if the difference voltage between nodes A and M be small, both $M_{p5,6}$ transistors are biased in the saturation region. In the proposed amplifier circuit, the pseudo resistor is used at the input of G_{m1} and G_{m2} and their bias circuit, and thus, the difference voltage of nodes A and M is small, and the node M equals the average of nodes A and B voltages. In this case, i.e., when the voltage drop across the pseudo resistor is small, the common source voltage of both M_{p5}-M_{P8} differential pair transistors is the average of their input gate voltages. In other words, both differential pairs operate as an averaging circuit, and their common source voltages are set according to their gate voltages.

If the difference voltage of nodes A and M be large and the voltage of node M is larger than the voltage of node A, transistors M_{p5} and M_{p6} will be on and off, respectively. Thus, node A is the source of M_{p1} and this transistor has a negative gate-source voltage. Also if the voltage node A is larger than the voltage node M, transistors M_{p6} and M_{p5} will be on and off, respectively. Thus, node M is the source of M_{p1} and this transistor has a negative source-gate voltage again. Therefore, the bias circuit of this pseudo resistor has two level shifters creating the negative source-gate voltage for $M_{p1,p2}$ transistors.

In proposed total circuit, two sides of the pseudo resistor (nodes A and B) are also connected to the output of G_{m2}, and the output swing is up to 800 mV_{pp}.

Also, the gate of $M_{p3,p4}$ transistors is connected to the bias circuit of the G_{m1}. It is not possible that the voltages at the drain of transistors $M_{p3,p4}$ are set to V_{DD} because of the presence of two level shifters. Thus, the common source voltage of both differential pairs are set according to the voltage across the pseudo resistors, and transistors $M_{p3,p4}$ are always biased in the saturation region by proper usage of the pseudo resistor in the main circuit.

The total current consumption of the proposed pseudo resistor is considered 50 nA, which is appropriate for the amount of the pseudo resistor in DC servo-loop. To reduce the leakage current, the proposed pseudo resistor is designed with large channel length transistors. Also, the proposed pseudo resistor is designed with small channel width to reduce the parasitic capacitance of the transistors.

To evaluate the resistance value of the proposed pseudo resistor, one of its terminals is fixed at DC voltage and the other terminal is swept and the I-V curve is shown in Fig. 6. Also, the simulated I-V curve of the conventional pseudo resistor [12] is shown in this figure. The same size is considered in the proposed and conventional pseudo resistors. As shown in Fig. 6, the amount of proposed pseudo resistor is larger than the conventional pseudo resistor and also the proposed pseudo resistor has less variation

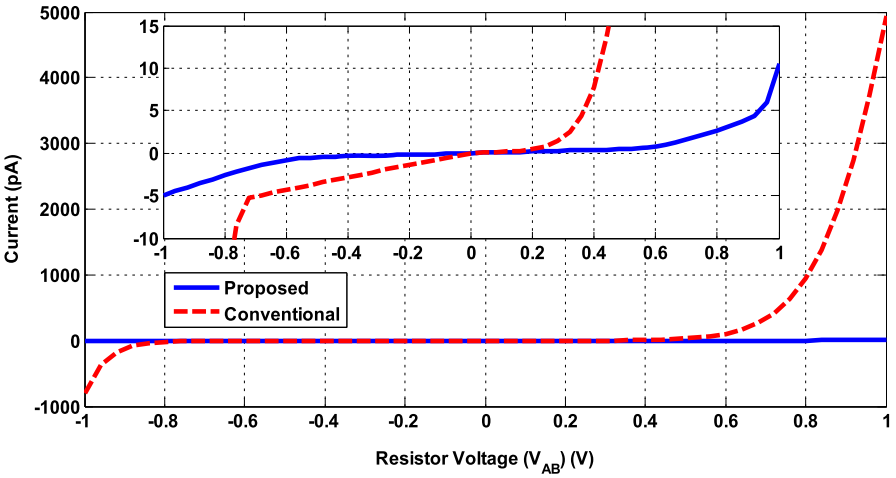

Fig. 6 Simulated I-V curve of the proposed and conventional pseudo resistors at 37 °C

to sweeping the input voltage than the conventional one. These improvements are attained since the proposed pseudo resistor is biased in the cut-off region with almost constant negative source-gate voltage for $M_{p1,p2}$ transistors and all transistors are the same type. The equivalent resistance characteristic of the proposed pseudo resistor is also almost symmetric by sweeping the input voltage. As shown in Fig. 6, the linearity of the proposed pseudo resistor is degraded when the voltage drop across its terminals is increased since in this case, one of differential pair transistors in its biasing circuit is turned off and the biasing circuit becomes a simple level shifter as explained already. Nonetheless, the linearity of the proposed pseudo resistor is still much better than the conventional pseudo resistor even in such extreme cases.

The value of the proposed pseudo resistor is simulated in different process corner cases and power supply variations, and the results are shown in Fig. 7. In these simulations, V_{DD} is 1.8 V in the typical corner, 1.6 V in SS and SF corners, and 2 V in FF and FS corners. As shown in Fig. 7, the value of the proposed pseudo resistor has less sensitivity to the process and voltage variations. The effect of temperature variations on the resistance value of the proposed pseudo resistor at 0.1 Hz is shown in Fig. 8 in the typical corner case. As it is seen, the variations of the proposed pseudo resistor at different temperatures from 0 to 85 °C are very small.

Monte Carlo simulations for resistance value of the proposed pseudo resistor at 0.1 Hz is shown in Fig. 9 considering both device mismatches and process variations. The mean value and standard deviation of resistance value for 500 runs are about 1 TΩ and 351.4 MΩ, respectively. This figure shows the amount of the proposed pseudo resistor is slightly sensitive to the device mismatches and process variations.

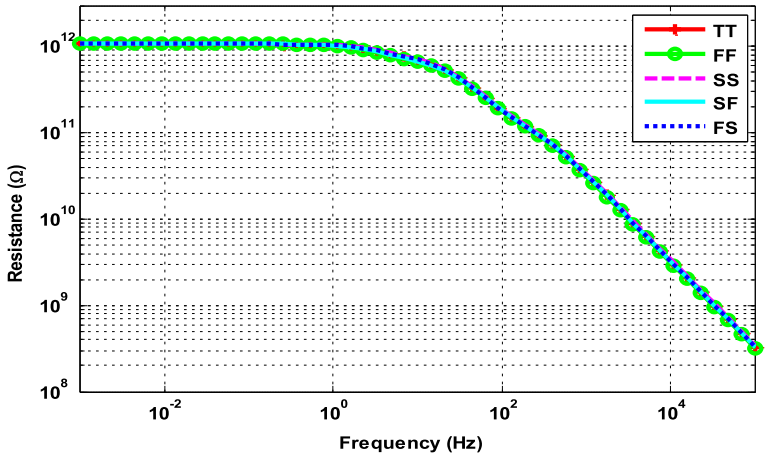

Fig. 7 Simulated resistance of the proposed pseudo resistor at 37 °C

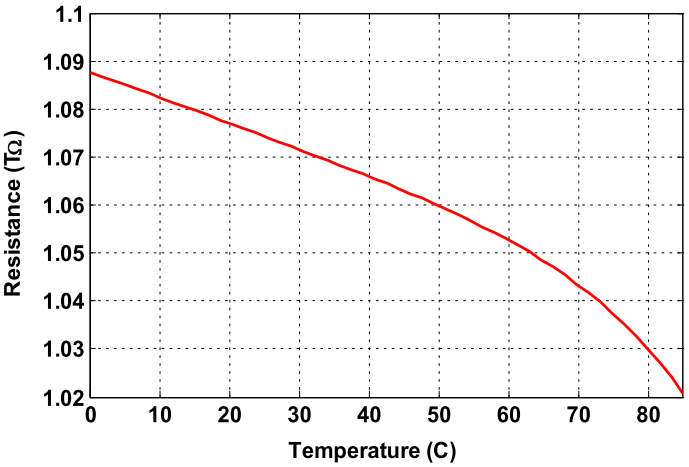

Fig. 8 Effect of temperature variations on the resistance value of the proposed pseudo resistor at 0.1 Hz

2.5 DC Servo-Loop

DC servo-loop consists of an RC integrator with a considerable time constant, chopper switches, and capacitors C_{hp}, and it is a low-pass filter in the feedback of the chopper CCIA [10]. The output of the chopper CCIA is sensed by DC servo-loop, and then it is subtracted from the input signal to provide a low cut-off frequency in the overall transfer function. Hence, the large electrode offset at low frequency is attenuated. The value of C_{hp} capacitors is obtained by:

$$V_{\mathrm{EO}} \leq \frac{V_{\mathrm{out,max}} C_{\mathrm{hp}}}{C_{\mathrm{in}}} \tag{8}$$

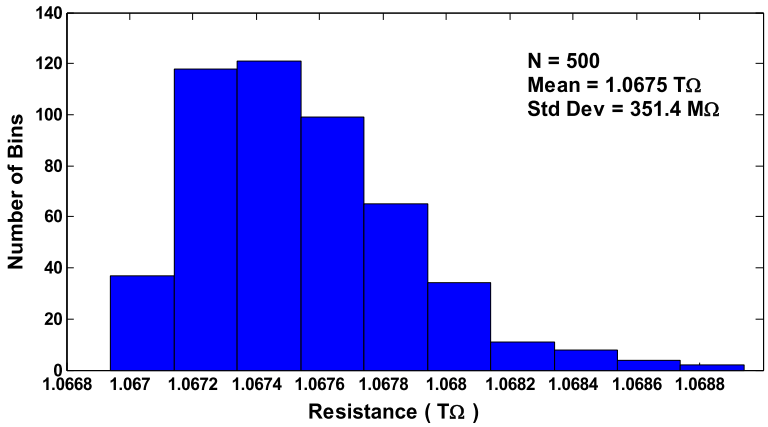

Fig. 9 Histogram diagram of Monte Carlo simulation for resistance value of the proposed pseudo resistor at 0.1 Hz

where V_{EO} is the maximum electrode offset voltage that is reduced by the DC servo-loop and $V_{\mathrm{out,max}}$ is the maximum output voltage of the DC servo-loop integrator [10, 15]. In this work, to ensure that the chopper CCIA can attenuate 50 mV electrode offset, C_{hp} is equal to 50 fF. The low cut-off frequency, f_{L}, of the DC servo-loop is defined as:

$$f_L = \frac{C_{\mathrm{in}}}{C_{\mathrm{fb}}} \times \frac{C_{\mathrm{hp}}}{C_{\mathrm{in}}} f_{\mathrm{ug}} = \frac{C_{\mathrm{hp}}}{C_{\mathrm{fb}}} f_{\mathrm{ug}} = \frac{C_{\mathrm{hp}}}{C_{\mathrm{fb}}} \times \frac{1}{2\pi R_{\mathrm{int}} C_{\mathrm{int}}} \tag{9}$$

where f_{ug} is the unity-gain frequency of the integrator in DC servo-loop, R_{int} and C_{int} are pseudo resistors and capacitors in DC servo-loop [11]. Due to the large value of the proposed pseudo resistor, the total value of integrator capacitors in DC servo-loop based on the RC integrator is decreased. Also, the large value of this pseudo resistor with a small C_{int} in DC servo-loop leads to a small low cut-off frequency. Figure 10 shows the.

G_{m3} and its CMFB circuit which are used in DC servo-loop to realize the RC integrator. A simple Miller compensated two-stage amplifier is used as G_{m3} with two separate CMFB circuits. The input transistors of the G_{m3} are biased in the sub-threshold region for low power consumption. This two-stage amplifier can provide enough gain to eliminate the large electrode offset.

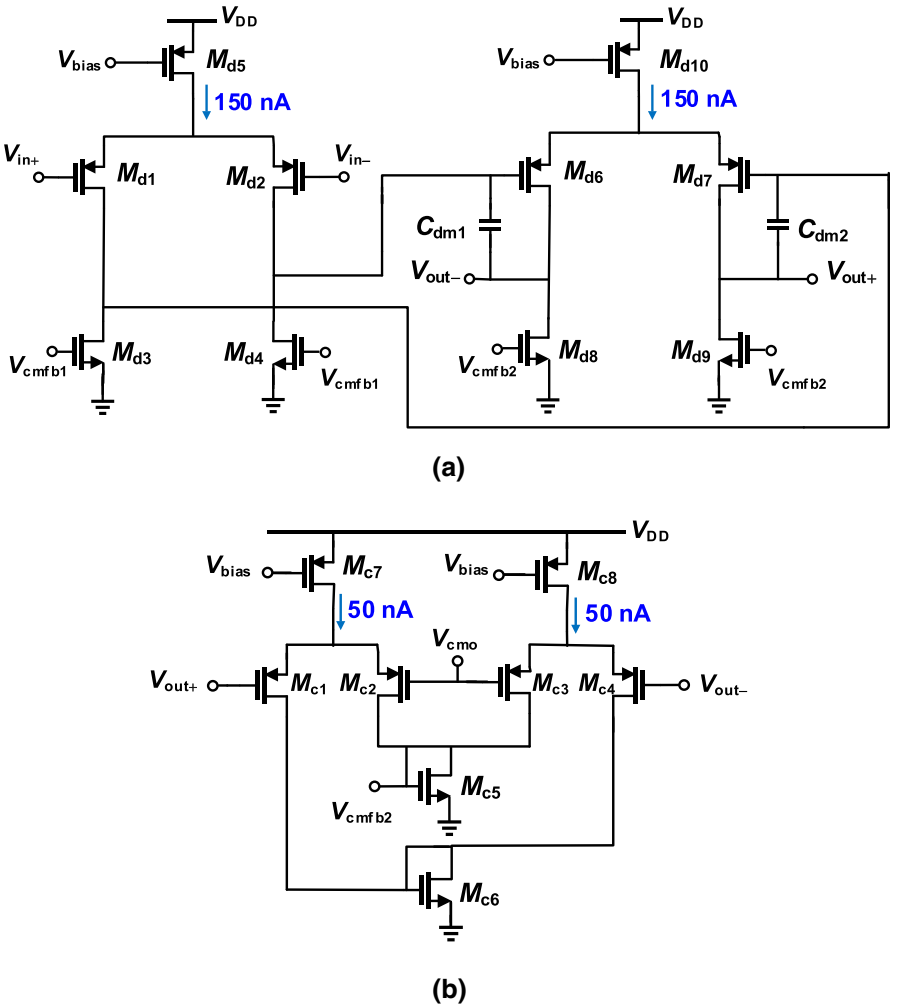

Fig. 10 Schematic of **a** the amplifier (G_{m3}) used in DC servo-loop and **b** one of its CMFB circuits

2.6 Positive Feedback Loop

In this work, as mentioned in the introduction section, the input chopper is placed before C_{in} capacitors. Thus, the value of CMRR has been increased. In this situation, the value of the differential input impedance due to the input chopper is given by:

$$Z_{in} = \frac{1}{2 f_{ch} C_{in}} \tag{10}$$

According to the relation (10), with $C_{in} = 1$ pF and $f_{ch} = 25$ kHz, the input impedance is about 20 MΩ. This value is not enough for neural recording because the input

impedance has to be larger than the electrode impedance in the frequency range of the neural signal. Also, the limited DC input impedance of the chopper CCIA creates a DC current at the electrodes. The prolonged presence of DC currents at the electrode has damaging results, and it can damage the tissue. Therefore, a method is needed to increase the input impedance. The DC servo-loop attenuates the DC signal at the output. Therefore, the positive feedback loop is disabled at low frequency. In this work, for boosting the input impedance, the positive feedback loop is used while the performance of the positive feedback loop despite the presence of DC servo-loop is improved by using the proposed high-density pseudo resistor. Hence with a small capacitor, the low cut-off frequency is decreased to 0.1 Hz and the positive feedback loop can boost the input impedance at low frequency as well. The value of the C_{pf} is determined by [10]:

$$C_{\mathrm{pf}} = \frac{C_{\mathrm{in}}}{G_{\mathrm{V}} - 1} \approx C_{\mathrm{fb}} \tag{11}$$

According to G_{V}, C_{pf} capacitors have been chosen to be equal with C_{fb}.

2.7 Ripple and Chopping Spikes Reduction

Upmodulated offset and noise of the CCIA creates the ripple at its output. To reduce the ripple, the ripple reduction loop is used in [10] where by creating a negative feedback loop, the output ripple is nulled. But it needs extra power consumption and area. In [4], a notch filter is used to reduce the ripple where attenuating the signals at the chopping frequency decreases the output ripple. But the desired signal is missed at the notch filter frequency and adds the unwanted phase delay to the desired signal. The main reason for the ripple is the offset current generated by G_{m1}. Thus, if it is blocked before flowing into G_{m2}, the output ripple can be decreased. Therefore, by using a capacitor between two stages of the chopper amplifier, the ripple at the output of the chopper CCIA is reduced [7]. Also, this capacitor isolates G_{m2} from the offset of G_{m1}.

To reduce the chopping spikes, the chopping spike filter is used in [35]. This circuit is appropriate for the LFP frequency range and should be re-designed for the AP frequency range. Also, large capacitors are used in this structure. A passive RC filter is used in [6, 8] to reducing and filtering the chopping spikes which is appropriate for both LFP and AP frequency ranges.

In this work, a pair of C_{DC} capacitors is used between the G_{m1} and G_{m2} amplifiers to reduce the ripple at the output of the chopper amplifier. Also, to reduce the chopping spikes, a passive RC filter with $R_{\mathrm{L}} = 2\ \mathrm{M}\Omega$ and $C_{\mathrm{L}} = 5$ pF is employed where R_{L} is a poly resistor and C_{L} is realized with a metal–insulator-metal (MIM) capacitor.

3 Post-Layout Simulation Results

The proposed chopper CCIA has been simulated in Cadence using TSMC 180 nm CMOS process. The pass-band closed-loop gain is considered 26 dB for avoiding the saturation of the amplifier due to the large artifacts in closed-loop neural recording.

Hence, $C_{in} = 1$ pF and $C_{fb} = 50$ fF are considered. The -3 dB bandwidth for neural recording should be 0.1–5 kHz. The input-referred noise of the chopper amplifier in the LFP band should be about 1–3 μV_{rms}, and in the AP band, it should be about 3–5 μV_{rms}. The power consumption should be less than 5 μW per channel to avoid tissue damage. In closed-loop neural recording, a large common-mode signal with about 500 mV_p is appeared at the input, and hence, the first-stage amplifier must tolerate this large common-mode artifact. The required THD for neural recording is about $-$ 70 dB.

The simulated device parameters including the aspect ratio (W/L) of transistors and the value of passive elements are summarized in Table 1. The layout view of the proposed chopper CCIA is shown in Fig. 11. The active area of the simulated chopper CCIA is 0.072 mm^2 and all of the capacitors are on-chip and realized by MIM capacitors. The simulated closed-loop chopper amplifier consumes about 2.02 μA from a 1.8 V power supply.

In all simulations, V_{DD} is 1.8 V in the typical corner, 2 V in FF and FS corners, and 1.6 V in SS and SF corners by considering the equivalent circuit of dry electrode. As shown in Fig. 12, the simulated pass-band closed-loop gain in the typical corner case is

Table 1 Simulated design parameters

Device	($M \times W/L$)	Device	($M \times W/L$) or Value
$M_{1\text{-}2}$, $M_{1a\text{-}2a}$	10 × 5 μm/1 μm	M_{b32}	1 × 2 μm/10 μm
$M_{3\text{-}4}$	1 × 18.7 μm/10 μm	M_{b33}	1 × 0.75 μm/10 μm
$M_{3a\text{-}6a}$	1 × 7 μm/10 μm	M_{b34}	1 × 1 μm/10 μm
$M_{5\text{-}6}$	1 × 0.22 μm/20 μm	$M_{b35\text{-}b46}$	1 × 0.22 μm/20 μm
$M_{7\text{-}8}$	1 × 1 μm/20 μm	$M_{c1\text{-}c4}$	1 × 4 μm/1 μm
$M_{9\text{-}10}$	1 × 0.22 μm/20 μm	$M_{c5\text{-}c6}$	1 × 0.26 μm/15 μm
$M_{11\text{-}12}$	1 × 0.275 μm/20 μm	$M_{c7\text{-}c8}$	1 × 1 μm/10 μm
M_{13}	1 × 11.6 μm/15 μm	$M_{p1\text{-}p2}$	1 × 0.22 μm/20 μm
$M_{14\text{-}15}$	10 × 4 μm/1 μm	$M_{p3\text{-}p4}$	1 × 0.5 μm/10 μm
$M_{16\text{-}17}$	1 × 0.23 μm / 15 μm	$M_{p5\text{-}p8}$	1 × 0.25 μm/10 μm
M_{18}	1 × 0.66 μm/10 μm	M_{ns}	1 × 0.22 μm/0.18 μm
$M_{d1\text{-}d2}$, $M_{d6\text{-}d7}$	1 × 15 μm/1 μm	M_{ps}	1 × 0.88 μm/0.18 μm
$M_{d3\text{-}d4}$, $M_{d8\text{-}d9}$	1 × 0.25 μm/10 μm	C_{int}	820 fF
M_{d5}, M_{d10}	1 × 3 μm/10 μm	C_{hp}, C_{fb}, C_{pf}	50 fF
M_{b1}	1 × 2 μm/10 μm	C_{in}	1 pF
M_{b2}	1 × 0.25 μm/10 μm	C_{DC}	6 pF
M_{b3}	1 × 0.3 μm/10 μm	C_m	4 pF
$M_{b4\text{-}b15}$, $M_{b18\text{-}b19}$, $M_{b22\text{-}b23}$	1 × 0.22 μm/20 μm	C_{dm}, C_L	5 pF
$M_{b16\text{-}b17}$	1 × 0.27 μm/15 μm	R_m	1.5 MΩ
$M_{b20\text{-}b21}$	1 × 0.26 μm/20 μm	R_L	2 MΩ
$M_{b24\text{-}b31}$	1 × 0.24 μm/20 μm		

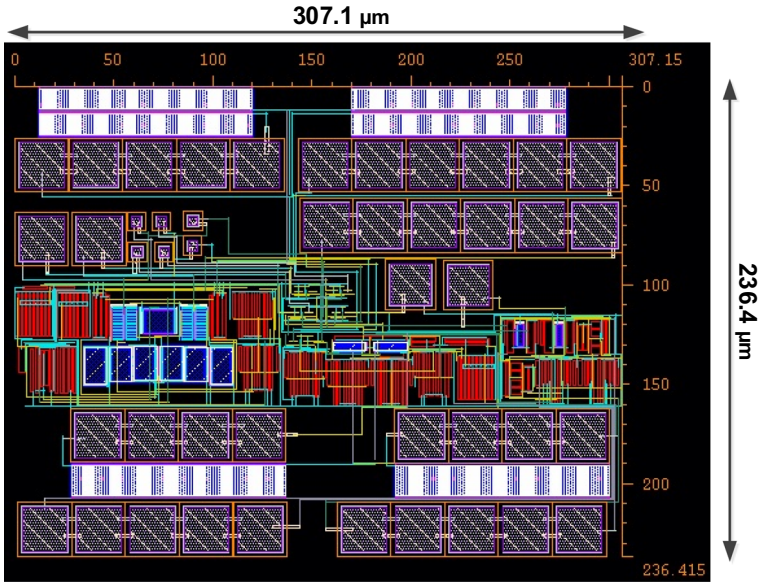

Fig. 11 Layout of the proposed chopper CCIA

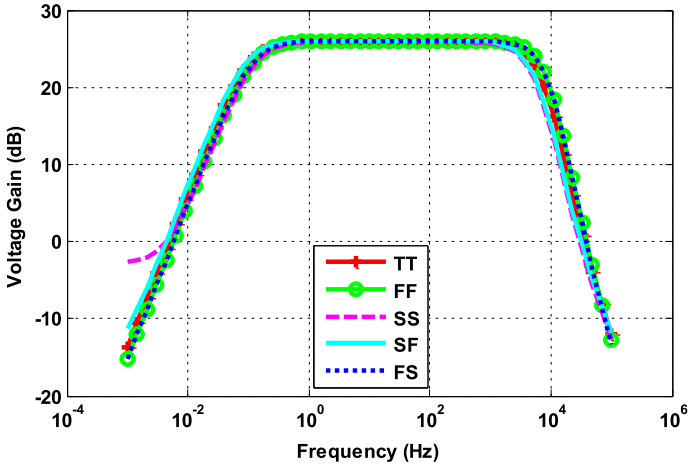

Fig. 12 Simulated frequency response of the proposed neural amplifier at 37 °C

26.04 dB with a -3 dB bandwidth of 0.1 Hz–5.1 kHz, which is appropriate for recording both LFP and AP signals. Due to low sensitivity of the proposed pseudo resistor to various process corners and supply voltage variations, the low cut-off frequency has small variations in different voltage and process corner cases.

The simulated frequency response of the proposed chopper CCIA with different pseudo resistors is shown in Fig. 13. As it is seen, the frequency response of CCIA

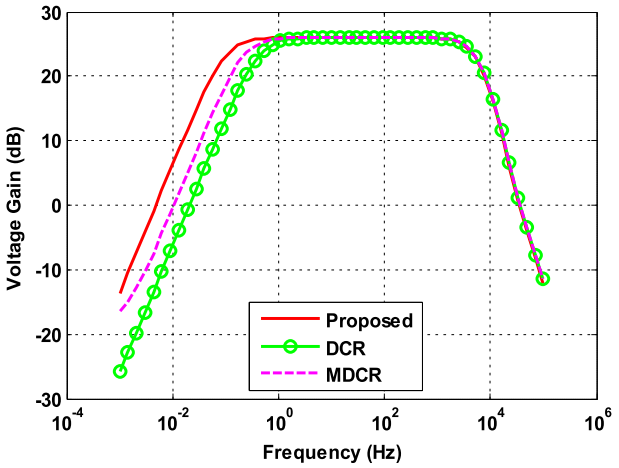

Fig. 13 Simulated frequency response of the proposed neural amplifier at 37 °C with different pseudo resistors and capacitors size

with the proposed pseudo resistor has a 0.1 Hz low cut-off frequency with 1.64 pF total integrator capacitors in DC servo-loop. Hence, the value of the proposed pseudo resistor is about 1 TΩ. Also, the THD of the chopper CCIA using the proposed pseudo resistor is about −71.94 dB. By using DCR and MDCR, with 1/40000 duty cycle factor and 1 MΩ poly resistor, the low cut-off frequency is 0.4 Hz and 0.2 Hz with 50 pF total integrator capacitors in DC servo-loop, respectively. Also, the THD of chopper CCIA using these pseudo resistors is −77.93 dB and −77.97 dB, respectively. In these simulations, the pseudo resistors are used in the proposed chopper CCIA, and the value of pseudo resistors are measured by using the PSS and PAC simulations. For calculating the THD of the presented chopper CCIA with three pseudo resistors, an input tone with 40 mV_{pp} at 1 kHz has been used. The achieved THD using the proposed pseudo resistor is worse than DCR and MDCR. However, by using the proposed pseudo resistor, the low cut-off frequency and capacitor value in DC servo-loop (DSL) is far less than when using the DCR and MDCR. Thus, by using the proposed pseudo resistor with smaller low cut-off frequency, the positive feedback loop (PFL) can operate better than the previous works. Actually, the advantages of the proposed pseudo resistor with some linearity degradation compared to the previously reported pseudo resistors are large amount of pseudo resistor, improvement the performance of PFL, and reduction of capacitors value in DSL which results in smaller chip area. The area of the proposed pseudo resistor is 532.6μm^2.

The simulated input-referred noise in various process corners and supply voltage variations at body temperature is shown in Fig. 14 using the PNOISE analysis in Cadence. The total input-referred noise of the chopper CCIA for the LFP and AP bands are 0.63 μV_{rms} and 2.86 μV_{rms}, respectively.

The simulated input impedance of the chopper CCIA is shown in Fig. 15 in process variations at 37 °C. According to Fig. 15, in this paper, the positive feedback loop operates better than [10, 15, 18] at low frequencies despite the presence of DC servo-loop.

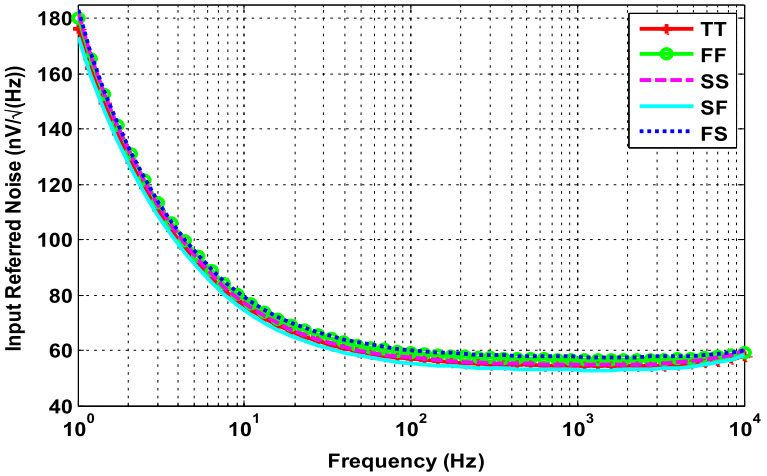

Fig. 14 Simulated total input-referred noise of the chopper CCIA at 37 °C

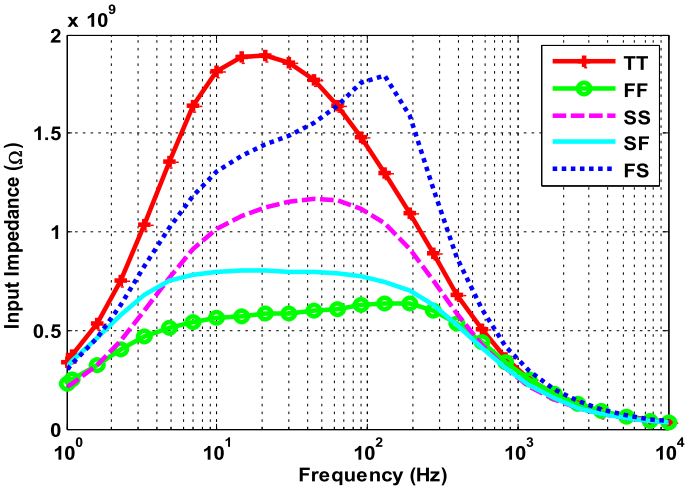

Fig. 15 Simulated input impedance of the chopper CCIA at 37 °C

The input impedance of the proposed chopper CCIA without the positive feedback loop is about 38 MΩ at 10 Hz. The input impedance of the proposed chopper CCIA is 342 MΩ and 1.8 GΩ at 1 Hz and 10 Hz, respectively. By reducing the amount of C_{int} and increasing the low cut-off frequency from 0.1 to 0.4 Hz, the input impedance of the proposed chopper CCIA is 80 MΩ and 820 MΩ at 1 Hz and 10 Hz, respectively.

As shown in Fig. 16, the simulated THD of the proposed CCIA is about −71.94 dB, where an input tone with 40 mV_{pp} at 1 kHz is applied. The THD is dominated by the core two-stage OTA in the frequency band of 200 Hz–5 kHz, while the DSL dominates it at the frequency band from near dc to 200 Hz [15]. Since DSL operates at low

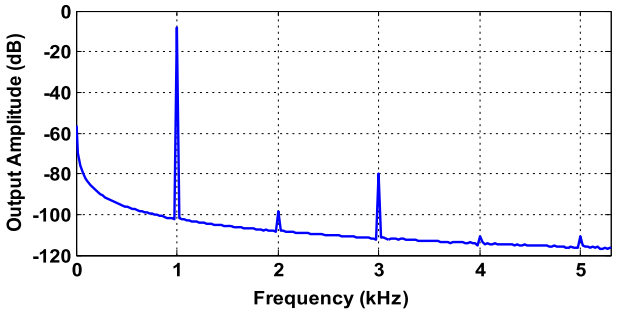

Fig. 16 Total harmonic distortion of the chopper CCIA for a 1 kHz 40 mV_{pp} input at 37 °C

frequencies to decrease the electrode offset and this is the main reason why the value of THD is mostly limited by DSL at low frequencies. The THD result shown in Fig. 16 is simulated at 1 kHz input signal frequency where the THD is dominated by the core two-stage OTA. Almost all previous papers that are related to the recording of LFP and AP signals have selected 1 kHz input signal frequency to calculate the value of THD. This is the main reason that we have also selected 1 kHz input signal frequency to report THD in order to provide a fair comparison with related works.

The node B of the proposed pseudo resistor will be driving large swings due to incoming the chopping signal at the output. The linearity of the proposed pseudo resistor could be changed with high voltage swing according to Fig. 6, and hence, the linearity of the pseudo resistor in DSL mostly affects on THD of the total circuit from dc to 200 Hz. Nonetheless, the performance of the proposed pseudo resistor with a higher voltage swing is much better than the conventional pseudo resistor, even in extreme cases, according to Fig. 6.

As another simulation, two differential input tones with 1 mV_p at 1 kHz as the desired neural signal and 20 mV_p at 750 Hz as the differential stimulation artifact are applied. Besides, a large common-mode input with 520 mV_p at 750 Hz is applied. As shown in Fig. 17, the intermodulation terms are small and the proposed chopper CCIA can tolerate large differential and common-mode artifacts while amplifying the desired small neural signal such as LFP and AP signals.

The simulated step response of the proposed chopper amplifier is shown in Fig. 18. As it is seen, there is no overshoot, which indicates the proper stability of the closed-loop chopper amplifier. The ripples in the step response are due to the chopping mechanism, and they are attenuated by the low-pass filter after the chopper amplifier.

Histogram diagram of Monte Carlo simulations for CMRR is shown in Fig. 19 considering the device mismatches and process variations. The mean value and standard deviation of CMRR are 104.3 dB and 4.5 dB, respectively, for 500 runs at the frequency of 50 Hz.

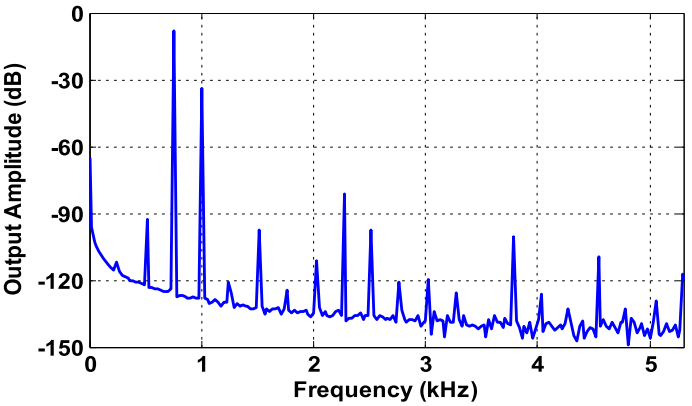

Fig. 17 Two-tone test for differential inputs of 1 mV_{p} at 1 kHz and 40 mV_{pp} at 750 Hz with a large common-mode input of 1040 mV_{pp} at 750 Hz

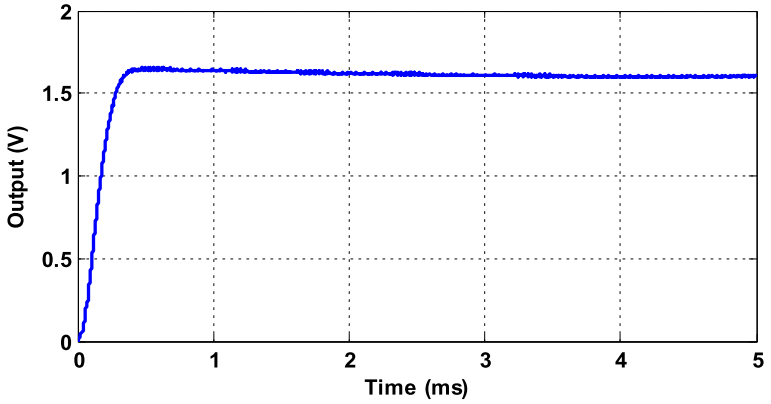

Fig. 18 Simulated step response of the closed-loop neural amplifier

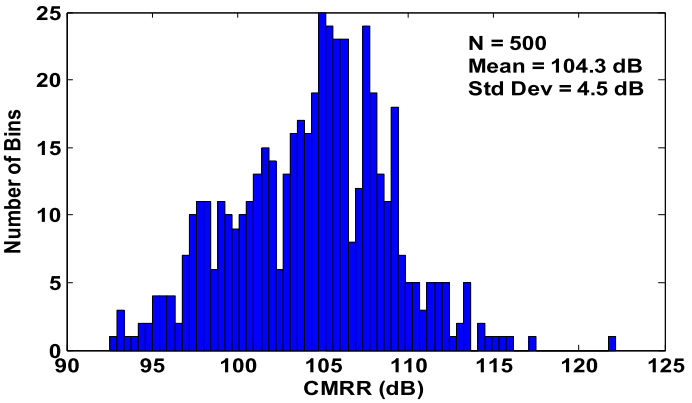

Fig. 19 Histogram diagram of Monte Carlo simulation for CMRR at 50 Hz input signal

Table 2 Simulation results of the proposed chopper CCIA in various process corners and supply voltage variations at 37 °C

Process Corner	TT	SS	SF	FF	FS
Mid-band Gain (dB)	26.04	25.93	26.03	26.05	26.05
Bandwidth (Hz)	0.1–5.1 k	0.1–4 k	0.1–4.1 k	0.1–6.4 k	0.1–6.5 k
Total Current (μA)	2.02	1.98	2.09	2.03	1.96
Input-referred Noise (μV_{rms})	LFP: 0.63	LFP: 0.64	LFP: 0.62	LFP: 0.66	LFP: 0.67
	AP: 2.86	AP: 2.88	AP: 2.75	AP: 2.96	AP: 2.96
Input Impedance at 10 Hz	1.8 GΩ	1 GΩ	798 MΩ	562 MΩ	1.3 GΩ
NEF	LFP: 2.5	LFP: 2.5	LFP: 2.5	LFP: 2.6	LFP: 2.6
	AP: 2.3	AP: 2.3	AP: 2.3	AP: 2.4	AP: 2.4
V_{DD} (V)	1.8	1.6		2	

The noise efficiency factor (NEF) is used for comparing the neural recording amplifiers, which is given by [12]:

$$\mathrm{NEF} = V_{\mathrm{ni,rms}}\sqrt{\frac{2I_{\mathrm{tot}}}{4\pi V_{\mathrm{T}} k \mathrm{TBW}}} \tag{12}$$

where $V_{\mathrm{ni,rms}}$ is the input-referred root mean square (RMS) noise voltage, BW is the amplifier bandwidth, and I_{tot} is the total supply current. NEF shows a trade-off between power and input-referred noise. The other figure of merit is the power efficiency factor (PEF), which is given by [20]:

$$PEF = V_{DD}.NEF^2 \tag{13}$$

PEF shows a trade-off between power and input-referred noise by considering the power supply voltage, V_{DD}. Smaller values of NEF and PEF mean that the CCIA is designed more appropriately.

Most of the power consumption is related to the CCIA due to reducing the input-referred noise and increasing the g_m of the input transistors. The simulation results of the chopper CCIA in various process corners and power supply variations are summarized in Table 2.

The summary of the simulated results of the proposed CCIA and several related designs are illustrated in Table 3. The achieved performance of the proposed neural amplifier is comparable with the best-reported designs in current literature. As shown in Table 3, this work can tolerate large differential and common-mode artifacts while amplifying small LFP and AP signals. Due to the small current consumption of recycling folded-cascode amplifier in G_{m1} than the conventional folded-cascode amplifier, NEF is decreased. By using the proposed pseudo resistor, the amount of total capacitors in DC servo-loop is reduced and this makes the realization of the small low cut-off frequency. Therefore, the positive feedback loop can operate at low frequency as well.

Table 3 Simulation results of the proposed CCIA and comparison with the current state-of-the-art works

Parameter	[18] JSCC'15	[31] TCAS'15	[6] JSCC'17	[8] JSCC'17	[20] AEUE'18	[16] ISCAS'18	[21] ISCAS'19	[15] JSCC'19	[13] TCAS'20	This work
Process (nm)	65	180	40	40	180	180	180	180	180	180
Supply Voltage (V)	0.5	1.25	1.2	1.2	1	1.8	1	1.8	1.2	1.8
Total Current (μA)	4.6	1.7	1.66	2.33	0.963	1.9	1.89	1.8	2	2.02
Signals	LFP	LFP + AP	LFP + AP	LFP + AP	LFP	LFP + AP	ECoG	LFP + AP	-	LFP + AP
Mid-band Gain (dB)	–	32	26	25.7	62–74	26	40	40	40	26.04
Bandwidth (Hz)	1–500	0.5–10 k	0.2–5 k	0.12–5 k	235	–	0.4–500	0.3–5.4 k	0.5–500	0.1–5.1 k
Input-Referred Noise (μV_{rms})	1.3 (1–500)	5.7	LFP: 2 AP: 7	LFP:1.8 AP: 5.3	1.33	LFP: 1.12 AP: 4.56	0.75 (1–200)	LFP: 0.65 AP: 2.14	1.8 (0.5–500)	LFP: 0.63 AP: 2.86
NEF	4.76	2.9	LFP: 7 AP: 4.9	LFP: 7.4 AP: 4.4	3.34	LFP: 4.19 AP: 3.56	2.77	LFP: 2.37 AP: 1.56	4.4	LFP: 2.5 AP: 2.3

Table 3 (continued)

Parameter	[18] JSCC'15	[31] TCAS'15	[6] JSCC'17	[8] JSCC'17	[20] AEUE'18	[16] ISCAS'18	[21] ISCAS'19	[15] JSCC'19	[13] TCAS'20	This work
PEF	11.3	10.51	LFP: 58.8	LFP: 65.71	9.06	LFP: 31.6	7.7	LFP: 10.11	23.23	LFP: 11.25
			AP: 28.81	AP: 23.23		AP: 22.8		AP: 4.38		AP: 9.52
Input Impedance	28 MΩ	N/A	300 MΩ	1.6GΩ	10 GΩ at 10 Hz	90 MΩ	100 MΩ	440 MΩ at 50 Hz	1 GΩ at 50 Hz	1.8 GΩ at 10 Hz
Tolerance to Large CM Signal	No	No	No	650 mVpp	No	1040 mVpp	No	No	Yes*	1040 mVpp
Electrode Offset Removal	–	RC Integrator DSL	RC Integrator DSL	RC Integrator DSL	Adaptive DSL	Gm-C DSL	Gm-C DSL	Gm-C DSL	RC Integrator DSL	RC Integrator DSL
Total Integrator Capacitors	–	30 pF	20 pF	24 pF	60 pF	80 pF	–	80 pF	48 pF	1.64 pF
Area/Ch. (mm^2)	0.025	0.23	0.071	0.069	3.09	0.219	0.14	0.2	0.46	0.072
DR (dB)	–	–	LFP: 78	LFP: 81	–	LFP: 82.02	–	–	–	LFP: 87.43
			AP: 69	AP: 74		AP: 69.83				AP: 74.65
THD (dB)	−48 (1 mV_{pp})	–	−74 (40 mV_{pp} at 1 kHz)	−76 (80 mV_{pp} at 1 kHz)	−41.27 (200 μV_{pp} at 20 Hz)	−72 (40 mV_{pp} at 1 kHz)	−46.02 (1 mV_{pp})	−63 (5 mV_{pp} at 1 kHz)	−80 (16 mV_{pp} at 69 Hz)	−71.94 (40 mV_{pp} at 1 kHz)
Post Sim./Meas	Meas	Meas	Meas	Meas	Post Sim	Meas	Post Sim	Meas	Meas	Post Sim

*The amplitude of the large common-mode signal that the chopper CCIA can tolerate is not mentioned

4 Conclusion

This work presents a chopper CCIA which can be used in closed-loop neural recording. This chopper CCIA can record LFP and AP signals in the presence of large differential and common-mode stimulation artifacts. The proposed pseudo resistor in DC servo-loop has made the small low cut-off frequency with small capacitors in the integrator. Hence, the amount of total required capacitors in chopper CCIA is decreased. The small low cut-off frequency makes the positive feedback loop to operate better than the other previous works that use both the positive feedback loop and DC servo-loop. This also boosts the low-frequency input impedance despite the presence of DC servo-loop in chopper CCIA. A two-stage Miller compensated amplifier with inherent CMFB circuits is used to realize the required stages. A recycling folded-cascode amplifier with an inherent CMFB circuit is used as the first stage. The current consumption of this structure is smaller than the conventional folded-cascode, and hence, NEF is decreased. Also, the first stage can tolerate large input common-mode variations without any extra circuit. In addition to improving these characteristics, the proposed chopper CCIA has appropriate noise and power consumption compared to the current state-of-the-art designs.

Data Availability Statement This manuscript has no associated data.

References

1. S. Barati, M. Yavari, An automatic action potential detector for neural recording implants. Circuits Systems Signal Process. **38**(5), 1923–1941 (2019)
2. S. Barati, M. Yavari, An adaptive continuous-time incremental $\Sigma\Delta$ ADC for neural recording implants. Int. J. Circuit Theory Appl. **47**(2), 187–203 (2019)
3. S. Basir-Kazeruni, S. Vlaski, H. Salami, A. H. Sayed, and D. Marković, A blind adaptive stimulation artifact rejection (ASAR) engine for closed-loop implantable neuromodulation systems. In: *8th Int. IEEE/EMBS Conference on Neural Engineering (NER)*, pp. 186–189 (2017)
4. R. Burt, J. Zhang, A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path. IEEE J. Solid State Circuits **41**(12), 2729–2736 (2006)
5. H. Chandrakumar, D. Marković, A 15.2-ENOB 5-kHz BW 4.5 μW chopped CT $\Sigma\Delta$-ADC for artifact-tolerant neural recording front ends. IEEE J. of Solid-State Circuits **53**(12), 3470–3483 (2018)
6. H. Chandrakumar, D. Marković, A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation. IEEE J. Solid-State Circuits **52**(3), 645–656 (2017)
7. H. Chandrakumar, D. Marković, A simple area-efficient ripple-rejection technique for chopped biosignal amplifiers. IEEE Trans. Circuits Syst. II Express Briefs **62**(2), 189–193 (2015)
8. H. Chandrakumar, D. Marković, An 80-mVpp linear-input range, 1.6 GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that Is tolerant to 650-mVpp common-mode interference. IEEE J. Solid-State Circuits **52**(11), 2811–2828 (2017)
9. C. Enz, G.C. Temes, Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization. Proc. IEEE **84**(11), 1584–1614 (1996)
10. Q. Fan et al., A 1.8 μW 60 nV/$\sqrt{}$Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes. IEEE J. Solid-State Circuits **46**(7), 1534–1543 (2011)
11. Q. Fan, F. Sebastianen, H. Huijsing, and K. Makinwa, A 2.1 μW area-efficient capacitively-coupled chopper instrumentation amplifier for ECG applications in 65 nm CMOS. In: *IEEE Asian Solid-State Circuits Conference*, pp. 1–4, (2010)
12. R.R. Harrison, C. Charles, A low-power low-noise CMOS amplifier For neural recording applications. IEEE J. Solid-State Circuits **38**(6), 958–965 (2003)

13. Q. Li, X. Wang, Y. Liu, A 60 nV/$\sqrt{}$ Hz < 0.01%-THD ±200 mV-DC-rejection bio-sensing chopper amplifier with noise-nonlinearity-cancelling loop. IEEE Trans. Circuits Syst. II Express Briefs **67**(2), 215–219 (2020)
14. D. Luo, J. Lei, M. Zhang, Z. Wang, Design of a low noise bio-potential recorder with high tolerance to power-Line interference under 0.8 V Power supply. IEEE Trans. Biomed. Circuits Syst. **14**(6), 1421–1430 (2020)
15. D. Luo, M. Zhang, Z. Wang, A low-noise chopper amplifier designed for multi-channel neural signal acquisition. IEEE J. Solid-State Circuits **54**(8), 2255–2265 (2019)
16. D. Luo, M. Zhang, and Z. Wang, Design of a low noise neural recording amplifier for closed-loop neuromodulation applications. In: *IEEE Internlational Symposium on Circuits and Systems (ISCAS)*, pp. 1–4 (2018)
17. C. Menolfi, Q. Huang, A low-noise CMOS instrumentation amplifier for thermoelectric infrared detectors. IEEE J. Solid-State Circuits **32**(7), 968–976 (1997)
18. R. Muller et al., A minimally invasive 64-channel wireless μECoG implant. IEEE J. Solid-State Circuits **50**(1), 344–359 (2015)
19. R. Nagulapalli, K. Hayatleh, S. Barker, P. Georgiou, F. Lidgey, A high value, linear and tunable CMOS pseudo-resistor for biomedical applications. J. Circuits Syst. Comput. **28**(6), 1950096 (2019)
20. M. Nasserian, A. Peiravi, F. Moradi, A fully-integrated 16-channel EEG readout front-end for neural recording applications. AEU-Int. J. Electron. Commun. **94**, 109–121 (2018)
21. N. Perez-Prieto, J. L. Valtierra, M. Delgado-Restituto, and A. Rodriguez-Vazquez, A sub-μV rms chopper front-end for ECoG recording. In: *IEEE International Symposium on Circuits and Systems* (ISCAS), pp. 1–5 (2019)
22. R. Puddu et al., A precision pseudo resistor bias scheme for the design of very large time constant filters. IEEE Trans. Circuits Syst. II Express Briefs **64**(7), 762–766 (2017)
23. C. Qian, J. Parramon, E. Sanchez-Sinencio, A micropower low-noise neural recording front-end circuit for epileptic seizure detection. IEEE J. Solid-State Circuits **46**(6), 1392–1405 (2011)
24. B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd edn. (McGraw-Hill, New York, 2017)
25. S.U. Rehman, A.M. Kamboh, A CMOS micro-power and area efficient neural recording and stimulation front-end for biomedical applications. Circuits Systems Signal Process. **34**(6), 1725–1746 (2015)
26. H. Rezaee-Dehsorkh et al., Analysis and design of tunable amplifiers for implantable neural recording applications. IEEE Journal on Emerging and Selected Topics in Circuits and Systems **1**(4), 546–556 (2011)
27. A. Samiei, H. Hashemi, A chopper-stabilized, current feedback, neural recording amplifier. IEEE Solid-State Circuits Letters **2**(3), 17–20 (2019)
28. A. Tajalli, Y. Leblebici, E.J. Brauer, Implementing ultra-high-value floating tunable CMOS resistors. Electron. Lett. **44**(5), 349–350 (2008)
29. N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, A.P. Chandrakasan, A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system. IEEE J. Solid-State Circuits **45**(4), 804–816 (2010)
30. C.-Y. Wu, C.-H. Cheng, Z.-X. Chen, A 16-channel CMOS chopper-stabilized analog front-end ECoG acquisition circuit for a closed-loop epileptic seizure control system. IEEE Trans. Biomed. Circuits Syst. **12**(3), 543–553 (2018)
31. J. Wu, M.-K. Law, P.-I. Mak, R.P. Martins, A 2 μW 45 nV/$\sqrt{}$ Hz readout front end with multiple-chopping active-high-pass ripple reduction loop and pseudofeedback DC servo loop. IEEE Trans. Circuits Syst. II Express Briefs **63**(4), 351–355 (2015)
32. J. Xu, Q. Fan, J.H. Huijsing, C. Van Hoof, R.F. Yazicioglu, K.A. Makinwa, Measurement and analysis of current noise in chopper amplifiers. IEEE J. Solid-State Circuits **48**(7), 1575–1584 (2013)
33. J. Xu, S. Mitra, C. Van Hoof, R.F. Yazicioglu, K.A. Makinwa, Active electrodes for wearable EEG acquisition: Review and electronics design methodology. IEEE Rev. Biomed. Eng. **10**, 187–198 (2017)
34. M. Yavari, T. Moosazadeh, A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits. Analog Integr. Circ. Sig. Process **79**(3), 589–598 (2014)
35. R.F. Yazicioglu, P. Merken, R. Puers, C. Van Hoof, A 200 μW eight-channel EEG acquisition ASIC for ambulatory EEG systems. IEEE J. Solid-State Circuits **43**(12), 3025–3038 (2008)