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MIXED SIGNAL LETTER

A three-stage NMC operational amplifier with enhanced slew rate for switched-capacitor circuits

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Abstract

This paper presents a new architecture for three-stage operational transconductance amplifiers (OTAs) with a class AB input stage to improve the slew rate. The nested Miller compensation scheme is utilized to stabilize the proposed OTA. A nonlinear current mirror in the first-stage is used to implement the class AB operation. Details of the proposed OTA are described and the circuit level simulation results are provided using HSPICE and a 90 nm CMOS technology to verify the usefulness of the proposed OTA. In comparison with the conventional class A OTA, it achieves 284.1% enhancement in the slew rate and the settling time is reduced from 15.7 ns to 9.1 ns with approximately the same power dissipation.

Keywords CMOS operational transconductance amplifiers (OTAs) · Nested Miller compensation · Switched-capacitor circuits · Fast settling · Slew rate · Three-stage OTAs

1 Introduction

The operational transconductance amplifier (OTA) is one of the most utilized building blocks in analog and mixed-signal integrated circuits. For high accuracy data converters and switched-capacitor circuits, high speed and high dc gain OTAs are required to settle with specific accuracy in a specified limited time. On the other hand, by reducing the feature size of the technology, the design of high dc gain OTAs becomes more complex and difficult due to the reduction in the transistor's inherent dc gain and power supply voltage. Hence to obtain both high dc gain and large output swing, cascading of several gain stages are utilized [1]. However, for closed-loop stability condition, complex frequency compensation schemes are needed in multi-stage amplifiers. Various compensation methods including the most popular nested Miller compensation (NMC) and reversed nested Miller compensation (RNMC) schemes have been presented in literature [2].

Several variants of the basic NMC and RNMC methods have been proposed in [3–11]. In the majority of these methods, the load capacitor of the OTA is large and the required gain bandwidth is small and the settling time is not a critical issue in their design consideration. On the other hand, in high accuracy and high speed switched-capacitor circuits, the load capacitor of the OTA is small and it is important that the output of the OTA to be settled with a specific settling accuracy at the desired limited time [12–15]. As a result, the settling time is one of the most vital parameters of OTAs which are used in the switched-capacitor circuits.

Settling time consists of two parts. The first one is the linear settling time which depends on the gain bandwidth of the OTA, and the second one is the nonlinear settling time which is limited by the slew rate of the OTA [16]. So the nonlinear settling time has a significant impact on the OTA settling performance. Therefore, the slew rate of the OTA should be large enough to ensure fast settling. On the other hand, the slew rate depends on the bias current of the amplifier stages. So, in a conventional three-stage class A OTA, to improve the slew rate, the bias current of the amplifier stages must be increased which also increases the static power dissipation. Therefore it is necessary to provide large slew rate without any additional power dissipation.

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Recently several schemes have been reported to improve the slew rate for single-stage, two-stage, and three-stage OTAs [16–21]. In [16], a positive feedback network is utilized to improve both the amplifier's large-signal and small-signal parameters significantly. In [17], two different three-stage OTAs with NMC and damping factor control frequency compensation (DFCFC) compensation schemes have been realized and it is shown that the DFCFC compensation scheme is more suitable to realize fast-settling three-stage OTAs**.** In [18], a new structure is proposed to improve the slew rate in three-stage OTAs with RNMC compensation. Though this method does not require any additional power dissipation but the utilized class AB structure in the last stage does not have a significant effect on the slew rate, because the major of the slew rate limitation is due to the lowest bias current in the first stage and the two additional capacitors used in this structure increase the die area. In [19], flipped voltage follower (FVF) cells are utilized to realize the class AB structure. The main concern in FVF cells is the common-mode rejection ratio (CMRR) degradation. This is because of the output resistance of the tail current-source is very low. In [20], adaptive biasing and local common-mode feedback (LCMFB) schemes are used to realize a super class AB structure which improves the slew rate without any additional power consumption. Nonetheless, the adaptive biasing is realized by FVF cells and the LCMFB includes two resistors which increases the die area. In [21], an architecture for sub-1 V bulk-driven OTAs has been presented which exploits an NMC three-stage topology and a class AB output stage to improve DC gain and driving capability, respectively. But this structure is not very useful for switched-capacitor circuits due to its limited slew rate and settling performance.

In this paper, a new architecture is presented to enhance the slew rate of three-stage OTAs with NMC compensation for switched-capacitor circuits. The proposed architecture enhances the slew rate by using a nonlinear current mirror in the first stage to realize the class AB input stage with no additional bias branches or voltages. The rest of the paper is organized as follows. In Sect. 2, the large signal analysis and slew rate of a three-stage class A OTA with NMC compensation are briefly reviewed. In Sect. 3, the proposed three-stage class AB OTA is described. The circuit-level simulation results of the proposed OTA are provided in Sect. 4, and finally, Sect. 5 concludes the paper.

2 Large signal analysis of three-stage class A NMC OTA

Figure 1(a) shows a typical fully-differential circuit implementation of a three-stage class A OTA with NMC compensation. The first-, second- and the third-stage comprises of an pMOS, pMOS, and nMOS input pairs with active loads, respectively. To define the output common-mode voltage of the OTA stages, as shown in Fig. 1(b), two independent switched-capacitor common-mode feedback (CMFB) circuits are used. The first one is used to define the output common-mode voltage of the first stage and the second one defines the output common-mode voltage of both the second and the third stages at the same CMFB loop. The NMC compensation for this OTA is performed by C_{m1} and C_{m2} capacitors as illustrated in Fig. 1(a) to ensure the OTA closed-loop stability.

When a large input signal is applied to the OTA, it enters to the slewing regime where the output of the OTA changes with a constant rate which is called the slew rate. The differential slew rate at the output of the OTA stages shown in Fig. 1(a) is obtained as follows [18]:

$$SR_1 = \frac{I_{D5}}{C_{m1}}, \quad SR_2 = \frac{I_{D10}}{C_{m2}}, \quad SR_3 = \frac{2I_{D13} - I_{D5} - I_{D10}}{C_L} \tag{1}$$

where I_{D5}, I_{D10}, and I_{D13} are the bias currents of M_5, M_{10}, and M_{13} transistors, respectively, and C_L is the total load capacitance. The overall slew rate of the OTA is defined by the minimum of the above mentioned slew rates. In a three-stage OTA with NMC compensation that derives a small load capacitance, because of the small-signal considerations and closed-loop stability, the transconductance of the last stage must be greater than that of the first and second stages. So, the slew rate of the OTA is mainly limited by the bias current of the first stage. Therefore, to reduce the settling time, it is necessary to boost the current of the first stage in the slewing phase without needing additional static power dissipation. In this paper, a three-stage OTA with a class AB structure in the first stage is proposed to improve the slew rate of the OTA.

3 Proposed three-stage class AB NMC OTA

3.1 Proposed OTA structure

Figure 2 shows the structure of the proposed three-stage class AB OTA. The first stage consists of a pMOS input pair, an active load, and a nonlinear current mirror. This nonlinear current mirror dramatically reduces the quiescent current and boosts the bias current during the slewing phase, and hence, improves the slew rate of the OTA [22, 23]. Recently, several types of nonlinear current mirrors have been proposed to enhance the slew rate of the OTAs [24, 25], which they need additional bias voltages to realize. But the nonlinear current mirror which is used in this paper is very power efficient because any additional bias branches or voltages are not needed [22]. The

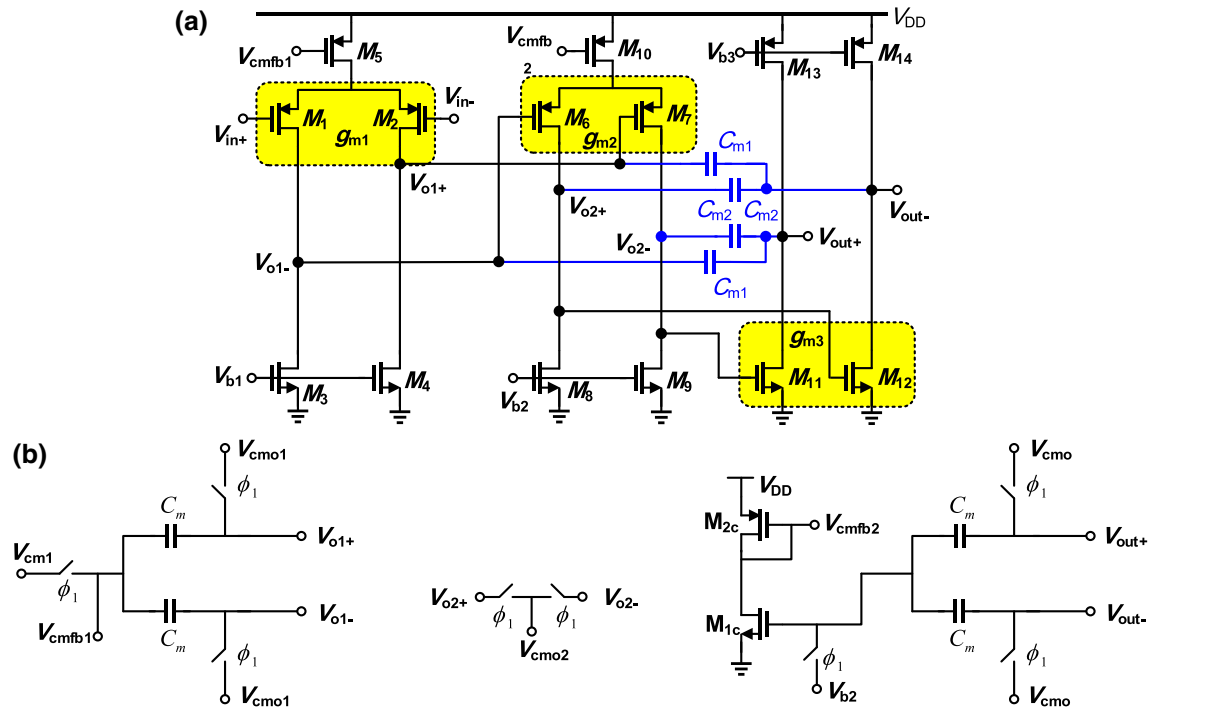

Fig. 1 **a** A typical fully-differential circuit implementation of a three-stage class A OTA (bias circuitry not shown for simplicity) and **b** CMFB circuits

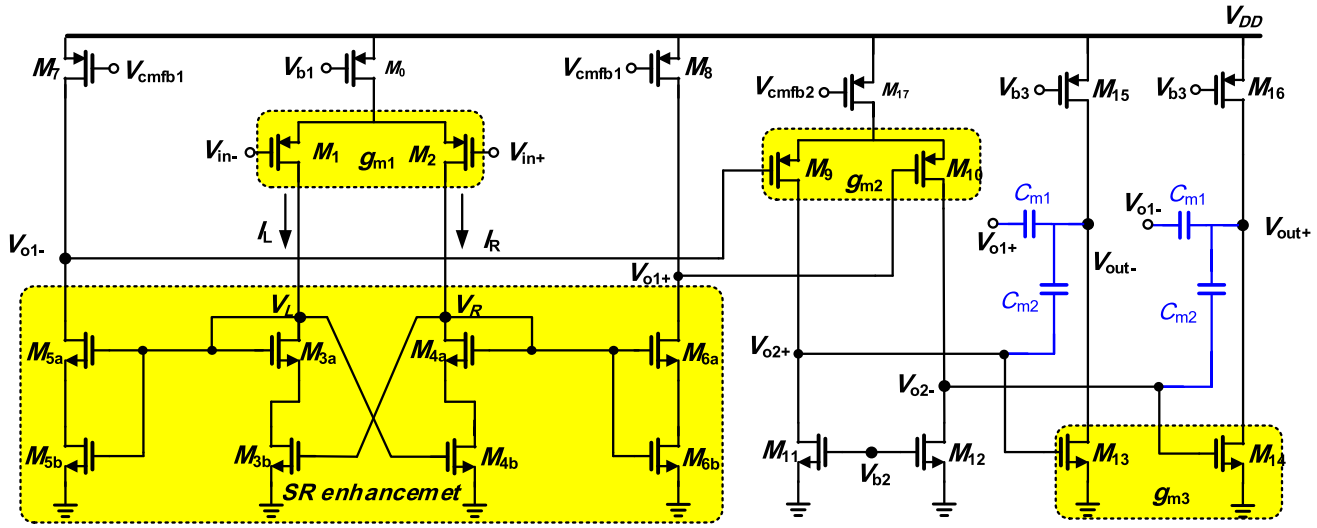

Fig. 2 Proposed three-stage class AB OTA (bias and CMFB circuits are not shown for simplicity)

nonlinear current mirror comprises of M_{3a} to M_{6b} transistors which are shown in Fig. 2, and it is used to build the class AB operation in the first stage of the proposed OTA. The second stage consists of a tail current source transistor, M_{17}, a pMOS differential pair with M_9 and M_{10}, and an nMOS active load with M_{11} and M_{12} transistors. The last stage comprises of an nMOS differential pair with M_{13}-M_{14} and a pMOS active load with M_{15}-M_{16} transistors.

As for the conventional three-stage class A OTA shown in Fig. 1(a), for this proposed three-stage class AB OTA, two separate switched-capacitor CMFB circuits shown in Fig. 1(b) are used to define the output common-mode voltage of the amplifier stages. To reduce the transistors transconductance dependence on the power supply voltage, temperature and process variations, a constant g_m biasing circuit is used in both class A and class AB OTAs [26].

In the proposed OTA, the slew rate enhancement becomes possible due to the dynamically changing of the V_L and V_R nodes voltage, and as a result, changing at the first stage current in the slewing phase. In the slew rate enhancement structure, transistors $M_{3b\text{-}6b}$ are designed to operate in the triode region. The same aspect ratio is selected for $M_{3b\text{-}6b}$ and $M_{3a\text{-}6a}$ transistors, respectively. Therefore, in the quiescent condition, $V_R = V_L$ and $M_{3b\text{-}6b}$ transistors have the same gate voltage. As a result, the resistance seen at the source of the $M_{3a\text{-}6a}$ transistors is equivalent and hence a 1:1 current ratio is achieved. The performance of the first stage at different modes is as follows.

If no differential voltage exists at the input of the amplifier, as mentioned above, $V_R = V_L$ and the copy ratio of the current mirror is still 1:1. But, when a large positive differential input voltage, V_{in}, is applied to the OTA's input, I_L increases and I_R decreases, and as a result, V_L increases and V_R decreases. So, the transistor M_{3b} enters into the saturation region and its drain-source resistance is increased while the drain-source resistance of M_{5b} is decreased since V_L is increased. In consequence, the copy ratio of M_{3a}-M_{5a} current mirror is enhanced. At the same time, the drain-source resistance of M_{4b} is decreased when V_L is increased while the drain-source resistance of M_{6b} is increased as V_R is decreased. Therefore, the copy ratio of M_{4a}-M_{6a} current mirror is decreased. If the differential input voltage is totally unbalanced ($V_{in+} > > V_{in-}$), $I_R = 0$ and $V_R = 0$, and as a result, the transistor M_{3b} is turned off. In consequence, V_L rises and gives the maximum current of the first stage output, and the slew rate of the first stage, and hence, the total slew rate of the OTA is enhanced. Therefore, the output current of the first stage is determined by the channel width of M_{5a} and M_{5b} transistors and it is independent of the bias current.

Similar to the large positive differential input voltage, when a large negative differential input voltage, V_{in}, is applied to the OTA's input, I_R is increased and I_L is decreased, and as a result, V_R is increased while V_L is decreased. In consequence, the copy ratio of M_{4a}-M_{6a} current mirror is enhanced. When the differential input voltage is totally unbalanced ($V_{in-} > > V_{in+}$), $I_L = 0$ and $V_L = 0$, and as a result, the transistor M_{4b} is turned off. Therefore, V_R rises and gives the maximum current of the first stage output, and hence, the slew rate of the first stage of the OTA is enhanced.

When a large input signal is applied to the proposed class AB OTA, the differential slew rate at the output of the OTA stages is obtained as follows:

$$SR_2 = \frac{I_{D10}}{C_{m2}}, \quad SR_3 = \frac{2I_{D13} - I_{D5} - I_{D10}}{C_L}$$
$$SR = \min\left(\frac{I_{D10}}{C_{m2}}, \frac{2I_{D13} - I_{D5} - I_{D10}}{C_L}\right) \tag{2}$$

According to relation (2), the slew rate of the first stage is large owing to its class AB structure and the overall slew rate of the proposed OTA is limited by slew rate of the second and third stages.

3.2 Small-signal analysis

The small-signal model of a three-stage OTA with NMC compensation technique is shown in Fig. 3 where g_{mi}, R_i, and C_i represent the transconductance, output resistance and the equivalent parasitic capacitance of the corresponding gain stages, respectively. C_L includes the load capacitor as well as the third-stage output parasitic capacitors of the OTA. By assuming high DC gain in amplifier stages and load and compensation capacitors are much greater than all parasitic capacitances of the circuit, i.e. $g_{mi} r_i > > 1$ and C_L , C_{m1} , $C_{m2} > > C_{1,2}$, the open-loop signal transfer function of the three-stage NMC amplifier is expressed by [3]:

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} = A_{dc}\frac{1 - \frac{C_{m2}}{g_{m3}}s - \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}s^2}{(1 + sR_1g_{m2}R_2g_{m3}R_3C_{m1})(1 + s\frac{C_{m2}(g_{m3}-g_{m2})}{g_{m2}g_{m3}} + s^2\frac{C_{m2}C_L}{g_{m2}g_{m3}})} \tag{3}$$

where $A_{dc} = -g_{m1}R_1g_{m2}R_2g_{m3}R_3$ is the dc gain and $\omega_{p1} = 1/(R_1g_{m2}R_2g_{m3}R_3C_{m1})$ is the dominant pole. The dc gain relation of class A and proposed class AB OTAs only differs in output resistance of the first stage. R_1 is the first-stage output resistance and its value is given by:

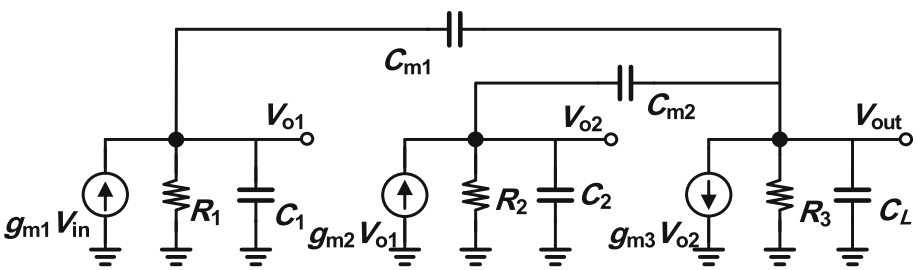

Fig. 3 Small-signal model of the three-stage NMC amplifier

$$R_{1,class\,A} = r_{ds1} || \, r_{ds4} \tag{4}$$

$$R_{1,class\,AB} = r_{ds7} || \, (r_{ds5a} + (1 + g_{m5a} r_{ds5a}) r_{ds5b}) \tag{5}$$

where r_{ds} is the drain-source resistance of the transistors. Since the transistor M_{5b} is in the triode region, its r_{ds} is very small and the first-stage output resistance of both structures is approximately the same. Therefore, there is not any significant improvement on the dc gain of the proposed OTA in comparison with the conventional class A OTA shown in Fig. 1. The gain-bandwidth product (ω_{GBW}) of the amplifier is well approximated by the open-loop unity-gain frequency as $\omega_{GBW} = g_{m1}/C_{m1}$. As it is seen from (3), the open-loop amplifier has three poles and two zeros. One of the poles is real and dominant and two others are complex-conjugate. The natural frequency, ω_n, and the damping factor, ζ, of the non-dominant poles are obtained as below:

$$\omega_n = \sqrt{\frac{g_{m2} g_{m3}}{C_{m2} C_L}} \tag{6}$$

$$\zeta = \frac{1}{2} \sqrt{\frac{C_{m2}}{C_L}} \sqrt{\frac{g_{m3}}{g_{m2}}} \tag{7}$$

The damping factor of the non-dominant complex poles is one of the most important parameters in the settling behavior of the OTAs [27]. So, it is necessary to adjust ζ properly, to have a fast settling three-stage amplifier. From the relations (6) and (7), it is seen that C_{m2} controls the damping factor of the non-dominant poles. Therefore, ζ can be controlled by setting an appropriate size of C_{m2} according to the following condition:

$$C_{m2} = 4\zeta^2 \frac{g_{m2}}{g_{m3}} C_L \tag{8}$$

By neglecting the zeros effect in the phase margin (PM), the value of the C_{m1} is achieved based on the required PM and damping factor of the non-dominant poles as [28]:

$$C_{m1} = 2\zeta \left(\zeta \tan(PM) + \sqrt{\zeta^2 \tan^2(PM) + 1} \right) \frac{g_{m1}}{g_{m3}} C_L \tag{9}$$

The value of the g_{m1} is chosen to satisfy the required gain-bandwidth and the value of g_{m3} must be much greater than that of g_{m1} and g_{m2}.

4 Simulation results

To prove the usefulness of the proposed three-stage class AB OTA shown in Fig. 2, it is designed using a 90 nm CMOS technology with HSPICE and circuit-level simulation results are provided. The goal is to design a fully-differential switched-capacitor sample and hold (S/H) circuit that is used in an 11-bit pipeline analog-to-digital converter (ADC) with a sampling rate of 50 MS/s and 2 V_{pp} differential input signal, where the power supply is 1.2 V. The simulated switched capacitor S/H is a flip-around type which is shown in Fig. 4 where ϕ_1 and ϕ_2 are the non-overlapping clock phases. The sampling capacitor is C_S = 1 pF and the effective load capacitance is C_L = 2 pF. C_L is comprised of the next stage capacitance, the CMFB capacitance, the parasitic capacitances of output transistors, and the feedback capacitors.

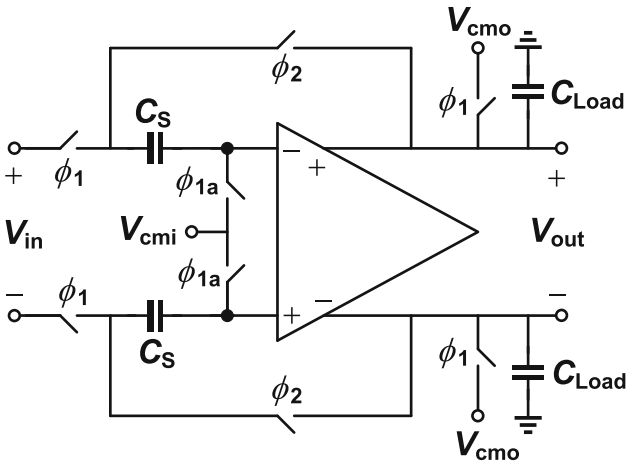

Fig. 4 Fully-differential flip-around S/H circuit

The designed OTA must meet the speed and accuracy requirements of the targeted S/H circuit. Therefore, in the first step, the requirements of the OTA must be met, such as dc gain, settling accuracy and settling time. In order to achieve the accuracy of 11 bits, the dc gain of the OTA must be $A_{dc} \geq 2^{12}$ = 72.2 dB, and the desired settling error is about $\psi \leq 0.0002$. The settling time (t_S) should be about half of the clock period. Therefore, according to the sampling frequency of 50 MS/s, the settling time must be less than 10 ns with less than 0.02% settling error.

For a fair comparison, both conventional class A and proposed class AB OTAs were designed with approximately equal power dissipation with the following design parameters: W_{GBW} = 150 MHz, ξ = 0.7, PM = 64°. By assuming that g_{m1} = 1 mA/V and g_{m2} = 2 mA/V, the obtained value for C_{m1} is about 1 pF from the gain-bandwidth requirement. g_{m3} and C_{m2} are obtained according to relations (8) and (9), respectively, as g_{m3} = 9.25 mA/V and C_{m2} = 0.8 pF. The final simulated device sizes of both OTAs are summarized in Table 1.

The simulated open-loop frequency response of both OTAs is shown in Fig. 5. The achieved unity-gain frequency and phase-margin of the proposed OTA are about 193.6 MHz and 61.8 degree, respectively. The simulated DC gain of the proposed OTA is 81.6 dB which is about 4 dB greater than DC gain of the class A OTA. This is achieved since instead of the simple current mirror, the

Table 1 Simulated device parameters of both OTAs

Class A NMC OTA			Proposed class AB NMC OTA		
Parameter	M × W/L	g_m (mA/V)	Parameter	M × W/L	g_m (mA/V)
M_1, M_2	2 × 8 µm/0.2 µm	**0.9 (g_{m1})**	M_1, M_2	2 × 4 µm/0.2 µm	**0.62 (g_{m1})**
M_3, M_4	2 × 1.8 µm/0.3 µm	1.1	M_0	4 × 4 µm/0.2 µm	1.03
M_5	4 × 8 µm/0.2 µm	1.9	M_{3a}, M_{4a}, M_{5a}, M_{6a}	1 × 1 µm/0.3 µm	0.33
M_6, M_7	4 × 6 µm/0.2 µm	**1.56 (g_{m2})**	M_{3b},M_{4b},M_{5b}, M_{6b}	2 × 1 µm/0.3 µm	0.17
M_8, M_9	4 × 1.8 µm/0.3 µm	1.2	M_7, M_8	6 × 2 µm/0.2 µm	0.71
M_{10}	8 × 6 µm/0.2 µm	2.7	M_9, M_{10}	4 × 6 µm/0.2 µm	**2.3 (g_{m2})**
M_{11}, M_{12}	8 × 3.5 µm/0.2 µm	**7.4 (g_{m3})**	M_{11}, M_{12}	4 × 1.8 µm/0.3 µm	2.41
M_{13}, M_{14}	8 × 16 µm/0.3 µm	11.4	M_{13}, M_{14}	8 × 3.5 µm/0.2 µm	**10.1 (g_{m3})**
C_{m1}, C_{m2} (pF)	0.8, 0.45		M_{15}, M_{16}	8 × 16 µm/0.3 µm	9.74
			M_{17}	8 × 6 µm/0.2 µm	5.4
C_L (pF)	2		C_{m1}, C_{m2} (pF)	0.8, 0.5	
			C_L (pF)	2	

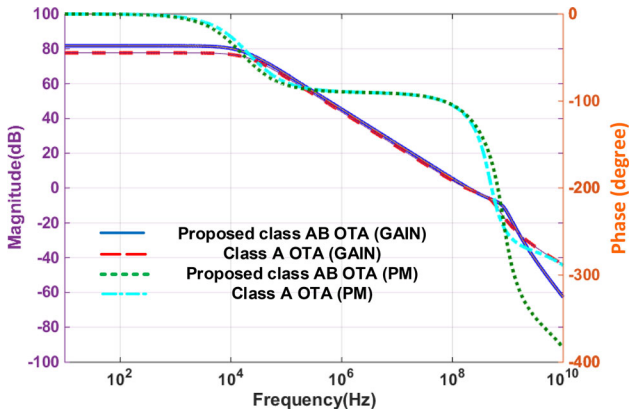

Fig. 5 Open-loop frequency response of the simulated OTAs

nonlinear current mirror is utilized in the first stage of the proposed OTA. The simulated closed-loop step response of both class A OTA and proposed class AB OTA is shown in Fig. 6 where a large differential input step of 1 V is applied. The settling time of the proposed three-stage class AB OTA with 0.02% settling error is 9.1 ns while for the conventional class A OTA, it is 15.7 ns. As shown in Fig. 6, there are some amounts of overshoot in step response. Nonetheless, this is acceptable in switched-capacitors circuits to achieve a fast settling behavior. Indeed, in switched-capacitor circuits, the settling time and accuracy are the most important parameters and the output voltage should be settled regardless of some rings and overshoots at the beginning of the step response. The achieved improvement in the settling time is mainly due to the dramatically enhancement in slew rate, which is 85.2 V/µ*s* for the conventional class A OTA and 327.3 V/µs for the proposed class AB OTA. Simulation results of the proposed three-stage class AB and conventional class A OTAs in different process corner cases and temperature variations are summarized in Table 2.

The simulated large-signal transient response of V_L and V_R node voltages and the first stage output current are illustrated in Fig. 7 when a large 1 V differential input voltage is applied to the proposed OTA in the closed-loop configuration. As it is seen, during the positive slewing, the drain current of M_{5a} and V_L are substantially increased. During the negative slewing phase, the M_{6a}'s drain current and the V_R are also substantially increased as theoretically expected. In consequence, the slew rate of the first stage is enhanced and the effectiveness of the proposed structure is well proved. It should be noted that in Fig. 4, the OTA is reset in phase ϕ_1. As a result, the output voltage and the other voltages and currents of the OTA are reset to the quiescent values as it is seen in Fig. 7.

To evaluate the robustness of the proposed class AB OTA against process and mismatch variations, extensive circuit-level Monte Carlo simulations have been done. The result is shown in Fig. 8 where the settling time is illustrated for 1000 runs in which both process and local variations of device parameters have been considered. As it is seen, the achieved settling time satisfies the targeted requirement.

In order to compare the proposed three-stage class AB OTA with respect to the conventional class A OTA, the small-signal and the large-signal figure-of-merits (FoMs) are used, which are defined as $FoM_S = GBW \times C_L$/power

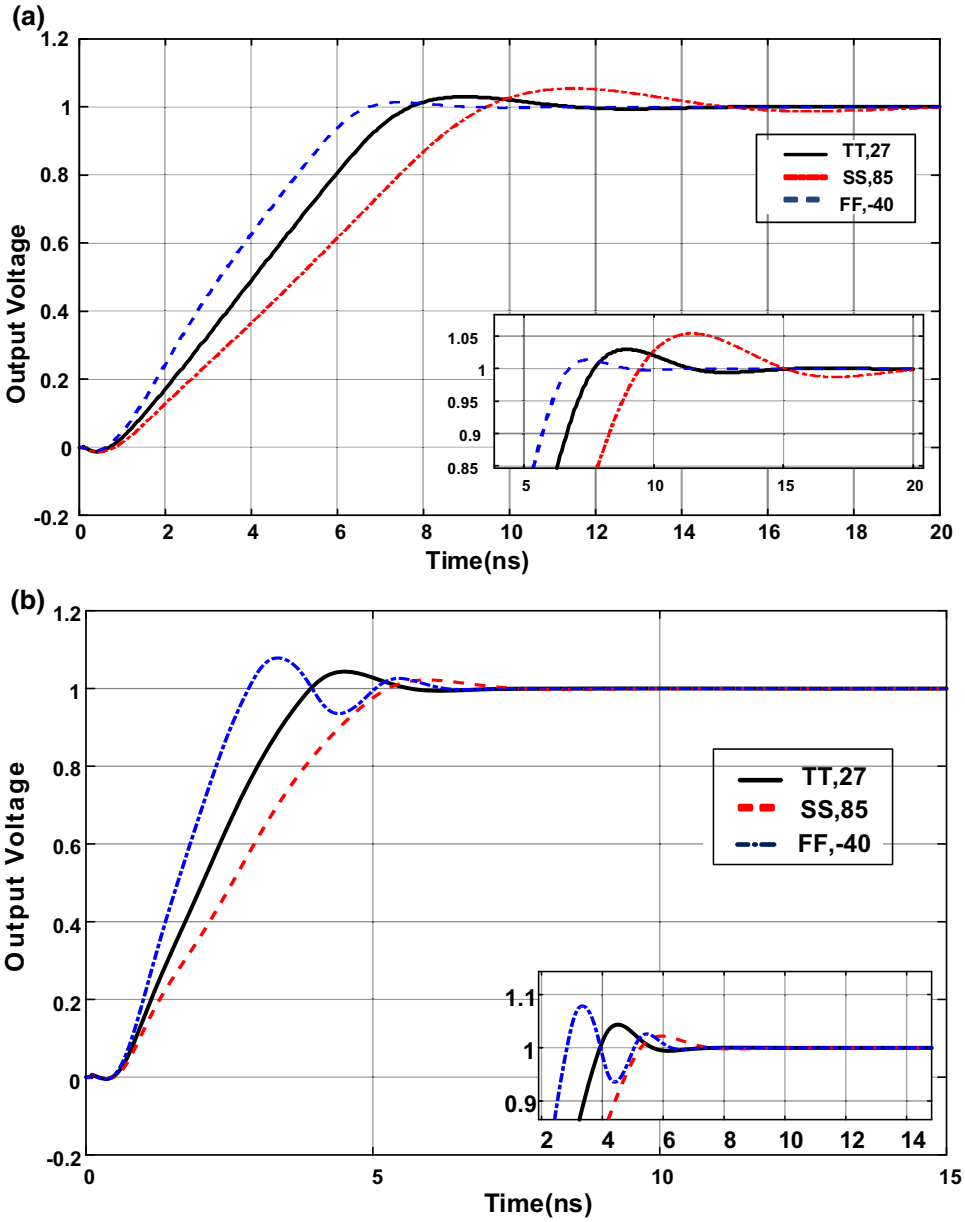

Fig. 6 Simulated step response of **a** three-stage class A and **b** proposed class AB OTAs

and $\mathrm{FoM_L} = SR \times C_\mathrm{L}/\mathrm{power}$, respectively. As it is seen in Table 2, the main advantage of the proposed OTA is its large slew rate which offers 210% improvement in the $\mathrm{FoM_L}$. This enhancement has a considerable effect on the settling performance of the proposed three-stage OTA. It is worth mentioning that the same value of compensation capacitors is utilized in both proposed OTA and conventional class A OTA which is shown in Fig. 1. Therefore, the required active die area in both OTAs will be approximately the same since it is mostly occupied with metal–insulator-metal (MIM) capacitors in mixed-signal integrated circuits. Finally, in Table 3, the proposed class AB three-stage OTA is compared with some other class AB OTAs which have been utilized in switched-capacitor circuits. It should be noted that in fast-settling switched-capacitor circuits, the load capacitor is small and the OTA design is different with those that are used in low-dropout (LDO) voltage regulators. In LDO regulators, the load capacitor is large and it is in the range of several hundreds of pF while in switched-capacitors, it is usually in the range

Table 2 Simulation results summary

Parameter	Class A NMC			Proposed Class AB NMC		
	TT @ 27 °C	SS @ 85 °C	FF @ − 40 °C	TT @ 27 °C	SS @ 85 °C	FF @ − 40 °C
DC gain (dB)	77.6	77.4	78.1	81.6	79.4	83.7
f_{GBW} (MHz)	175	122.4	245	193.6	168.6	229.1
Phase margin (degree)	62.8	64.5	60.0	61.8	62.5	61.8
0.02% settling time, t_s @ 1 V input step	15.7	18.3	14.1	9.1	9.8	7.85
Static power dissipation (mW)	2.5	2.3	2.65	3.09	3.0	3.35
Average slew rate (V/μs)	85.2	79.1	93.8	327.3	256.2	470.6
FoM_S (MHz × pF/mW)	140	106	184	125.3	112.4	136.8
FoM_L (V/μs × pF/mW)	68.2	68.8	70.8	211.4	171	280.95
V_{DD}	1.2 V					
Technology	90 nm CMOS					

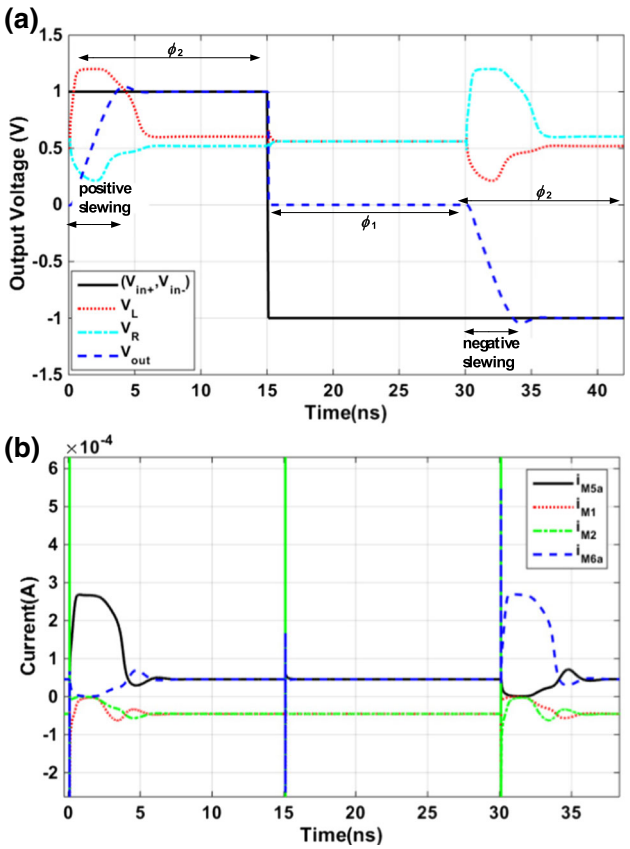

Fig. 7 Simulated transient response for **a** V_L, V_R, input and output voltages and **b** input and output currents of the first-stage during the OTA slewing

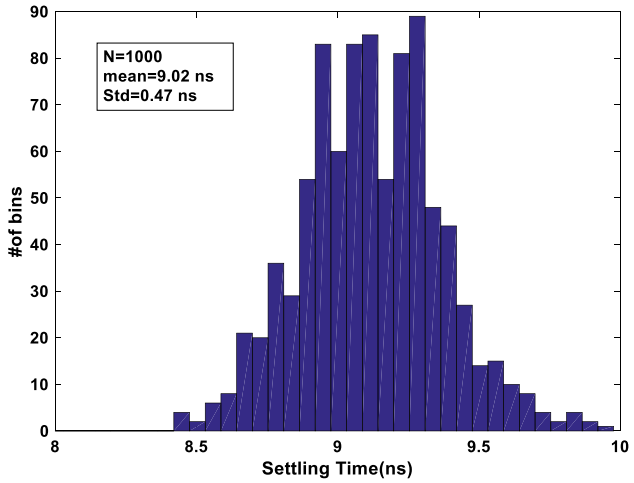

Fig. 8 Monte Carlo simulation results of the settling time

of several pF. According to Table 3, the achieved results of the proposed three-stage Class AB OTA are comparable with references and it is also better in some aspects.

5 Conclusions

In this paper, a new three-stage class AB OTA with NMC compensation technique is proposed. The slew rate of the NMC amplifier is mainly limited by the bias current of the input stage. By using a class AB structure in the input stage, the slew rate of the proposed OTA is well increased. The proposed class AB OTA achieves a fast-settling

Table 3 Performance comparison of several three-stage amplifiers which have been used in switched-capacitor circuits

Parameter	IEICE 2011 [12]	AICSP 2014 [13]	ICEE 2014 [17]	AICSP 2015 [18]	This work
Supply (V)	1.8	1.2	1.2	1.2	1.2
DC gain (dB)	85.7	72.1	72.9	72.4	81.6
f_{GBW} (MHz)	21.3	202.8	110.7	121	193.6
Phase margin (degree)	62.0	63.2	61.3	63.8	61.8
C_L (pF)	2	2	2	2	2
Average slew rate (V/μs)	–	–	120.9	487.9	327.3
Implementation	Single-ended	Fully-differential	Fully-differential	Fully-differential	Fully-differential
Settling time t_{ss+}/t_{ss-} (ns) @ 1 V input step	13.1 20.9	8.7	17.5	7.5	9.1
Settling accuracy	0.1%	0.02%	0.02%	0.02%	0.02%
Static power dissipation (mW)	0.54	5.2	3.0	2.5	3.25
FoM_S (MHz × pF/mW)	78.8	78	73.8	96.8	125.3
FoM_L (V/ μs × pF/mW)	–	–	80.6	390.3	211.4
Technology	0.35 um	90 nm	90 nm	90 nm	90 nm

performance in switched-capacitor circuits in comparison with the conventional class A OTAs.

References

1. Kim, Y.-J., & Lee, S.-H. (2012). A 10-b 120-MS/s 45 nm CMOS ADC using a re-configurable three-stage switched amplifier. *Analog Integrated Circuits and Signal Processing, 72*(1), 75–87.
2. Huijsing, J. (1995). *Frequency compensation techniques for low-power operational amplifiers*. Amsterdam: Kluwer Academic Publishers.
3. Leung, K. N., & Mok, P. K. T. (2001). Nested Miller compensation in low-power CMOS design. *IEEE Transactions on Circuits Systems II: Analog Digital and Signal Processing, 48*(4), 388–394.
4. M. Jalalifar, M. Yavari, & F. Raissi. (2008) "A novel topology in reversed nested Miller compensation using dual-active capacitance," *IEEE International Symposium on Circuits and Systems,* 2270–2273.
5. Yavari, M. (2010). Active-feedback single Miller capacitor frequency compensation techniques for three-stage amplifiers. *Journal of Circuits, Systems, and Computers, 19*(7), 1381–1398.
6. Garimella, A., Rashid, M. W., & Furth, P. M. (2010). Reverse nested Miller compensation using current buffers in a three-stage LDO. *IEEE Transactions on Circuits and Systems II: Express Briefs, 57*(4), 250–254.
7. Chong, S. S., & Chan, P. K. (2012). Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load. *IEEE Journal of Solid-State Circuits, 47*(9), 2227–2234.
8. Mojarad, M., & Yavari, M. (2014). A low power four-stage amplifier for driving large capacitive loads. *International Journal of Circuit Theory and Applications, 42*(9), 978–988.
9. Grasso, A. D., et al. (2018). High-performance three-stage single-Miller CMOS OTA with no upper limit of C_L. *IEEE Transactions on Circuits and Systems-II: Express Briefs, 65*(11), 1529–1533.
10. Liu, S., et al. (2019). A 1.2-V 2.41-GHz three-stage CMOS OTA with efficient frequency compensation technique. *IEEE Transactions on Circuits and Systems I: Regular Papers, 66*(1), 20–30.
11. Riad, J., Estrada-Lopez, J. J., Padilla-Cantoya, I., & Sanchez-Sinencio, E. (2020). Power-scaling output-compensated three-stage OTAs for wide load range applications. *IEEE Transactions on Circuits and Systems I: Regular Papers, 67*(7), 2180–2192.
12. Yavari, M. (2011). A design procedure for CMOS three-stage NMC amplifiers. *IEICE Transactiopns on Fundamentals, E94-A*(2), 639–645.
13. Golabi, S., & Yavari, M. (2014). Design of CMOS three-stage amplifiers for fast-settling switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing, Springer, 80*(2), 195–208.
14. Yavari, M., & Shoaei, O. (2004). Low-voltage low-power fast-settling CMOS operational transconductance amplifiers for switched-capacitor applications. *IEE Proceedings-Circuits, Devices and Systems, 151*(6), 573–578.
15. Yavari, M. (2010). Single-Stage class AB operational amplifier for SC circuits. *IET Electronics Letters, 46*(14), 977–979.
16. Yavari, M., & Moosazadeh, T. (2014). A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing, Springer, 79*(3), 589–598.
17. S. Golabi and M. Yavari (2014) "High-Speed three-stage operational transconductance amplifiers for switched-capacitor circuits". *Iranian Conference on Electrical Engineering* (ICEE), 413–417.
18. Golabi, S., & Yavari, M. (2015). A three-stage class AB operational amplifier with enhanced slew rate for switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing, 83*(1), 111–118.
19. Carvajal, R. G., Ramírez-Angulo, J., López-Martín, A. J., Torralba, A., Galán, J. A. G., Carlosena, A., & Chavero, F. M. (2005). The flipped voltage follower: A useful cell for low-voltage low-power circuit design. *IEEE Transactions on Circuits and Systems I: Regular Papers, 52*(7), 1276–1291.
20. Garde, M. P., & Carvajal, R. G. (2018). Super class-AB recycling folded cascode OTA. *IEEE Journal of Solid-State Circuits, 53*(9), 2614–2623.

21. Cabrera-Bernal, E., Pennisi, S., Grasso, A. D., Torralba, A., & Carvajal, R. G. (2016). 0.7-V three-stage class-AB CMOS operational transconductance amplifier. *IEEE Transactions on Circuits and Systems I: Regular Papers, 63*(11), 1807–1815.
22. Pérez-Nicoli, P., Veirano, F., Lisboa, P. C., & Silveira, F. (2016). Low-power operational transconductance amplifier with slew-rate enhancement based on non-linear current mirror. *Analog Integrated Circuits and Signal Processing, 89*(3), 521–529.
23. Sutula, S., Dei, M., Terés, L., & Serra-Graells, F. (2016). Variable-mirror amplifier: a new family of process-independent class-AB single-stage OTAs for low-power SC circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers, 63*(8), 1101–1110.
24. Galan, J. A., Lopez-Martin, A. J., Carvajal, R. G., Ramirez-Angulo, J., & Rubia-Marcos, C. (2007). Super class-AB OTAs with adaptive biasing and dynamic output current scaling. *IEEE Transactions on Circuits and Systems I: Regular Papers, 54*(3), 449–457.
25. Ramirez-Angulo, J., & Holmes, M. (2002). Simple technique using local CMFB to enhance slew rate and bandwidth of one-stage CMOS op-amps. *Electronics Letters, 38*(23), 1409–1411.
26. Carusone, T. C., Johns, D. A., & Martin, K. (2012). *Analog integrated circuit design* (2nd ed., pp. 307–309). Hoboken: Wiley.
27. Nguyen, R., & Murmann, B. (2010). The design of fast-settling three-stage amplifiers using the open-loop damping factor as a design parameter. *IEEE Transactions on Circuits and Systems I, 57*(6), 1244–1254.
28. Pugliese, A., Cappuccino, G., & Cocorullo, G. (2005). Nested Miller compensation capacitor sizing rules for fast-settling amplifier design. *Electronics Letters, 41*(10), 573–575.

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