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A LOW-VOLTAGE LOW-POWER 10-BIT 200 MS/S PIPELINED ADC IN 90 NM CMOS*

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This paper presents a low-power 10-bit 200 MS/s pipelined ADC in a 90 nm CMOS technology with 1 V supply voltage. To decrease the power dissipation efficiently, a new architecture using a combination of two power reduction techniques named double-sampling and opamp-sharing has been used to reduce the power consumption significantly, without any degradation in the performance of the ADC. In addition, the stage scaling technique has been applied to the ADC efficiently, and two-stage class A/AB and class A amplifiers and dynamic comparators have been used in sample and hold and sub-ADCs. According to HSPICE simulation results, the 10-bit 200 MSample/s pipeline ADC with a 9.375 MHz, 1-$V_{P-P,diff}$ input signal in a 90 nm CMOS process achieves a SNDR of 58.5 dB while consuming only 30.9 mW power from a 1 V supply voltage.

Keywords: Pipelined ADC; low-power; stage scaling; double sampling; opamp sharing.

1. Introduction

Nowadays, high-speed medium-resolution analog-to-digital converters (ADCs) play a critical role in modern digital communication and signal processing systems. They are widely used in applications which require a combination of high-speed and low-power. However, the power dissipation of an ADC is remarkably raised as its sampling rate and resolution increase.

In general, pipelined ADCs have proven to be very efficient architectures for managing the trade-off between low power dissipation and high conversion rate. In a pipelined ADC, the high frequency input is sampled by the sample-and-hold (S/H)

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circuit, and then each stage samples the residue from its previous stage and provides a digital output code and a residual voltage. This feature allows each stage to start processing a new sample as soon as its residue is sampled by the following stage. The digital output codes constitute the output of the entire ADC, leading all of the stages to operate concurrently and to give one output sample per clock cycle. Thus, pipelined ADCs can operate at very high sampling rates.[1]

ADCs often appear as the bottleneck in high performance mixed-signal systems. Since it is not drastically reduced by device scaling, the power dissipation of analog circuits is becoming increasingly an important design issue.[2] In a conventional pipelined ADC, the amplifiers of two successive stages are active in opposite non-overlapping phases. Based on this fact some power-reduction techniques like amplifier sharing and double sampling, which make use of the amplifiers in both phases have been introduced. Although each of these approaches can introduce some degradation in the performance of a single pipeline, they have been widely used because of their impressive effect on power consumption.[1–5]

In this paper, different design methods are combined to achieve very low power consumption in a medium-resolution high-speed pipeline ADC. Considering the advantages and disadvantages of the mentioned techniques, double sampling and amplifier sharing along a single pipeline, the authors have presented an architecture which takes advantage of them both and attenuates their drawbacks. In addition, capacitor scaling is applied to the pipeline stages efficiently. Gain-boosted two-stage class A/AB and class A amplifiers and dynamic comparators have also been employed to achieve low-power and high performance. Simulation results for a 10-bit 200 MS/s ADC in a 90 nm CMOS process with 1 V supply voltage show 58.5 dB SNDR while consuming only 30.9 mW power.

This paper is organized as follows. Section 2 describes the architecture of the presented ADC. Section 3 demonstrates the circuit implementation of the key building blocks. The simulation results and conclusions are presented in Secs. 4 and 5, respectively.

2. The Proposed Architecture

2.1. *Comparison between amplifier sharing and double sampling*

In the conventional opamp sharing technique an opamp is shared between two adjacent stages of a single pipeline.[3] As shown in Fig. 1(a), in $\phi_1$when the first stage is in the sampling mode, the amplifier is used in the second stage which is in the multiplying digital-to-analog converter (MDAC) mode. Then in ϕ_2, the second stage samples its input and the first stage uses the amplifier. In this way, the number of amplifiers is halved compared to the basic pipelined ADC. However, the total power dissipation is only reduced by one-third, because the capacitor scaling cannot be efficiently applied to the ADC.[4]

In the basic pipeline ADC, the optimum sampling capacitor for each stage is determined by noise budgeting, which leads each stage to have a relatively smaller sampling capacitor in comparison with its previous stage, without significant degradation in the total signal-to-noise ratio (SNR). As a result, the current consumed in the amplifier of the second stage can be considerably decreased compared to that of the first one, since the power of the amplifier is scaled down according to the sampling capacitor. Therefore, when an amplifier is shared between the first and the second stages, the capacitor scaling cannot be effectively used along the ADC.[4] To show more clearly how this problem affects the power consumption of a pipelined ADC, a model based on what is introduced in Ref. 6 has been used to plot the normalized total power consumption (P) versus scaling factor (δ) in two

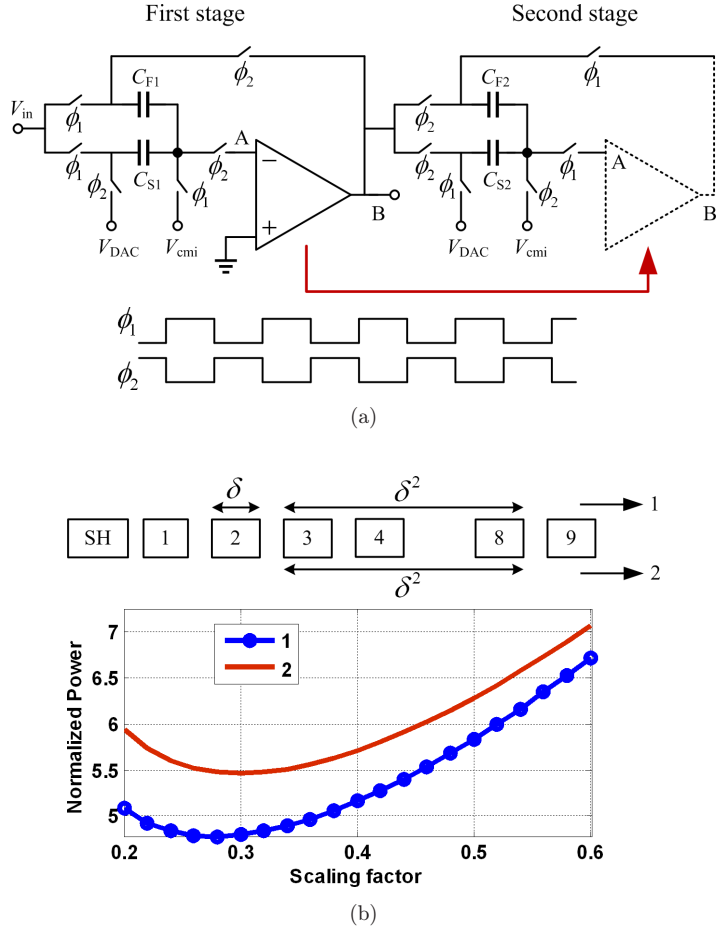

Fig. 1. (a) Two consecutive stages of a pipelined ADC using the conventional amplifier sharing technique, and (b) two configuration of a 9-stage 1.5-bit per stage pipelined ADC and their power consumption versus the scaling factor.

configurations of a 9-stage 1.5-bit per stage pipelined ADC. As illustrated in Fig. 1 (b), the stage 2 and stages 3 to 8 of the first configuration are scaled compared to the stage 1 with scaling factors δ and δ^2, respectively. But, in the second configuration the amplifiers of stage 2 and stage 1 are the same and only stages 3 to 8 are scaled to stage 1 with scaling factor δ^2.

The total power in a 1.5 bit/stage pipelined ADC (P) is proportional to:

$$P \propto \left(\frac{1}{C_{s0}} + \frac{1}{2^2 C_{s1}} + \frac{1}{2^4 C_{s2}} + \frac{1}{2^6 C_{s3}} + \cdots\right) \sum_{i=0}^{m} C_{si}\,, \tag{1}$$

where C_{s0} and C_{si} are the sampling capacitors of sample-and-hold (S/H) and the ith stage, respectively, and m is the number of the stages of pipeline.

Equation (1) which is a function of δ can be written as Eqs. (2) and (3) for configurations 1 and 2 in Fig. 1(b), respectively:

$$P \propto \left(1 + 2^{-2} + \frac{2^{-4}}{\delta} + \frac{2^{-6} + 2^{-8} + 2^{-10} + \cdots + 2^{-16}}{\delta^2}\right)(1 + 1 + \delta + 6\delta^2)\,, \tag{2}$$

$$P \propto \left(1 + 2^{-2} + 2^{-4} + \frac{2^{-6} + 2^{-8} + 2^{-10} + \cdots + 2^{-16}}{\delta^2}\right)(1 + 1 + 1 + 6\delta^2)\,, \tag{3}$$

where C_{s0} and C_{s1} are assumed to be equal. Figure 1(b) shows the results in which the curves named 1 and 2 belong to the first and second configurations, respectively. The results obviously show that the total power dissipation of a 1.5 bit/stage pipelined ADC remarkably increases when the second stage is not scaled down compared to the first one. Therefore, this is a considerable drawback of amplifier sharing, since it is regarded as a power reduction technique.

As it is shown in Fig. 2, each gain stage using the double sampling technique has its own opamp. But, there are two sets of capacitors in each stage, C_{S1}–C_{F1} and

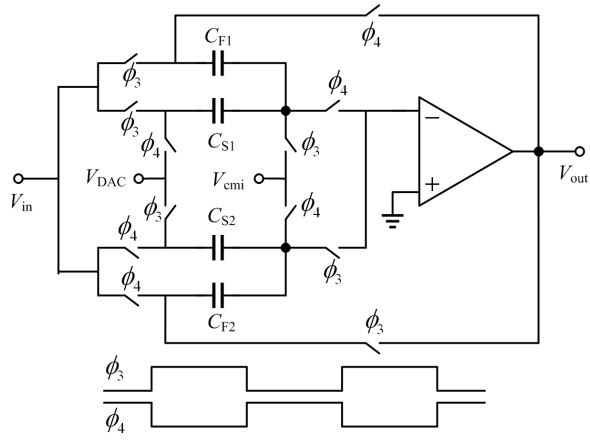

Fig. 2. A gain stage using the double sampling technique.[7]

C_{S2}–C_{F2}, each of which samples the input signal at $f_s/2$, while the sampling frequency of the whole ADC is f_s.[7] For example, in ϕ_3, C_{S1} and C_{F1} sample the input signal, while C_{S2} and C_{F2} are in the amplification configuration. In this way, the amplifier operates in both phases. Therefore, not only the double sampling technique reduces the power consumption of the amplifier due to its reduced unity-gain-bandwidth, but, also makes it possible to use the optimum amplifier in each stage, as opposed to the conventional amplifier sharing technique.

2.2. *The proposed architecture*

The proposed architecture for a 10-bit pipeline ADC with 1.5-bit per stage is presented in Fig. 3. The front-end sample-and-hold and the first two stages use the double sampling (DS) technique. In this way, each of the stages has its optimum amplifier; the power of which is approximately halved in comparison with that in the basic pipeline ADC. In addition, the S/H amplifier has a lower power compared to that of a pipeline ADC using the conventional opamp sharing in which the amplifier of the S/H cannot be shared.

In the last stages of pipelined ADCs, the size of the optimum sampling capacitors which is based on noise and matching characteristics do not usually differ for two successive stages. For example, in the prototype designed ADC, the optimum unit capacitor for stage 3 is equal to that of stage 4, and the same is true for the next stages of the pipeline. Therefore, an amplifier can be shared between these two consecutive stages optimally. This fact leads the double sampling technique not to be preferable for these last stages. Moreover, it adds too many switches and capacitors to the ADC which makes it inefficient from the chip area point of view. Thus, the amplifiers in the last stages of the proposed architecture are shared between two successive stages instead of being double sampled. In this way, the number of opamps, and therefore the area devoted to them, is also reduced compared to that of a pipelined ADC where all of the stages use the double sampling technique.

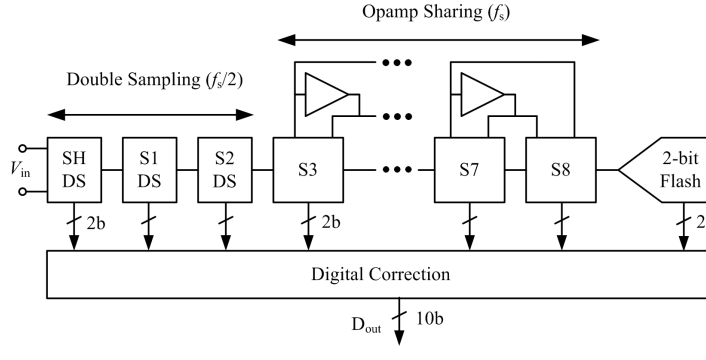

Fig. 3. The proposed architecture.

Since the architecture uses both opamp sharing and double sampling techniques to reduce the power consumption, the capacitor scaling can be applied to it in the most effective way, as apposed to the conventional amplifier sharing along a single pipeline. In addition, unlike to an ADC using the double sampling technique, it does not use more capacitors and switches in order to reduce the power dissipation, which results in this ADC being efficient from the die area and design viewpoints.

3. Circuit Implementation

3.1. *Skew insensitive sample-and-hold circuit*

The performance of S/H circuit directly affects the accuracy and speed of the ADC. The input S/H, which drives the large load capacitance of the next stage, must be as accurate as the total resolution of the converter. The S/H, operating in both non-overlapping phases, uses the timing skew insensitive double sampled architecture.[8] In this way, the systematic error between the channels, resulting from the inherent parallelism of the double sampling circuit, is avoided.

A two-stage class A/AB amplifier based on an OTA introduced in Ref. 9, and depicted in Fig. 4(a) has been used as the S/H amplifier. The first stage of the amplifier is a gain-boosted folded cascode opamp (gain-boosting amplifiers are not shown in the figure for clarity) with a p-type input pair that works properly under low supply voltage and needs low input common-mode voltage. Since the S/H drives a comparably high capacitance load, active current mirrors are used as the second stage instead of simple common-source amplifiers. The class AB operation of this stage ensures that the slew limiting occurs only in the first stage. For frequency compensation, the amplifier employs the hybrid-cascode compensation scheme where two capacitors are used between two low-impedance nodes of the first stage and the output node.[9] This scheme yields a higher amplifier bandwidth than the conventional Miller and cascode compensation methods as demonstrated in Ref. 17.

Since this opamp is active in both phases, there is a potential problem of introducing a correlation between the consecutive samples due to the finite gain of opamp; a charge is injected in the input parasitic capacitance which never resets. Therefore, the output voltage will be a recursive function of the present and previous samples.[10] To increase the gain and overcome this "memory effect" in a 10-bit pipeline ADC, the gain boosting technique has been applied to the first stage of the amplifier to achieve a DC gain higher than $2 \times (2^{10+1})$. The boosting amplifiers are two fully-differential folded cascode opamps which have a p-type or n-type input differential pair for nMOS and pMOS cascode transistors of the main amplifier to allow a flexible input common-mode range.

A simple switched-capacitor common-mode feedback (CMFB) circuit is used in the first stage of the S/H amplifier. The CMFB circuit of the second stage of the amplifier is shown in Fig. 4(b), where ϕ_1 and ϕ_2 are two non-overlapping phases.[9] The output common mode voltage is used to control two common source amplifiers,

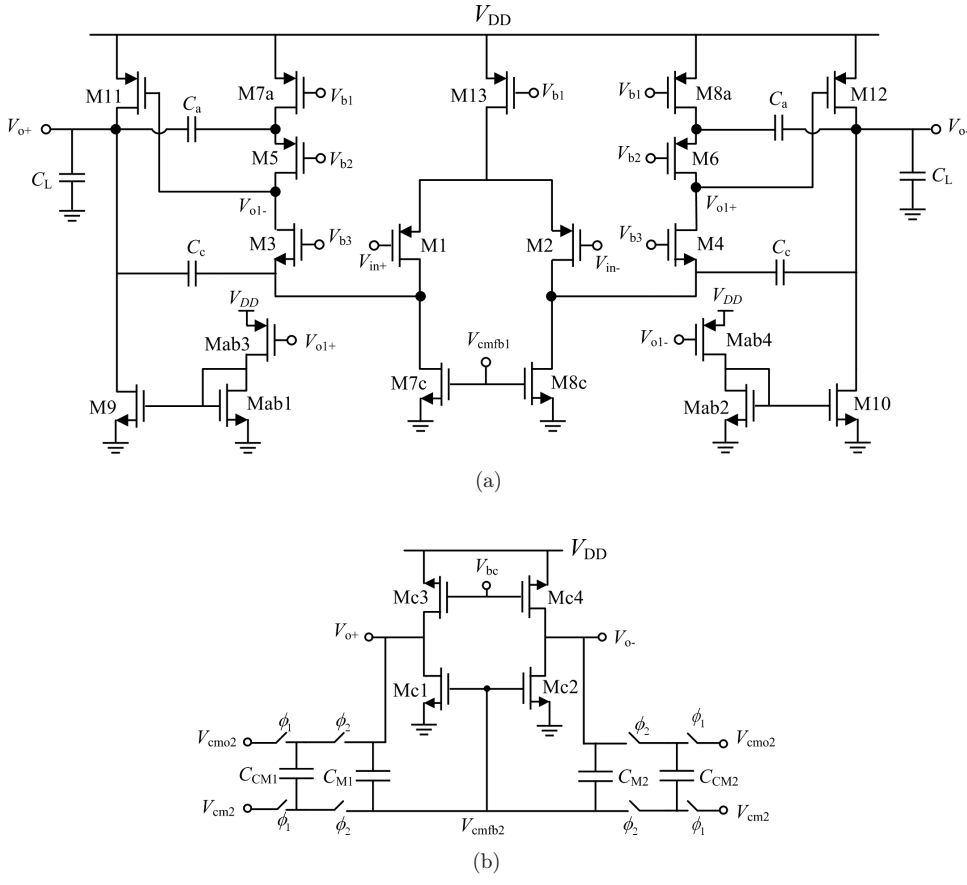

Fig. 4. (a) The two stage class A/AB amplifier, used in S/H, (b) CMFB circuit of the second stage of the amplifier.[9]

*Mc*1 and *Mc*2, which drive the output nodes. It should be mentioned that the CMFB circuits have been implemented with one set of output holding capacitors ($C_{M1}-C_{M2}$) and two sets of resetting capacitors ($C_{CM11}-C_{CM21}$ and $C_{CM21}-C_{CM22}$) although only one set of which is shown in Fig. 4(b) for simplicity.[11] These two resetting capacitors work on both non-overlapping phases leading the opamp to maintain the common-mode output level with the double sampling technique.

3.2. *Multiplying digital-to-analog converter*

As explained in Sec. 2, the MDACs of the first two stages employ the double sampling technique, and the amplifier of these stages have the same structure as that of S/H circuit. The amplifiers of the next stages also have the same structure as that of S/H circuit except that they do not use the class AB technique in their second stage, since their capacitance load is relatively smaller and it would not be efficient to

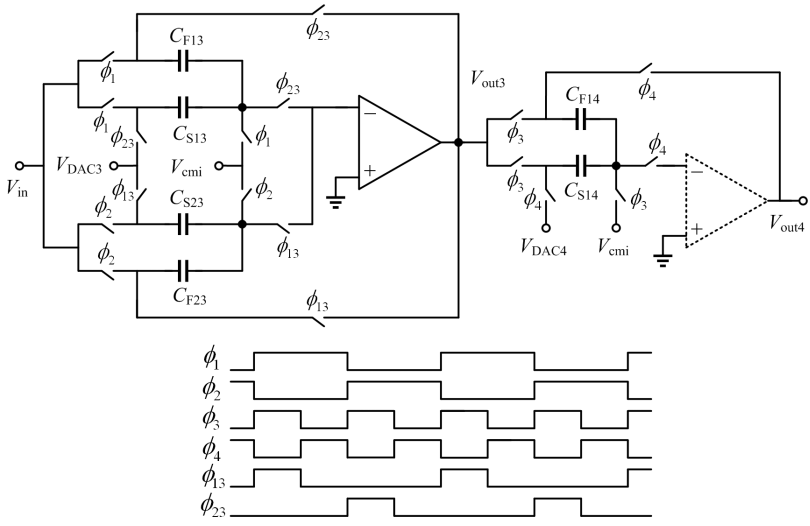

Fig. 5. The proposed configuration for the third stage and its timing.

use the class AB approach. Therefore, simple common-source amplifiers have been used as the second stage of the opamps. Moreover, depending on the gain requirements of the stages, the two gain-boosting opamps have only been applied to the amplifiers of stages 1 and 2, one gain-boosting opamp has been applied to pMOS cascode transistors of the amplifier in stage 3, and the other stages have not used the gain-boosting technique.

Figure 5 shows the proposed switched capacitor architecture of the third stage which matches the double sampling stages (stages 1 and 2) with the next stages of the pipeline. The single-ended structure is shown for simplicity. The two sets of capacitors, $C_{S13}-C_{F13}$ and $C_{S23}-C_{F23}$, sample the input signal to stage 3 in ϕ_1 and ϕ_2, respectively. But these capacitors are connected to the amplifier in only half of the next clock phase (ϕ_2 or ϕ_1), which is ϕ_{23} and ϕ_{13}. This means that the amplifier of stage 3 works in ϕ_3 and it can be used for stage 4 in ϕ_4. In this way, this opamp is shared between stage 3 and stage 4 in ϕ_3 and ϕ_4, while the input signal to stage 3 is sampled in ϕ_1 and ϕ_2. In other words, the holding time for outputting the signals from stage 2 to stage 3 is the same as a conventional stage using the double sampling technique, while the amplifiers of stages 3 to 8 are shared between two adjacent stages and are twice as fast as the double sampling stages (stages 1 and 2).

3.3. *Switches*

The input sampling switches and the feedback switches of S/H and MDACs are implemented in a reliable bootstrapped configuration introduced in Ref. 12 to minimize the nonlinearity introduced by the signal-dependant on-resistance of the switches, based on the linearity requirement of a 10-bit ADC. In addition, some

switches connecting to $V_{DD}/2$ needed to use this configuration to provide the proper on-resistance.

3.4. *Comparators*

In the 1.5-bit per stage pipeline architecture, there is one redundant quantization level in each sub-ADC which with the digital correction allows $\pm V_{Ref}/4$ offset in the comparator decision levels to be tolerable where V_{Ref} is the maximum single-ended amplitude of the input signal. Therefore, a switched-capacitor based dynamic comparator consuming no static power has been used in the prototype ADC which is depicted in Fig. 6.[13,14] The comparison threshold is determined by the ratio of the sampling capacitors, which is 4:1 in this design. The size of C has been chosen based on the matching and common-mode charge injection errors. When ϕ_c is low, transistors M_7-M_{10} reset four nodes. After a rising edge in ϕ_c, the two inverters M_3-M_6 which are in positive feedback perform the decision. The two capacitors named C_N decrease the charge injection from the drains to the gates of M_1 and M_2 and hence reduce the kickback noise. They were realized as MOS capacitors of the same dimensions as M_1 and M_2 to ensure the proper matching. The outputs of this circuit are connected to an SR latch.

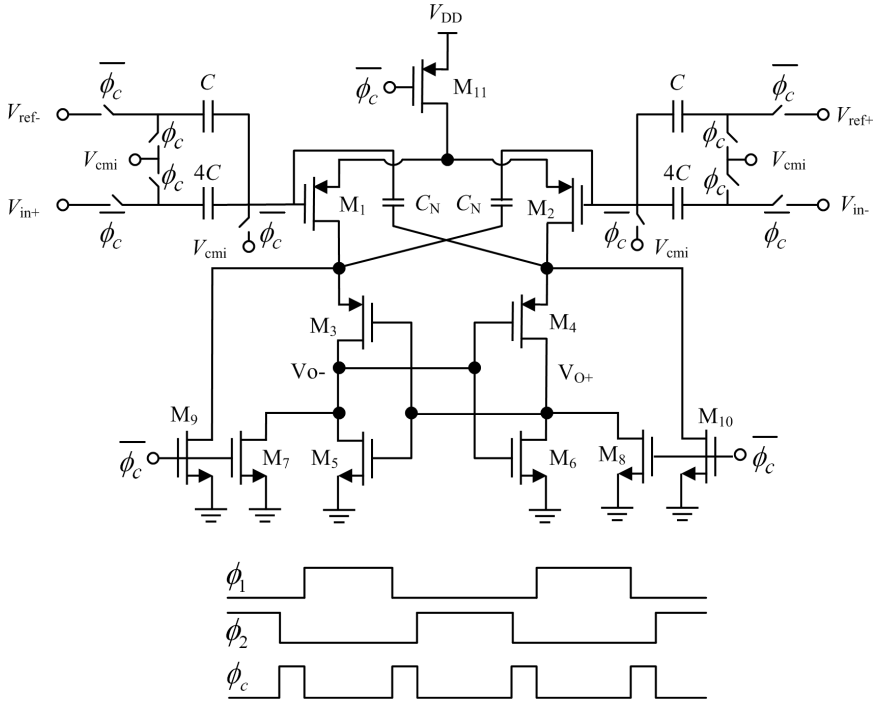

Fig. 6. Dynamic comparator and its timing diagram for the double sampling stages.

Each stage has two comparators which work in ϕ_c for double sampling stages based on the timing diagram shown in Fig. 6. For the next stages, the timing of the comparators is the same as that in conventional pipelined ADCs.

4. Simulation Results

The proposed ADC is simulated with HSPICE models of a 90 nm CMOS process with MIM capacitors. The full-scale input signal is 1 $V_{p-p,diff}$ and the supply voltage is 1 V. The simulation results show that the power consumption of the 10-bit 200 MS/s ADC is 30.9 mW and signal-to-noise plus distortion ratio (SNDR) is 58.5 dB and 56.8 dB at $(48/1024)\times 200$ MHz and $(480/1024)\times 200$ MHz, respectively. The output FFT plot for $f_{in} = 9.375$ MHz is shown in Fig. 7 where the circuit noise has not been considered.

The simulated spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), and SNDR are shown in Fig. 8 for sinusoidal inputs at frequencies spanning from

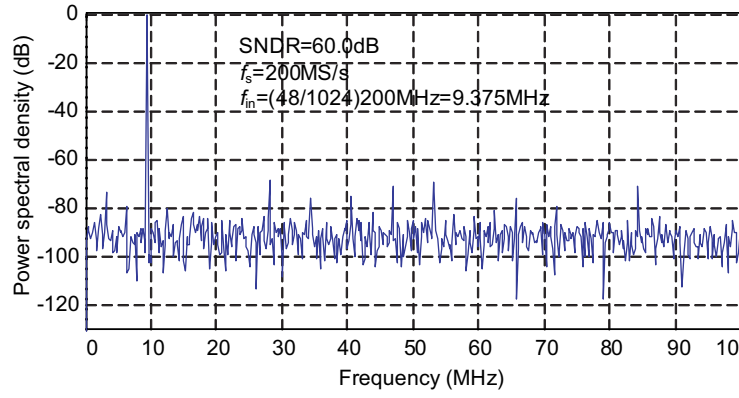

Fig. 7. FFT plot of the designed ADC at $f_{in} = 9.375$ MHz.

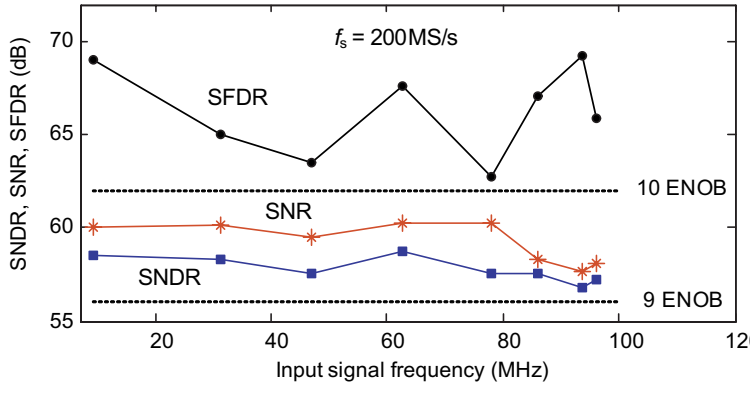

Fig. 8. Dynamic performance: SFDR, SNR, and SNDR versus input frequency.

9.375 MHz to 93.75 MHz. The achieved resolution based on SFDR is higher than 10-bit effective resolution and the resolution determined by SNR and SNDR lies above the 9 effective number of bits (ENOB) level. It is worth mentioning that the ADC resolution characterization is mainly determined by the application and in digital communication systems the ENOB is often characterized by SFDR rather than SNDR which actually determines the ADC linearity.

To have an estimation of the static performance of the ADC, a 10-bit 200 MS/s pipelined ADC was simulated by MATLAB/SIMULINK software. After the calculated voltage offsets resulting from the mismatches in the simulated comparators in 90 nm CMOS were applied to the ADC as Gaussian distributed random signals with $3\sigma = V_{\text{off}} = 30\,\text{mV}$, INL and DNL were plotted versus the output codes for a ramped input signal. As presented in Fig. 9, the peak DNL and INL are $-0.22\,\text{LSB}$ and $\pm 0.16\,\text{LSB}$, respectively.

The performance of the ADC has been checked in the different process corner cases under temperature variations spanning from -40°C to 85°C, and the worst case results (SS@85°C and FF@−40°C) are summarized in Table 1, in comparison with some recently reported pipelined ADCs. The comparison is based on a figure of merit defined as:

$$FOM = \frac{P}{2^{\text{ENOB}} \cdot f_s}\,. \tag{4}$$

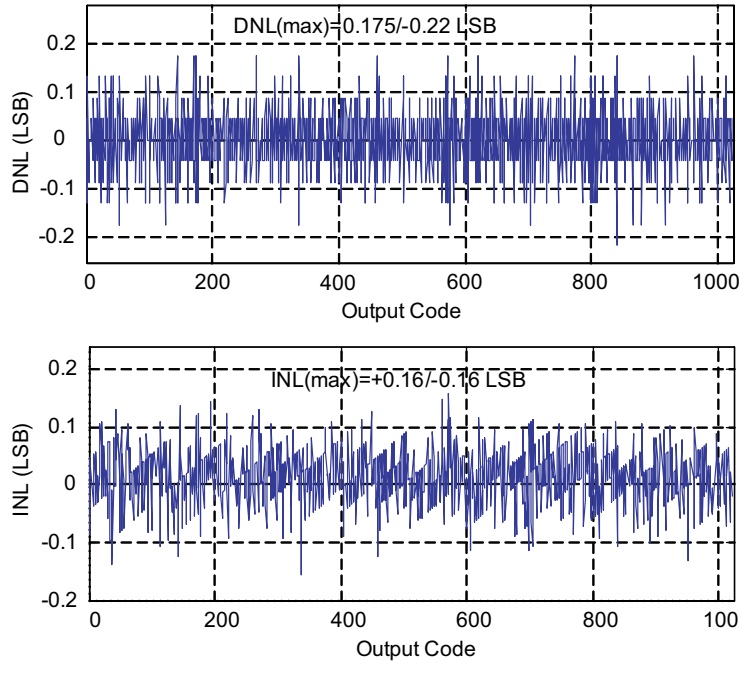

Fig. 9. Static performance: DNL and INL versus output code.

Table 1. Comparison with some reported ADCs.

Reference	Tech. (nm)	V_{DD} (V)	f_s (MSPS)	Power (mW)	SNDR (dB)	FOM (pJ/conversion)
4	90	1.2	200	55	54.4	0.64
5	90	2.5	40	25	56.5	1.18
15	90	0.5	10	2.4	48.1	1.15
16	65	1.2	800	30	44.2	0.28
This work (TT@27)				30.9	58.5	0.22
This work (SS@85)	90	1.0	200	27.8	55.9	0.28
This work (FF@−40)				33.8	56.5	0.31

The proposed ADC shows the lowest figure of merit, though its reported performance has been obtained by simulation. This comparison shows that the proposed architecture is an efficient way to decrease the power consumption in pipelined ADCs without any degradation in the ADC function or a remarkable increase in its chip area.

5. Conclusions

In this paper a low-voltage low-power 10-bit 200 MS/s pipelined ADC is presented. This ADC employs a new architecture combining two existent methods to reduce the power consumption in pipeline ADCs more efficiently. Since this ADC takes the advantages of both amplifier-sharing and double-sampling techniques, the capacitor scaling is efficiently applied along it, and the power consumption of the S/H amplifier is approximately halved compared to the conventional amplifier sharing. In addition, the ADC does not suffer from too much capacitances and switches which are added to ADCs using the double sampling technique. The power-efficient low-voltage amplifiers and dynamic comparators are also employed to achieve low-power and high performance. HSPICE simulation results for the 10-bit 200 MS/s ADC in a 90 nm CMOS process with 1 V supply voltage show 58.5 dB SNDR while consuming only 30.9 mW power.

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