

# A New Digital Background Correction Algorithm with Non-Precision Calibration Signals for Pipelined ADCs

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**Abstract**—A new digital background calibration algorithm for pipelined analog-to-digital converters is proposed in this paper. It is based on error estimation with non-precision calibration signals for foreground correction and a modified split structure for converting the foreground structure to the background one. This architecture allows improving the calibration signals accuracy contrarily to linear gain error coefficient, while the modified split structure does not need matching between the two channels. The presented algorithm is investigated in system level in MATLAB for a 12-bit pipelined ADC. It achieves an improvement equal to 36.5 dB and 44.5 dB for SNDR and SFDR, respectively where the input signal frequency is 39 MHz with a 100 MHz sampling frequency.

## I. INTRODUCTION

New generations of wireless communication systems highly demand for high-speed, high resolution, low-power and low-voltage analog-to-digital converters (ADCs). The Pipelined ADCs are the best candidate for resolutions between 10 to 16 bit and speeds between 15 MHz to 250 MHz [1]. Obviating these demands requires using deep-submicron CMOS technologies, while those will involve us with the constraints that result in a limited resolution for ADCs. Such phenomena are mostly arisen by three different sources: capacitor mismatch, finite amplifier dc gain, and nonlinear behavior of the gain stage. These problems are aggravated by shrinking the technology size because in scaled-down CMOS, the transistor intrinsic gain ( $g_m r_{ds}$ ) and matching between the circuitry components decrease considerably. So, the digital calibration techniques have been presented for palliating the ADC constraints that can reduce the power consumption and relax the amplifier design process [1]–[7]. Also, the calibration process in digital domain is very interesting because digital circuits are fast and reliable in CMOS nano technologies. The digital calibration algorithms are majorly classified into two categories of foreground and background techniques. The foreground calibration interrupts the conversion of the input and enters the ADC into the calibration mode. On the other hand, the background calibration scheme doesn't interrupt the conversion of the input signal; rather the calibration and digitization processes are done at the same time.

A 12-bit pipelined ADC is shown in Fig. 1(a). It includes twelve 1.5-bit stages where its  $i$ -th stage is sketched in

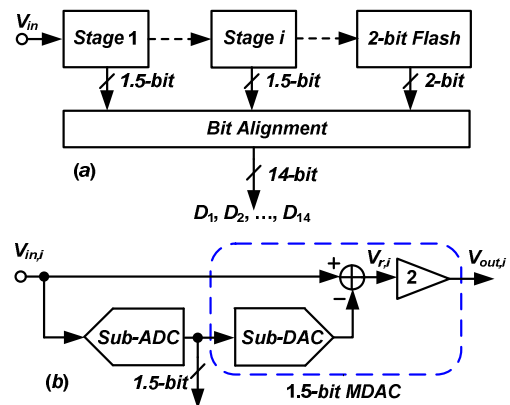


Figure 1. (a) 12-bit pipelined ADC architecture, (b) 1.5-bit gain stage.

Fig. 1(b) and also consists of a two-bit flash ADC, producing digital outputs as  $D_1, D_2, \dots, D_{14}$ . Since the gain of each stage is not exactly equal to 2, a total of 13 stages are required to achieve 12-bit resolution. We do not have the front-end SHA circuit in this structure because of the additional noise and power consumption which it imposes to the circuit. Eliminating of SHA could be compensated by time matching technique between the MDAC and sub-ADC paths [2].

This paper presents a new digital background calibration algorithm for 1.5 bit per stages pipelined ADCs. It utilizes the LMS algorithm to estimate the error coefficients and improves the calibration signals accuracy contrarily to the gain error coefficient ( $\alpha_1$ ). In addition, a modified split structure is proposed for changing the foreground algorithm to the background one.

## II. CALIBRATION ALGORITHM IN FOREGROUND MODE

### A. LMS-Based Algorithm

Figure 2 shows the ADC structure in the calibration mode where the first stage non-idealities are modeled by a fifth-order polynomial,  $f_5(\cdot)$ , and the other stages are assumed to be ideal. In this figure,  $V_{r1}$  is the residue voltage of the first stage,  $V_{d1}$  is its distorted value,  $V_{out1}$  is the stage analog output and  $D_{r1-desired}$ ,  $D_{d1}$  and  $D_{out1}$  are their digital values, respectively. The input of the first stage is connected to the ground and a two level dither signal,  $PN$ , is injected into the



created as the studied procedure is repeated for the stages three and four. So, if sub-DACs in the second and third stages use the same voltage levels as the sub-DAC of the first stage, for an extra DAC added to the third stage, the value of  $D_{r1-desired}$  will be equal to 110111111111 when the value of  $V_i$  is  $3V_{Ref}/8$ . Similarly, if sub-DACs in second, third and fourth stages utilize the same voltage levels as sub-DAC of first stage does when an extra DAC is added in fourth stage, the value of  $D_{r1-desired}$  will be 111011111111 and the value of  $V_i$  is  $7V_{Ref}/16$ . The considerable constraint of the method is the error term at under calibration stage shouldn't have any effect on the next three stages. That is because of changing in 1.5-bit outputs of the stages can distort the effect of extra DACs.

### III. BACKGROUND CALIBRATION METHOD

Setting parameters of an ADC would change during its normal operation where the temperature variation is among the most significant. Tracking these variations requires the calibration process working continuously. It means that the background calibration is undeniable. There are a few structures that are recommended for changing foreground methods to their corresponding background versions [2]–[7]. The interpolation method that has been widely used, suffers from delay between sampled input signal and its associated digital output [2], [3]. Therefore this conventional method is not suitable for high speed applications. The split structure also has matching problem between the channels [4], [5]. The nested structure needs the extra power and area consumption for reference ADC [6]. Also, queue-based structures suffer from extra and fast phases [7]. Therefore a new method is proposed that not only changes foreground structures to the background one but also solves some of the previous mentioned problems.

Figure 4 shows the block diagram of the proposed method for changing the foreground calibration to a background algorithm by modifying the split structure. For selecting one of two channels for calibration, we use two random one bit signals. The difference between this structure and the conventional split structure is that it does not require matching between channels (except same delay of channels). Because, each of the channels will be calibrated independently, so the differential signal will not be used in the proposed structure.

There are three major operation phases for ADC in calibration mode: (1) the analog input voltage would be converted using both of the channels where non of them is in the calibration mode, (2) the first channel is in the calibration mode where the input will be converted by the second channel, and (3) the second channel is in the calibration mode where the input will be converted by the first channel. For specifying percent of these phases, we can utilize MSE criterion between the output of an ADC with 12-bit resolution and the output of the proposed structure. Figure 5 shows the value of MSE to different input frequency and different rate of operational phases. This simulation shows that if phase 1 has more than 90% and any of phases 2 and 3 has 5% of the calibration mode; the effect of rising noise floor can be reduced up to the 6 dB, by eliminating one of the two

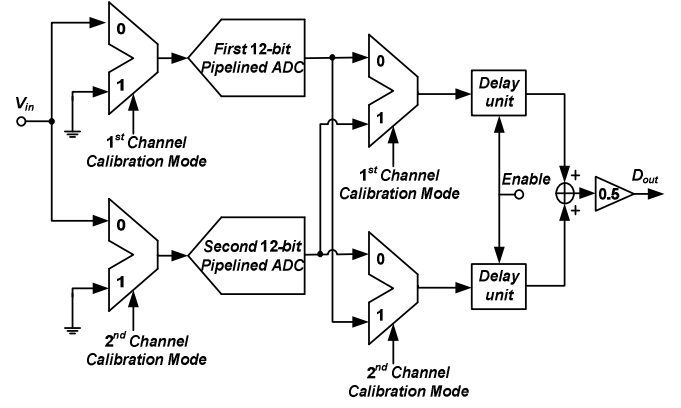


Figure 4. Background calibration by using a modified split structure.

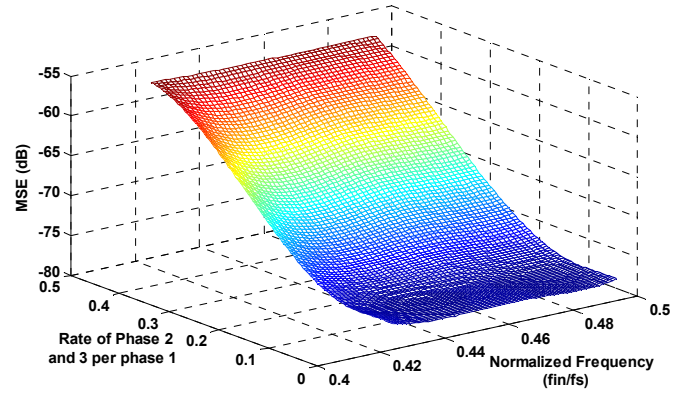


Figure 5. MSE of digital output at variable input frequency and different percent of operating phases .

channels. Indeed, the necessary number of samples for calibration would be increase with larger percent of phase 1. The MSE is defined as:

$$MSE = \frac{1}{N} \sum_{n=1}^N |D_{one-channel} - D_{split}|^2 \quad (6)$$

where  $D_{one-channel}$  is the output of ADC with 12-bit resolution and  $D_{split}$  is the output of the proposed modified split structure.

Delay in producing outputs would be solved in this structure. But, there exist a considerable problem of tuning delays of channels in order to create the output of both channels at the same time. However, it can be solved by using delay units which would send the outputs of the channels into the output of the structure by a controllable signal.

### IV. SIMULATION RESULTS

The proposed digital background calibration algorithm which is implemented by the proposed Error estimation method is applied to a 12-bit pipelined ADC which is composed of twelve 1.5-bit stages and one 2-bit flash ADC as the final stage. The error parameters in all of the first twelve stages are  $\alpha_1=0.04$ ,  $\alpha_3=0.06$  and  $\alpha_5=0.12$  where the calibration algorithm is applied only to the first six stages. In fact, the proposed method signals is imposed to the first four stages

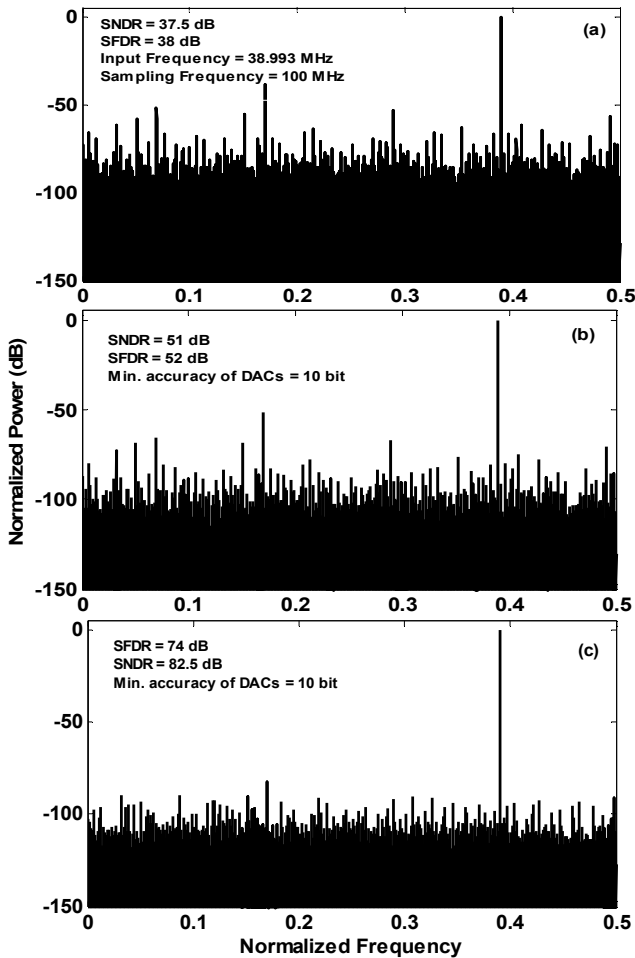


Figure 6. Power spectral density of ADC digital output (a) without calibration, (b) calibrated without the proposed method, (c) calibrated with the proposed method.

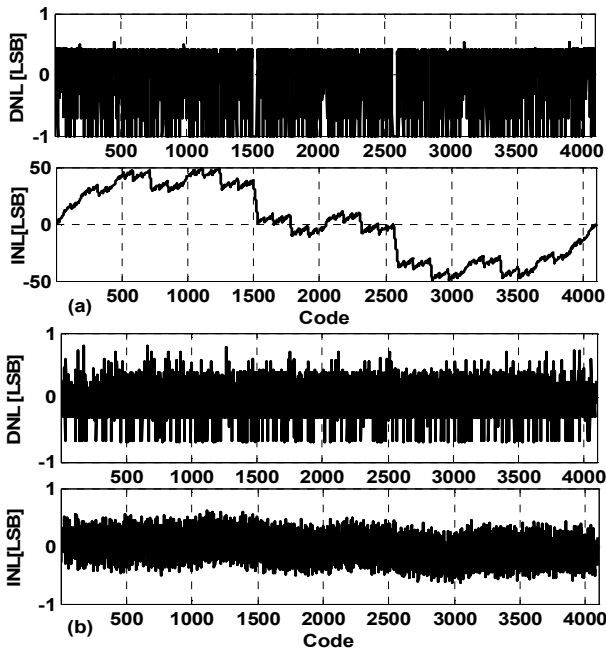


Figure 7. DNL and INL plots (a) without calibration, (b) with the proposed method.

and the other two stages use the normal DACs. The proposed converter has been simulated in MATLAB platform with and without calibration algorithm where the power spectral densities (PSD) of the converter's output for any of these settings are shown in Fig. 6. Also, the PSD is sketched for calibrated ADC with and without proposed method in Figs. 6(b) and 6(c). In these plots, the conventional DAC accuracy is assumed to be 10 bit. The important operation specifications like SNDR and SFDR were 37.5 dB and 38 dB in non-calibrated ADC and they are improved to 51 dB and 52 dB after calibration where the nonsufficient accuracy of DACs limits them. However, SNDR and SFDR improve to 74 dB and 82.5 dB, respectively by adding the proposed error estimation to the calibration algorithm. The sampling frequency was 100 MHz with 39 MHz input signal. The necessary number of samples for the calibration of the one stage is  $2^{13}$  samples and the total calibration time is 491.52  $\mu$ sec. The other important specifications of ADC are DNL and INL errors. As seen in Fig. 7(a), there so many missing code in output of ADC, but, after calibration DNL  $< \pm 0.8$  LSB shows that there are no missing codes. Also, the maximum value of INL after calibration is  $\pm 0.6$  LSB.

## VIII. CONCLUSIONS

A new digital background calibration algorithm for pipelined analog-to-digital converters was proposed. It is based on error estimation with non-precision calibration signals for foreground calibration and a modified split structure for background calibration. The usefulness of the presented algorithm was demonstrated in system level with MATLAB for a 12-bit pipelined ADC.

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