A VERY LOW-NOISE LOW-POWER INTEGRATOR FOR HIGH-RESOLUTION ΔΣ MODULATORS

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ABSTRACT

In this paper a very low-noise low-power correlated double sampled integrator has been presented. For attenuating the sampling thermal noise, two large capacitors are well incorporated in the integrator with no using large sampling and integrating capacitors that are necessary in ordinary integrators. The integrator is used in the front-end of a 24 bit, forth-order single-loop single-bit Delta-Sigma modulator with a bandwidth of 1000 rad/s. A fully differential class AB op-amp with a preamplifier is designed with gain of 85dB, bandwidth of 12 Mrad/s and overall input referred noise floor of –171dB without the need for large compensation capacitors as in the ordinary topologies are used. The integrator power consumption is only 2.8 mW with a single 3.0V supply in 0.6-μm CMOS technology.

1. INTRODUCTION

For low frequency, very high-resolution applications such as industrial control process, biomedical instrumentation and remote seismic monitoring, single-loop single-bit high-order Delta-Sigma (DS) modulators are the most suitable analog to digital converters due to their tolerance to the circuits imperfections, inherent linearity and reduced antialiasing filtering requirements [1][2].

In a proper design of high-order single-bit DS modulators, the major constraint issue to obtain a very high resolution is the front-end integrator noise including input switches thermal noise and flicker and thermal noise of its op-amp. For this reason and the linearity constraints, the major power consumption (about more than 35%) of a high resolution DS modulator is due to the first integrator [1][2]. In order to achieve a 24-bit resolution in the 1000rad/s bandwidth, a fully differential modulator requires sampling capacitors in the order of 900pF in the first integrator. This consequently in ordinary integrators leads to a very large area and power consumption in the first op-amp. Using four off-chip capacitors for the first integrator still requires high power consumption and also causes the matching and parasitic capacitance problem.

In the proposed CDS (correlated double sampling) integrator two large capacitors are well embedded to strongly attenuate the input sampling noise without using any large sampling or integrating capacitors. Also using these large capacitors doesn't cause the matching and parasitic capacitance problem. Therefore, it can be easily designed with a little power and area consumption. Moreover, it uses a combination of a preamplifier with a one-stage class AB op-amp to reduce the size of compensation capacitors.

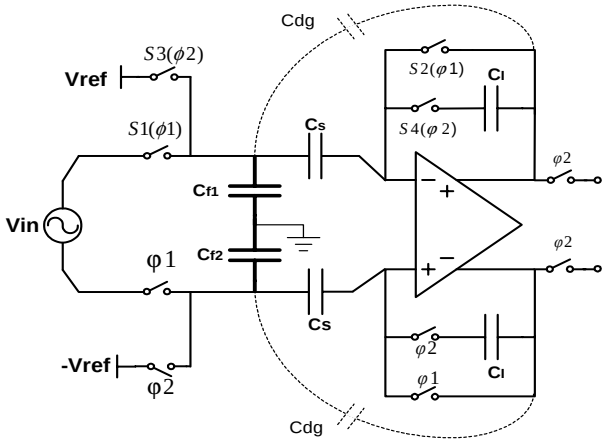

Figure 1. The proposed very low-noise CDS integrator with the small sampling and integrating capacitors.

2. INTEGRATOR CONFIGURATION

For the fully differential SC DS modulator with the front-end integrator, signal to noise ratio is given by [3]:

$$SNR = 10\,Log\left(\frac{0.5\,(2\cdot OL\cdot Vref)^2}{\gamma\cdot kT/(C_f\cdot OSR)}\right) \qquad (1)$$

where OL, OSR and γ denote the overload factor, the oversampling ratio and the sampling noise coefficient depending on the number of the contributing capacitors in the input referred sampling noise respectively. Equation (1) shows that with an overload factor of about –1.24dB, OSR of 1024 and γ = 3, a C_f equal to 900pF satisfies 24-bit resolution. Also in equation (1) it is assumed that the op-amp's thermal noise is as low as possible, below –171dB, to satisfy 24-bit resolution in a bandwidth of 1000 rad/s [3]. Moreover the CDS technique attenuates strongly op-amp's 1/f noise and offset. By using old CDS integrators such as the integrators used in [1] and [2], the equation (1) obliges to use very large sampling capacitor to keep sampling noise below desired level. So, the integrating capacitor will be large due to the desired integrator gain. In our case, keeping

the input referred noise floor at a very low level (–171dB), leads to use a large sampling capacitor (900pF) and consequently a large integration capacitor. Due to the very large amount of area and power consumption, it will be an un-optimized to use such integrator structures.

In the proposed integrator architecture, shown in Fig. 1, for solving the sampling (*KT/C)* noise problem, two large capacitors (C_{f1} & C_{f2}) are well incorporated to decrease the noise of the input switches as much as needed. They are well suited where all switches that contribute major sampling noise meet them in their equivalent RC. The input referred sampling noise in this configuration is $\gamma KT/C_f$ rather $\gamma KT/C_S$ in ordinary integrators. Therefore there is no need to use large sampling and integrating capacitors for attenuating the sampling noise.

Moreover C_{f1} & C_{f2} can be off-chip capacitors with no matching and parasitic problem. The parasitic capacitors due to pads are in parallel with the input or the voltage references and clearly have no effect. For attenuating the effects of the offset and 1/*f* noise, CDS is also used in this integrator. The small 'deglitching' capacitors (Fig. 1), i.e. Cdg, are incorporated to prevent glitches in the output when the feedback is open during the non-overlapping clock phases [4].

3. SWITCHES NOISE

A precise analysis for switches and op-amp's noise power spectral density (PSD) transfer functions is performed. If S1NTF, S2NTF, S4NTF and OPNTF represent the switch S1, S2, S4 and input referred op-amp's noise PSD transfer functions (in Fig. 1), respectively, the analysis shows:

$$S1NTF(z)=\left(\frac{-K}{1+\frac{1+K}{A}-(1+\frac{1}{A})z^{-1}}\right)^2 \quad (2)$$

$$S2NTF(z)=\left(\frac{\frac{-K}{1+A}}{1+\frac{1+K}{A}-(1+\frac{1}{A})z^{-1}}\right)^2 \quad (3)$$

$$S4NTF(z)=\left(\frac{z^{-1}-1}{1+\frac{1+K}{A}-(1+\frac{1}{A})z^{-1}}\right)^2 \quad (4)$$

$$OPNTF(z)=\left(\frac{1+K\frac{-Kz^{-1/2}}{1+1/A}-z^{-1}}{1+\frac{1+K}{A}-(1+\frac{1}{A})z^{-1}}\right)^2 \quad (5)$$

where $K=C_S/C_I$ and A represents the finite open-loop gain of the integrator's op-amp.

From the equations (3) and (4), it is clear that the switches S2 and S4 have no significant effect on the total output noise PSD of the integrator while the input switch S1 does. The behavior of input switch S3 is as same as S1. The contribution of the op-amp thermal noise on the total output noise PSD is significant because of its fold-over component. As it is seen by the equation (5), the CDS technique is not an efficient technique for reducing op-amp's thermal noise. The output PSD of the integrator resulting from the switch S1, S2, S4 and the op-amp thermal noise is shown in Fig. 2. The plotted result confirms the above discussion. As a result, a very low noise op-amp is designed with a minimum allowable bandwidth for reducing its contribution on the overall noise PSD. The equation (5) also shows that CDS power transfer function places double zeros at DC frequency that cancels out the offset and substantially attenuates the *1/f* noise components of the integrator's op-amp. The comparison between this integrator output with an ordinary integrator output for 1/f noise input shown in Fig. 3 confirms this claim.

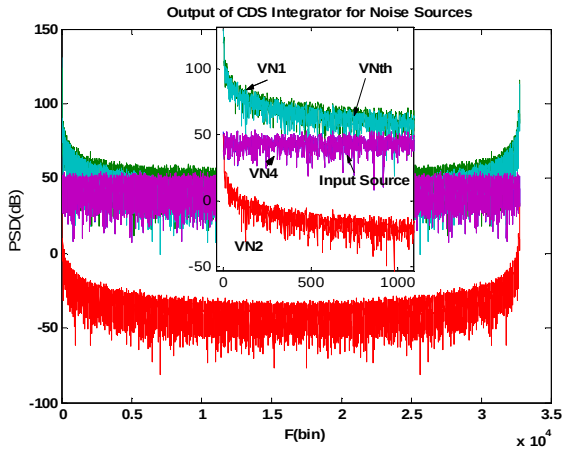

Figure 2. The contributions of different sources in the output noise PSD of the integrator shown in Fig. 1. For each case, the normalized noise source is chosen.

From the above discussion, it is clearly seen that the major constraint is thermal noise that leads to use a large input capacitors (C_f) and also a low noise op-amp in the integrator.

4. SETTLING NOISE

The settling noise in the sampling and integrating phases due to the resistance of switches, the finite DC gain, bandwidth and the slew-rate of the op-amp can be a big constraint in a very high-resolution application.

Fig. 4 demonstrated the equivalent model of the integrator of Fig. 1 in the sampling and integrating phase for settling analysis. In the high-resolution applications, the integrator is forced to settle in fast regime wherein the settling time constant,τ, is smaller than an upper limit, and the slew-rate, S, is larger than a lower limit [5]. Using class AB configuration for the op-amp guaranties that the slewing never occurs and the settling process is linear. Assuming the open loop transfer function of the op-amp as a single pole response of the form $A(j\omega)=\frac{A_0}{1+j\omega/\omega_{-3dB}}$, input voltage is

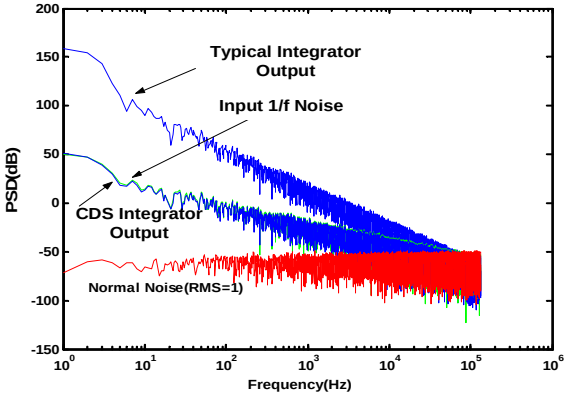

Figure 3. The comparison between the proposed integrator output with an ordinary integrator output for flicker noise input.

sampled on capacitor C_S in the sampling phase with the transfer function of:

$$\frac{V_{Cs}}{V_{in}} = 1 - \frac{j\omega\left(R_{on1}+\frac{R_{on1}+R_{on2}}{A_0}\right)C_S - \omega^2\left(\frac{R_{on1}+R_{on2}}{\omega_{-3dB}A_0}\right)C_S}{1+\frac{1}{A_0}+j\omega\left(\frac{\frac{1}{\omega_{-3dB}}+R_{on2}C_S}{A_0}+R_{on1}(C_S+C_f)(1+\frac{1}{A_0})\right)-B_1(\omega^2)-B_2(\omega^3)} \quad (6)$$

$$\cong 1-\frac{j\omega R_{on1}C_S}{1+j\omega\left(R_{on1}C_f+\frac{1}{\omega_t}\right)}$$

where ω_t , K and β_x (ω) are the op-amp unity gain bandwidth, Integrator gain and a function of frequency respectively.

In the integrating phase, the transfer function from the last sampled voltage on C_f and reference voltage to the output are:

$$\frac{V_{Out}}{V_C} = \frac{-K(1+j\omega R_{on4}C_I)(1+j\omega R_{on3}C_f)}{1+\frac{1}{A_0}+j\omega\left(R_{on3}(C_S+C_f)(1+\frac{1}{A_0})+\frac{1+K}{A_0\,\omega_{-3dB}}\right)-B_3(\omega^2)-B_4(\omega^3)} \quad (7)$$

$$\cong \frac{-K(1+j\omega R_{on4}C_I)(1+j\omega R_{on3}C_f)}{1+j\omega\left(R_{on3}C_f+\frac{1}{\beta\omega_t}\right)} \qquad A_0, \frac{C_f}{C_S} >> 1$$

$$\frac{V_{Out}}{V_f} = \frac{-K(1+j\omega R_{on4}C_I)}{1+\frac{1+K}{A_0}+j\omega\left(R_{on3}(C_S+C_f)+\frac{1+K}{A_0\,\omega_{-3dB}}+B_5\right)-B_6(\omega^2)-B_7(\omega^3)} \quad (8)$$

$$\cong \frac{-K(1+j\omega R_{on4}C_I)}{1+j\omega\left(R_{on3}C_f+\frac{1}{\beta\omega_t}\right)} \qquad A_0, \frac{C_f}{C_S} >> 1$$

where β is the feedback factor. It is apparent from equations (6), (7) and (8) that in the two phases, the equivalent time constant is due to the input equivalent *RC* and also the unity gain bandwidth of the op-amp. Even though making use of the fully differential approach significantly reduces the error of the settling time because of the linear settling, the signal source input resistance should be kept as low as possible and also large-size input switches should be used. Moreover, the inverse of the equivalent time constant of the op-amp should be at least six times of the sampling frequency.

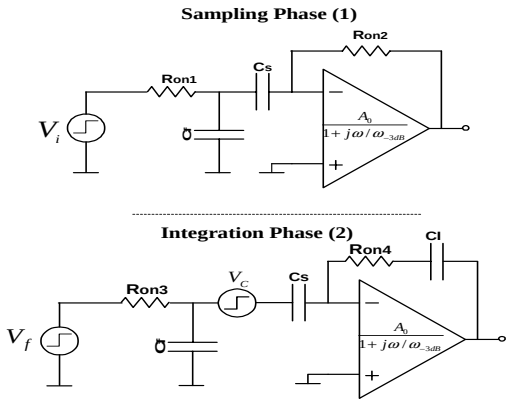

Figure 4. The simplified transient models of the integrator shown in Fig. 1 in the sampling and the integrating phases.

5. OP-AMP CONFIGURATION

As discussed in pervious sections, the op-amp for the integrator should have noise level below -171dB and also the maximum bandwidth of $\omega_t \approx 6 \cdot OSR \cdot (2\omega_b)$ where ω_b is the input signal bandwidth of the DS modulator. Considering noise and the bandwidth of the op-amp, designing such an op-amp with a little power and area consumption is a difficult task because of a very large compensation capacitance needed to reduce the amplifier bandwidth. The merits of two-stage and single-stage amplifier topologies are examined. The unity gain bandwidth of conventional compensated techniques of a two-stage and a single-stage op-amp shown in Fig. 5 are about g_{m1}/C_{Out} and g_{m1}/C_C respectively. Assuming that the thermal noise of the op-amp is dominated by the noise of its input differential-pair transistors, the desired very low noise op-amp requires a very high input transconductance (g_{m1}). As a result, achieving a minimum allowable unity gain bandwidth demands a very large compensation capacitor C_c and C_{out} in the conventional two-stage and single-stage topologies respectively. Doing the same calculation as in equation (1), for the op-amp used in the first integrator of a 24-bit modulator having a bandwidth of 1000rad/s results in a compensation capacitor of about 1000pF.

Adding a preamplifier to the main op-amp to achieve these specifications with a small compensation capacitor seems to be an attractive option. The idea of adding a low gain preamplifier is used in [6] for a high-speed low-power example. Besides, a cascode stage used there cannot be a good candidate for our application because of its limited output swing, the compensation topology and the non-

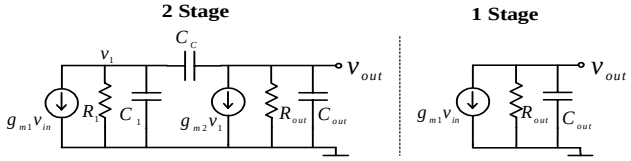

Figure 5. The simplified equivalent small-signal models for a single-stage and a two-stage conventional op-amps.

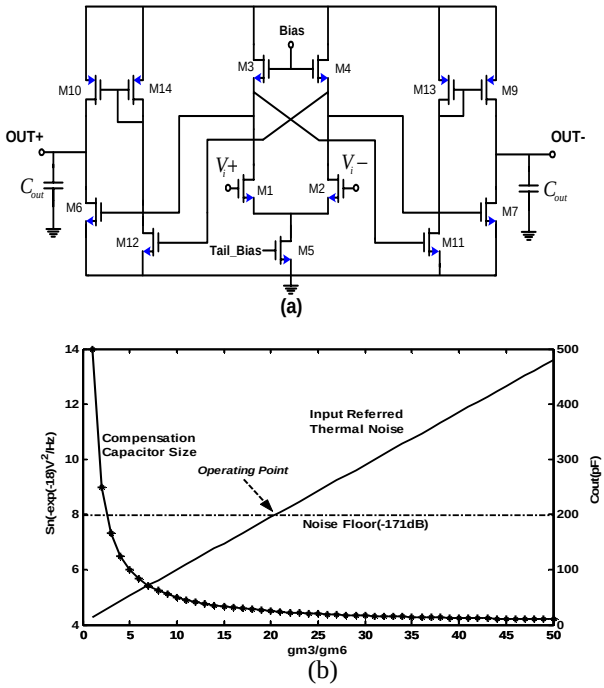

Figure 6. (a) The proposed fully differential class AB op-amp (b) The size of its compensation capacitor and input referred thermal noise floor vs. g_{m3} / g_{m6}.

linearity coming from its slew-rate limitation effect. Taking into account the above requirements and issues, a viable solution is to use a single-stage class AB op-amp with a moderate gain preamplifier and using the output capacitance for the compensation as shown in Fig. 6(a) for this really two-stage op-amp. The unity-gain bandwidth of this op-amp is approximately given by:

$$\omega_t \cong 2\frac{g_{m1} \cdot g_{m6}}{g_{m3} \cdot C_{out}} \qquad (9)$$

Targeting a very low thermal noise op-amp imposes a very high input transistor transconductance (g_{m1}). However equation (9) shows that the compensation capacitor can be decreased with the gm_3/gm_6 factor proportionally. Also, increasing gm_3/gm_6 increases the total input referred thermal noise as shown in Fig. 6(b). Taking into account the contribution of M1, M3 and M6 in the overall thermal noise, g_{m3} is chosen 20 times bigger than g_{m6} to allow the reduction of the compensation capacitor proportionally and to set the operating point at the corner of the limited noise floor shown in Fig. 6(b). It can also be observed that the reduction of the compensation capacitor happens in the expense of reduction in the achievable dc-gain. To improve the dc-gain, the output resistance should be increased by using long channel transistors in the output stage of the main amplifier. A low quiescent current in the output branch is also required. Due to the low-frequency low-power feature required in our application, the input transistors M1 and M2 are operating near the subthreshold region [7]. Noise on the bottom supply tail appears as a common-mode input to the second stage of

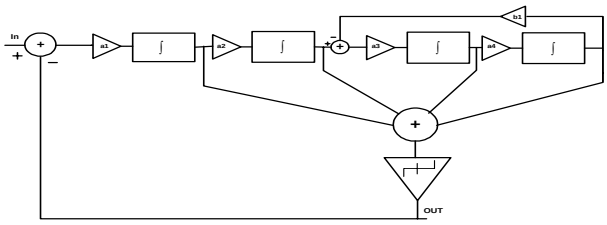

Figure 7. The modulator used for the 24-bit resolution.

the op-amp and is thus attenuated by the common-mode rejection of that stage. Also using the class AB configuration in our work guaranties that the slew-rate never occurs and the settling process is linear.

6. SIMULATION RESULTS

The proposed CDS integrator is used in the front-end of the single-loop single-bit forth-order DS modulator shown in Fig. 7. Taking into account most of the non-idealities, exhaustive behavioral simulations that are close models of HSPICE simulations are performed. After behavioral simulations in MATLAB, HSPICE transistor level simulations of the circuit level of Fig. 7 have been performed in a 0.6 μm process using reference voltage of 3.0V. The modulator has a signal to noise ratio of 144 dB with a bandwidth of 1000 rad/s [3]. The power consumption of the whole modulator is about 8.5mW while the first integrator only consumes 2.8mW.

7. CONCLUSION

This paper presents a very low-noise, low-power low-area CDS integrator used in the front-end of a forth order modulator to achieve 24 bit resolution in a bandwidth of 1000 rad/s. The integrator has a very low noise op-amp, -171dB, with no need to large sampling and integrating capacitors. Using a single-stage class AB configuration with a moderate gain preamplifier enables us to achieve 85dB DC gain in a bandwidth of 12Mrad/s with an only 50pF compensation capacitor.

8. REFERENCES

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