A Third-Order noise-shaping SAR ADC With Optimized NTF Zeros for IoT Applications

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***Abstract*— This article presents a fully dynamic, simple, and area-efficient third-order noise shaping successive approximation register analog to digital converter (NS-SAR ADC) that is suitable for the internet of thing (IoT) applications. This work utilizes a passive integrator in the feed-forward (FF) path of a second-order error-feedback (EF) NS-SAR ADC to enhance its in-band quantization noise suppression effect. This integrator is very simple and area-efficient because built just with a switch and a capacitor. Integrator attenuation arising from charge-sharing is compensated with embedded comparator relative gain of 4. The noise transfer function (NTF) zeros are optimized. In this work sampling frequency, bandwidth, and over-sampling ratio (OSR) are 3.2 MS/S, 200 kHz, and 8 respectively. The proposed structure is investigated systematically by MATLAB software. Using the proposed technique, a 3rd order NS-SAR ADC is obtained and the signal to noise and distortion ratio (SNDR) of the ADC is enhanced from 94.7dB to 104.3dB.**

***Keywords*— SAR ADC, Noise-Shaping, NTF zeros optimization, EF-filter, FF, Passive integrator.**

I. Introduction

The successive approximation register analog to digital converters (SAR ADCs) is the right choice for low power medium resolution applications. But for High resolution, low-power applications like the Internet of Things (IoT) sensors, SAR ADCs aren't appropriate because of their limited resolution. On the other hand, Sigma-Delta (SD) ADCs have high resolution caused by noise shaping (NS) property. But this kind of ADCs uses power-consuming operational trans-conductance amplifiers (OTAs) that make them not to be suitable for low power cases. So in recent years, the SAR ADC structure has been modified to be equipped with NS effect which increases its resolution.

Noise-shaping ideas in the NS-SAR ADCs are almost like Sigma-delta ADCs. By noise-shaping, the in-band SAR ADC's quantization and comparator noise can be shaped out of the band. There are several advantages of NS-SAR ADCs over SD ADCs. Firstly using the same DAC array for both quantization and feedback in NS-SAR ADC, alleviates the circuit complexity. Secondly, its conversion residue is small and accessible on the DAC at the end of the SAR operation which relaxes the loop filter linearity and design issues. This type of ADCs is OTA free leading to power efficiency.

A 1st-order high-pass filtered NS-SAR ADC using a passive switched capacitor (SC) integrator has been proposed in [1-2]. Another 1st-order NS-SAR ADC is based on the error-feedback (EF) method reported in [3-5]. Although these structures are simple and have low power, their noise suppression effect is weak. In [6] an energy-efficient noise-shaping SAR ADC has been presented that uses a dynamic amplifier (DAMP) to compensate gain attenuation of a dynamic finite impulse response- infinite impulse response (FIR-IIR) filter. So it improves the noise shaping effect of the ADC. In [7] a 2nd order NS-SAR ADC has been reported which applied the EF structure to realize optimized noise transfer function (NTF) zeros. So it improves the NS effect with little moderation to a classic SAR. It achieved a low-power scaling-friendly EF path by utilizing a passive FIR filter. In this structure, the comparator is used as both comparator and dynamic amplifier in two different phases. It is insensitive to process voltage temperature (PVT) variations as its NTF depends on the capacitor ratios value, not on their absolute values. However, this structure has a limited quantization noise suppression effect in low frequencies. In [8] a passive NS structure for SAR ADC has been suggested which employed the two-step integration with passive gain and comparator gain methods. Although using comparator input transistors scaling to obtain high gain, can increase the thermal noise, it is a low power method to achieve the required gain resulting in NS enhancement. Another way to get passive gain is by adding integration capacitors with opposite polarity in series with comparator input as [9]. In this structure two capacitors preserving the residue voltage act in a ping-pong way. They connect between the top plates of the DAC arrays, helping as attenuation. When the conversion finishes, the capacitors get the final residue with an opposite polarity which makes a passive gain of 2 for differential residue voltage. [10] reported a second-order fully passive NS SAR ADC using passive SC integrator and a 3-path comparator which provides a gain of 4 and 16 for a feed-forward path. However, this increases the thermal noise of the comparator.

In this work, we propose a 3rd order NS-SAR ADC using combined error-feedback and feed-forward (FF) methods to suppress in-band quantization and comparator noise and especially low-frequency noise to improve the resolution of the ADC. The rest of the paper is organized as follows. Section II explains the proposed NS-SAR ADC and its analysis. Section III presents the MATLAB simulation results and finally, Section IV concludes the paper.

II. Proposed 3rd order NS-SAR ADC system

A. System overview

Fig. 1 depicts the architectural block diagram of the proposed 3rd order EF-FF NS-SAR ADC. As shown in this

figure, our structure has two added filters compared with the classic SAR ADC. $H_1(z)$ is a second-order FIR EF-loop filter. $H_2(z)$ is a FF-loop filter to enhance the in-band noise suppression, especially at low frequencies. $V_{res}(z)$ is the residue voltage of the ADC, that is available on the top plate of the CDAC at the end of the SAR conversion operation. We use a two-path comparator to provide a gain of 4 for the FF-filter path.

Our work pursues the DAMP-assisted EF manner [6-7], [11] to implement the 2nd-order EF-filter ($H_1(z)$). The EF summation implements charge-sharing among FIR-capacitors and DAC capacitors, which is low power and simple. However, it is accompanied by voltage attenuation that is compensated using DAMP gain (G). Moreover, the presence of the DAMP let us use rather small FIR capacitors resulting in a small area overhead.

In Fig. 1 γ, β_1 and β_2 are charge-sharing coefficients. Although these coefficients in the EF path are compensated by DAMP gain, their attenuation effect on input signal ($V_{in}(z)$) amplitude remains. So, input signal amplitude reduction is represented by a coefficient of (1- β_1- β_2) at the ADC input path.

Another part of the proposed structure is FF-filter ($H_2(z)$) which is implemented by a passive SC integrator. The aim of adding this part is to enhance noise suppression at low frequencies which is a problem in [7]. $H_2(z)$ is a passive, low-power integrator that is consisted of a switch and a capacitor. The pole of the integrator is the zero of the NTF of the system. So we implement this pole as near to z=1 as possible to enhance noise attenuation at DC and low frequencies.

(1- α) is the attenuation factor of the integrator amplitude which arises from charge-sharing between DAC and integrator capacitor. α represents the pole of the integrator that deviates from z=1 due to charge sharing attenuation. b is a passive gain that is constructed by comparator input transistors ratio. So this structure needs a two-path comparator. It is noteworthy, this comparator just provides a gain of 4 that compared to [10] is a small gain. Also, we will see the comparator noise will be 3rd order shaped. So added thermal noise of the comparator arising from the second path is not significant.

B. *Analysis and design of the proposed structure*

As for Fig. 1, the input-output equation of the system can be obtained as:

$$V_{out}(z) = V_{in}(z) + \frac{1 - H_1(z)}{1 + H_2(z)} \cdot Q(z) \tag{1}$$

from (1) signal and noise transfer function are:

$$\begin{cases} STF(z) = 1 \\ NTF(z) = \dfrac{1 - H_1(z)}{1 + H_2(z)} \end{cases} \tag{2}$$

the zeros of 1-$H_1(z)$ and pole of $H_2(z)$ construct the NTF zeros. As shown in Fig. 1 we can extract $H_1(z)$, $H_2(z)$, STF(z), and NTF(z) with more details as below:

$$H_1(z) = G_1.(\beta_1.z^{-1} - \beta_2.\gamma.z^{-2}) \tag{3}$$

$$H_2(z) = b.z^{-1}.\left[\frac{(1-\alpha)}{1-\alpha.z^{-1}}\right] \tag{4}$$

$$STF(z) = 1 - \beta_1 - \beta_2 \tag{5}$$

$$NTF(z) = \frac{(1-\alpha.z^{-1})(1 - G_1.\beta_1.z^{-1} + G_1.\beta_2.\gamma.z^{-2})}{1 - (\alpha - b(1-\alpha)).z^{-1}} \tag{6}$$

We present a 3rd-order NS-SAR ADC with optimized zeros. The optimum location of the zeros in an oversampling ADC can be get from the Scherier [12]. According to it, the optimum zeros frequency for a 3rd order NS-ADC is:

$$\frac{f_1}{f_s} = 0; \quad \frac{f_{2,3}}{f_s} = \pm\sqrt{\frac{3}{5}}.\frac{f_b}{f_s} = \pm\sqrt{\frac{3}{5}}.\frac{1}{2 \times OSR} \tag{7}$$

where f_1 and $f_{2,3}$ are the frequency of the 3 zeros. f_b is the bandwidth of the ADC and f_s is the sampling frequency of the ADC. On the other hand, the relation among optimum zeros location and their frequency is:

$$z_{opt} = e^{j2\pi\frac{f_{opt}}{f_s}} \tag{8}$$

So from (7) and (8), the optimum zeros location obtained:

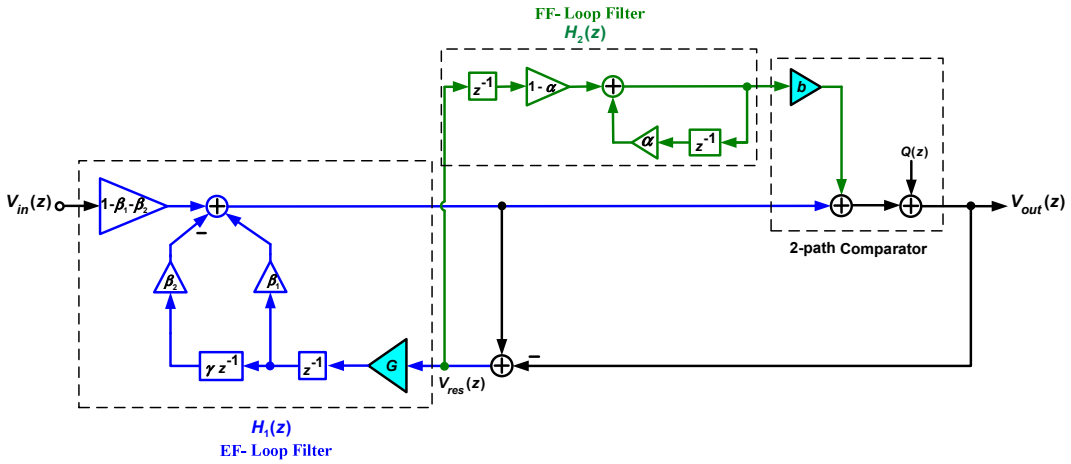

Fig. 1. Architectural block diagram of the proposed 3rd order NS-SAR ADC.

$$z_1 = e^0 = 1;$$
$$z_{2,3} = e^{j2\pi\frac{f_{2,3}}{f_s}} = \cos\left(2\pi\frac{f_{2,3}}{f_s}\right) + jsin\left(2\pi\frac{f_{2,3}}{f_s}\right) \quad (9)$$

we assume *OSR* = 8, then from (7) and (9) we get:

$$z_{2,3} = 0.954 \pm j0.299 \quad (10)$$

to implement a NS-SAR ADC with NTF as (6), we use a combined technique of FF and EF. In this structure, the two resonance zeros are provided by the EF path, while the DC zero is implemented by the FF path. Of course, the FF path is made of a passive integrator. The passive integrators don't have an accurate response. They encounter some charge-sharing attenuation which causes little deviation in their pole location. On the other hand, to have a robust NTF is required that the pole of the integrator be within the unit circle [7]. So we assume z_1=0.8. From (10) we have:

$$\begin{cases} z_2 + z_3 = 1.908 \\ z_2 . z_3 = 1 \\ z_1 = 0.8 \end{cases} \Rightarrow NTF\ Numerator = (1 - 0.8z^{-1})(1 - 1.908z^{-1} + z^{-2}) \quad (11)$$

the NTF numerator from (6) is equal to (11), so we have;

$$\begin{cases} \alpha = 0.8 \\ G_1.\beta_1 = 1.908 \\ G_1.\beta_2.\gamma = 1 \end{cases} \quad (12)$$

we assume G_1=30, γ=0.476, and b=4 then β_1 and β_2 can be calculated. Also with the above assumptions, the NTF pole was omitted. So the final *NTF*(z) is as follow:

$$NTF(z) = (1 - 0.8z^{-1})(1 - 1.908z^{-1} + z^{-2}) \quad (13)$$

the proposed *NTF*(z) has three zeros. All the zeros are within the unit circle. In section III, the system-level simulation results of the proposed ADC are presented.

C. Overal noise analysis of the proposed structure

Fig. 2 shows the non-ideality and noise effects of the proposed-NS SAR ADC. These have been studied and the total output noise is:

$$\begin{aligned} N_{out,tot} = {} & [Q(z) + n_{comp}(z) + n_{DAC}(z) \\ & + V_{OS}(z)].NTF(z) \\ & + [n_{amp}(z) + n_{EFC}(z)]G.z^{-1}(\beta_1 \\ & - \gamma.\beta_2.z^{-1}) + n_{res1}(z).\beta_1 \\ & + [n_{drst}(z) \\ & + n_{res2}(z)].\gamma.\beta_2.z^{-1} \\ & + n_{dres2}(z).\beta_2 \\ & + n_{samp}(z).(1 - \beta_1 - \beta_2) \\ & + n_{int}(z).\frac{b}{1 - \alpha.z^{-1}} + \varepsilon_{DAC}(z) \end{aligned} \quad (14)$$

where $Q(z)$ is the quantization noise of the ADC. $n_{comp}(z)$, $n_{DAC}(z)$ are thermal noise of the comparator and CDAC respectively. V_{os} (z) is the comparator offset. These four sources transfer to the output by the NTF. So they will be 3rd- order shaped and impose a negligible effect on the total noise portion. $n_{amp}(z)$ is the DAMP input-referred noise. $n_{EFC}(z)$ catches the noise polled on the CDAC when disconnecting the FIR capacitors before the residue amplification. As seen in (14), $n_{amp}(z)$ and $n_{EFC}(z)$ will be 1st- order shaped and has little effect on the total output noise. n_{res1}, n_{res2}, n_{drst}, and n_{dres2} are relevant to the SC activities of the FIR filter in the EF path. n_{samp} is the differential input sampling noise on the CDAC. n_{int} is the passive integrator noise captured by the integrator capacitor at the integration phase. ε_{DAC} is the DAC non-linearity. These noise sources will be unshaped and make output noise of the system.

III. Simulation Results

In NS SAR ADC, the SAR ADC core generally purveys multi-bit quantization. This feature obviates the stability obstacle of conventional high-order SD modulators with a coarse quantizer. So we can implement high-order NTF by NS-SAR ADC securely [14]. Of course, higher-order NTF resulted in more power, area, and complexity of the structure. So with this trade-off, we consider a 3rd- order NTF to implement. In this work the SAR ADC has a crude resolution of 10 bits, allowing a comparatively low OSR of 8 to get higher bandwidth. The sampling frequency and bandwidth of the signal are f_s = 3.2 MS/S and f_b = 200 kHz respectively. This ADC is suitable for some applications such as IoT sensors [11].

Considering optimized NTF as (15), we sketched the NTF pole-zero plot by the MATLAB software. Fig. 3 shows

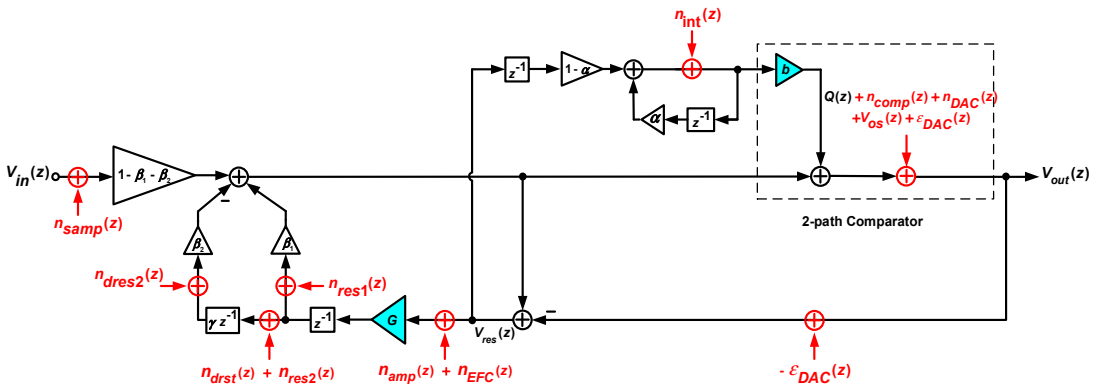

Fig. 2. Non-ideal noise sources in the signal flow diagram of the proposed system.

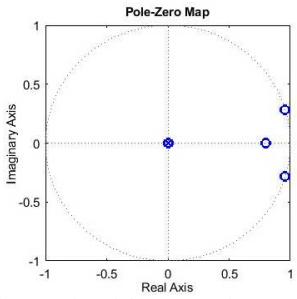

Fig. 3. Pole-zero plot of the proposed NTF

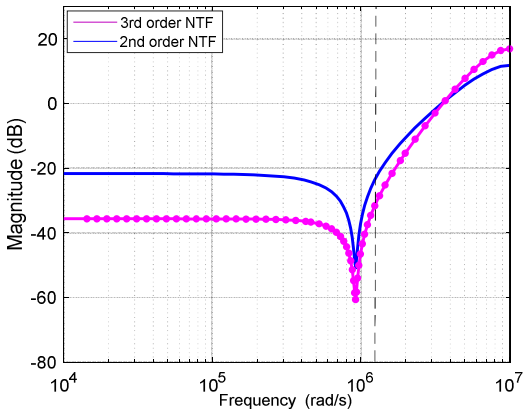

Fig. 4. The magnitude of the proposed NTF compared with the 2nd order NTF.

the result. As seen in this figure, the proposed NS-SAR ADC has two complex conjugate zeros. Despite the complex zeros do not fall exactly on the unit circle, they are sufficiently close circles and the third zero is near to DC.

Fig. 4 shows the magnitude of our proposed 3rd-order NTF compared with the 2nd -order NTF. The noise spectrum around the zeros of the NTF will be attenuated remarkably, allowing the input signal band to be positioned around the NTF's zeros. As shown in this figure, two complex conjugate zeros make a strong notch at the signal band. Because of added real zero, noise suppression by the proposed NTF is near 14 dB more than 2nd order NTF at low frequencies. Also, this applies to in-band noise.

Fig. 5 presented the MATLAB simulation result of the proposed system compared with the 2nd-order NS-SAR ADC reported in [7]. According to that, the output spectrum of the proposed 3rd-order NS-SAR ADC obtains lower total noise power at the interested frequency band, especially at low frequencies. With the OSR of 8, able to create a strong notch that gives the effective number of bit (ENOB) of 17 which shows 1.6 bits improvement compared with 2nd order NS-SAR ADC. In this simulation, the number of the FFT points (NFFT) is 1024. TABLE I have shown complete simulation results of two structures. Fig. 6 shows the simulated SNDR versus input signal amplitude that determines a dynamic range (DR) of 107dB for the proposed structure.

Unlike many published articles [10,15], this work just uses one switch and capacitor to build a passive integrator. So it is more simple and area-efficient compared with them. Also, it just uses a 2-path comparator with an embedded gain of 4 to compensate passive integrator attenuation that is lower required gain and is more power-efficient compared

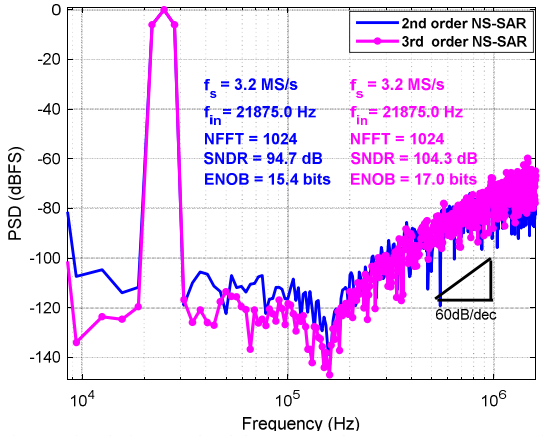

Fig. 5. simulation result of the proposed system PSD compared with the 2nd-order NS-SAR.

TABLE I. SUMMARY OF THE PROPOSED 3RD ORDER NS-SAR ADC COMPARED TO THE 2ND ORDER NS-SAR ADC.

Specifications	2nd order NS-SAR	Proposed 3rd order NS-SAR
f_s (MS/S)	3.2	3.2
f_b (kHz)	200	200
OSR	8	8
SAR ADC resolution (bits)	10	10
Number of FFT points	1024	1024
SNDR (dB)	94.7	104.3
ENOB (bits)	15.4	17
SFDR (dB)	104.6	113.5

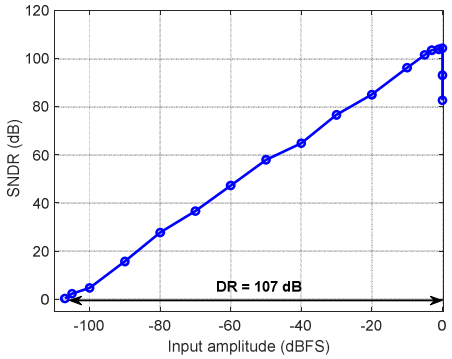

Fig. 6. SNDR versus input signal amplitude.

with other works like [10,16]. This work Utilizing passive integrator in a 2nd-order EF-NS-SAR make quantization and comparator in-band noise suppression improvement compared with [7] which is a 2nd-order EF structure. Furthermore, the proposed structure is low power and has a fully dynamic behavior, which means it doesn't consume any static power. So is suitable for low-power high resolution applications.

IV. Conclusion

This paper proposes a simple, robust, and scaling-friendly 3rd-order NS-SAR ADC. It employs a combined technique of the EF and FF methods to build an effective 3rd-order NS-SAR ADC with low modification in raw SAR-ADC. It uses a passive integrator to increase quantization noise suppression at low frequencies. We compensate the integrator attenuation by setting a respective low gain of 4 inside a two-path comparator. The NTF zeros are optimized which makes effective noise-shaping implementation. The SNDR is improved from 94.7 dB to 104.3 dB in a 200 kHz bandwidth after adding FF-path. The proposed ADC is a good candidate for IoT applications.

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