The Design of Sigma-Delta Analog to Digital Converters for Digital Audio

Mohammad Yavari and Omid Shoaei

Electrical & Computer Engineering Department, University of Tehran, Iran

P.O. 14395-515, Tehran, Iran

Emails: yavari@ieee.org

yavari@ece.ut.ac.ir

Abstract: **This paper presents the design of a second-order Sigma-Delta modulator for digital audio. This modulator has been designed at 3 V power supply with oversampling ratio of 256 and simulated in a 0.6 mm CMOS technology. The simulated results give SNDR of 96 dB for a 24 KHz signal bandwidth. The sampling frequency is 12.288 MHz and the Nyquist rate of the modulator is 48 KHz.**

Index terms: **Sigma-Delta modulation, switched capacitor circuits, operational amplifier, digital audio.**

1. INTRODUCTION

SIGMA-DELTA modulation is a robust means of implementing high-resolution analog to digital converters in VLSI technology [1]. The basic properties of the Sigma-Delta modulators include: 1) the sampling frequency is much higher than the Nyquist rate of the input signal, 2) a low resolution quantizer is used within a feedback loop configuration, 3) the noise energy generated in the quatizer is shaped toward higher frequencies. Moreover, by trading accuracy with speed, Sigma-Delta modulators allow high performance to be achieved with a low sensitivity to analog component imperfections and without requiring component trimming. By combining oversampling and feedback to shape the noise, and then using a digital low-pass filter to attenuate the noise that has been pushed out-of-band, it is possible to achieve a dynamic range as high as 18-bit. Moreover, oversampling architectures are potentially a power efficient means of implementing high-resolution A/D converters. In effect, an increase in sampling rate can be used to reduce the number and complexity of the analog circuits required in comparison with Nyquist rate architectures, transferring much of the signal processing into the digital domain where power consumption can be dramatically reduced simply by scaling the technology and reducing the supply voltage.

In the past decade, oversampled Sigma-Delta modulation has been the technology of choice for audio A/D converters. This is due to insensitivity to component mismatch and the cost merit when using a fine-line CMOS process. Such ADC's for performance-driven applications like professional audio are usually classified as high-end and require at least 16-b resolution. Several

Sigma-Delta ADC's with 16-b and higher performance have been previously reported [2], [3], [4], [5], [6], [7], however all operate with 5-V power supply to take advantage of the larger signal swing or use a more complex modulator than a second-order. In this paper our goal is to design a second-order modulator for digital audio with low complexity structure that has more benefits than the higher order and cascade modulators for implementation.

Section (2) presents the design of a Sigma-Delta modulator in system level; the effect of non-idealities is modeled and simulated in this section. In section (3) the required building blocks of the modulator is designed. Section (4) presents the result of simulations that has been performed in circuit level with HSPICE.

2. SYSTEM LEVEL DESIGN

A. Modulator Architecture

Sigma-Delta modulator architectures may be classified as either single loop, which use one A/D and D/A converter along with a series of integrators, or multistage (MASH), which consist of a cascade of single loop Sigma-Delta modulators. Both single loop and cascade architectures may employ either single bit or multi bit A/D and D/A converters.

A single loop Sigma-Delta modulator with more than two integrators will suffer from unstable oscillations for large level inputs, therefore they cannot be chosen for higher overload level modulators. An important advantage of using a multi bit quantizer is that the integrator settling requirements are greatly relaxed since the amplitude of the maximum step change in the integrator input is smaller than with a 1-bit quantizer. Therefore, the integrator seldom slew limits, and the time available for linear settling is maximized. This, in turn, implies a savings in power. Finally, the amplitude of spectral tones is greatly diminished because the total quantization noise is lower, and the quantizer is not continuously in an overload condition. The obvious drawback of multi bit quantization modulators is the need for high linearity in the feedback DAC. Unfortunately, much of the power savings of multi bit quantization are lost owing to the complexity of the techniques that must be used to linearize the output of this DAC. Cascade architectures use combination of inherently stable first and second order Sigma-Delta modulators to achieve higher order noise shaping. Since stability criteria are relaxed as compared to the higher order loops, the cascade modulators approach the dynamic range more than higher order single loop implementations at the cost of a higher sensitivity to the non-idealities of the building blocks [8].

According to the above discussion, a second order Sigma-Delta modulator with one-bit quantizer has been considered in this paper.

Fig. 1 shows the second-order sigma-delta modulator, which has been used in [9]. The integral gain coefficients of this modulator have been improved for achieving higher Signal-to-Noise Ratio (SNR) and Dynamic Range (DR) with behavioral simulations. The peak SNR of an ideal nth order Sigma-Delta modulator with oversampling ratio of OSR and b-bits in the quantizer can be expressed as:

$$SNR_{peak} = \frac{3p}{2}(2^b - 1)(2n + 1)(\frac{OSR}{p})^{2n+1} \qquad (1)$$

Relation (1) tells us that oversampling ratio (OSR) should be at least 256 for 16-b resolution. It should be noted that for simplicity in the design of decimation filters, oversampling ratio should be a power of two. With considering OSR of 256 and one-bit DAC relation (1) gives SNR of 109 dB. Therefore a second order modulator with this oversampling ratio is suitable for 16-b resolution.

B. Non-Idealities

In relation (1) the effect of the non-idealities is ignored. The non-idealities include clock jitter, switches thermal noise, op-amp noise, finite dc gain, finite bandwidth, slew rate, limited swing of op-amps and comparator hystersis [10]. With modeling each of the non-idealities, the proposed second-order modulator has been simulated at behavioral level simulation [11]. These simulations give the required specifications of the building blocks of the modulator, which are shown in Table 1.

In the high-resolution Sigma-Delta modulators, the sampling capacitance is determined by noise requirements due to the KT/C noise of the switches. For fully differential modulators, the SNR due to KT/C noise can be written as:

$$SNR_{KT/C} = \frac{(2 \times OL \times Vref)^2}{2} \times \frac{Cs \times OSR}{4KT} \qquad (2)$$

With considering the sampling capacitance of 1pF the maximum SNR due to KT/C noise is 106 dB, which is suitable for 16-b resolution. The maximum Signal to Noise + Distortion Ratio (SNDR) that has been obtained with this non-idealities is 102dB. The power spectral density (PSD) of the modulator has been shown in Fig. 2, whereas Fig.3 shows the SNDR versus the input signal level. From this figure the dynamic range (DR) of 105 dB is obtained that is suitable for 16-b resolution.

3. CIRCUIT LEVEL DESIGN

A. Operational Amplifier

Fig. 4 shows the folded cascode fully differential op-amp that achieves high bandwidth with capacitive loads. The use of a PMOS differential pair eliminates the need of chopper stabilization, since the 1/f noise is 30 times lower than NMOS in this process. For achieving the 60 dB dc gain and 92 MHz bandwidth there is no need for gain enhancement and other techniques. Common mode feedback is a switched capacitor circuit that has shown in Fig. 5. It senses the output common mode voltage and controls the bias current of M3 and M4, therefore sets the output common mode voltages to mid-supply. The simulated op-amp unity gain bandwidth is 98 MHz with a 2pF load, and the dc gain is 65 dB in the worst case.

B. Comparator

The second major component of the modulator is the comparator. The performance of the modulator is relatively insensitive to comparator offset and hystersis since the effects of these impairments are attenuated by the same second order noise shaping that attenuates the large quantization noise. The regenerative latch shown in Fig. 6 has been used to implement the comparator. In this latch, the cross-coupled devices M_3-M_4 and M_7-M_8 are strobed at their drains, rather than sources, to eliminate back-gating effects and promote faster regeneration [1].

C. Clock Generation

The integrators need a 2–phase non-overlapping clock (with delays) to minimize signal-dependent charge injection errors. Fig. 7 shows the circuit that has been used for this work. The delays and non-overlap times are affected by the delays in the inverter chain and the NOR gates.

D. Modulator Circuit Schematic

A circuit schematic of the modulator is shown in Fig. 8. Two-phase, non-overlapping clocks together with delayed versions of these clocks control the modulator. Because of the large signal swings in the first integrator of the modulator, switches s_1 and s_2 are full CMOS transmission gates and the other switches are NMOS transistors only. In the switches s_1 and s_2 which sample the input

and the feedback references in the first integrator, it is important to maintain a relatively constant resistance with variations in the voltage being sampled in order to avoid signal dependent charge injection. This was accomplished by making the PMOS transistors in those switches 3 times larger than the NMOS transistors. While this does not only equalize the on-resistance of the two transistors, it significantly reduces the variation. Large switch sizes at the input have the disadvantage of increased kickback into the signal source, which have difficulty absorbing the charge. The output of comparator is stored in a SR latch, which is used for DAC's.

4. SIMULATION RESULTS

The modulator of Fig. 8 has been simulated in a 0.6 μm, 3 V CMOS technology with HSPICE and the resultant SNDR, which has been obtained, is 96 dB. Fig. 9 shows the power spectral density for a 1.5 KHz, -3dB sinusoidal input signal, and 8192 FFT points. The power efficiency of the ADC's that has been obtained in the references of this paper are compared with following figure of merit and shown in Fig. 10. Table 2 shows the resultant performance of the simulated modulator.

$$FM = \frac{4KT \times SNDR \times f_N}{P} \qquad (3)$$

Where P is the total power dissipation of the converter and $SNDR$ is expressed as a ratio rather than in dB.

5. CONCLUSION

In this paper a second order Sigma-Delta modulator for digital audio has been designed and simulated in a 0.6 μm CMOS process. It uses only a 3 V power supply and achieves 96 dB SNDR that is suitable for 16-b resolution. The modulator total power consumption is 2.2 mW without considering output buffers.

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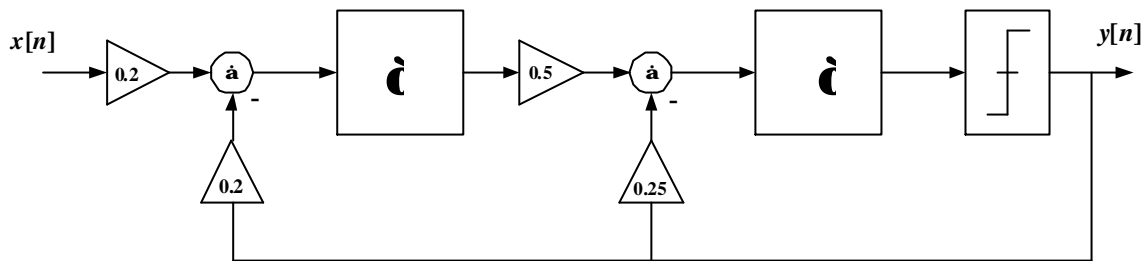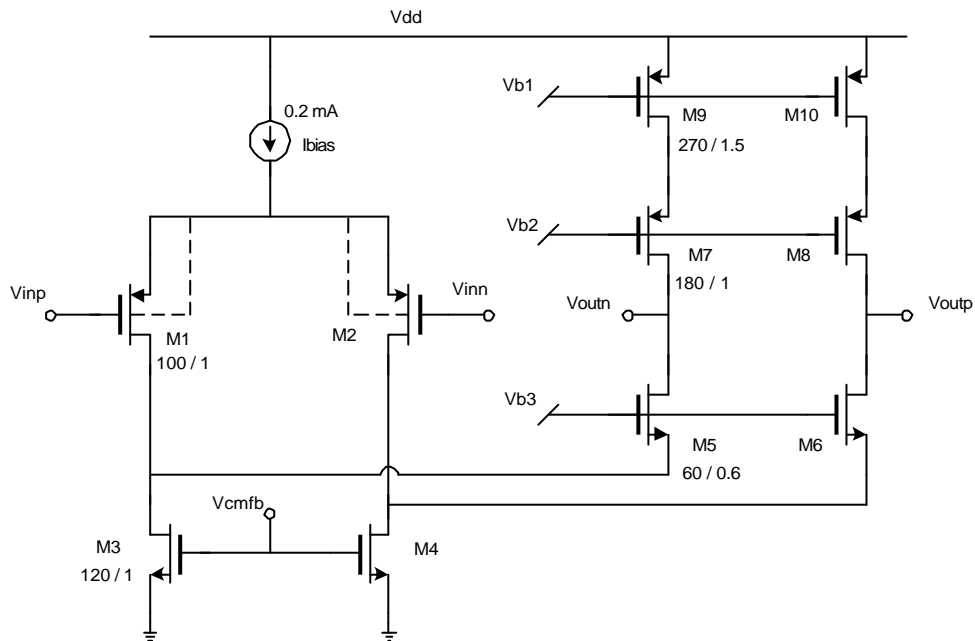
Fig. 1: Second-order Sigma-Delta Modulator.
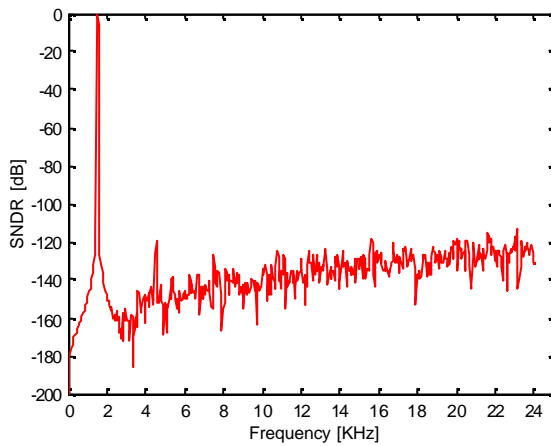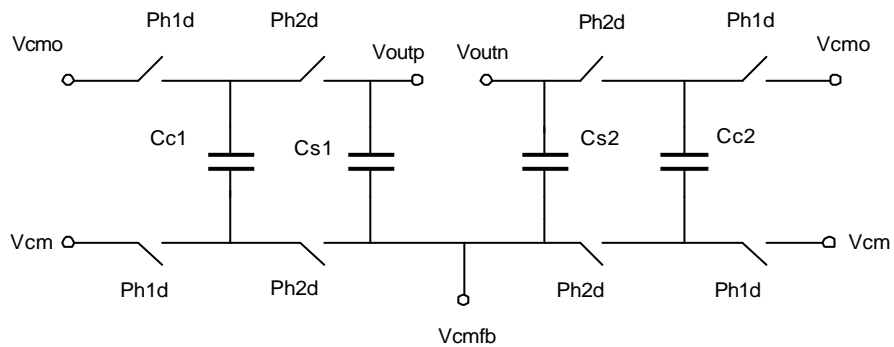

Fig. 2: Power Spectral Density.
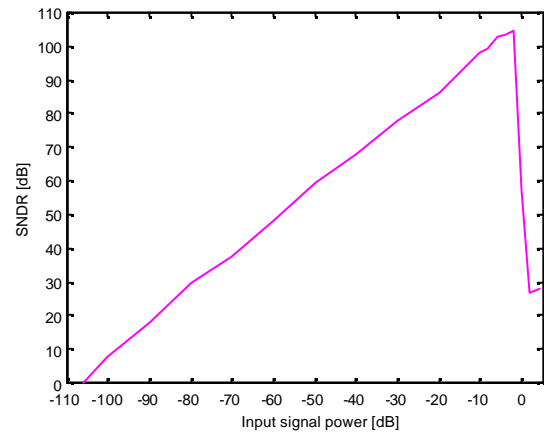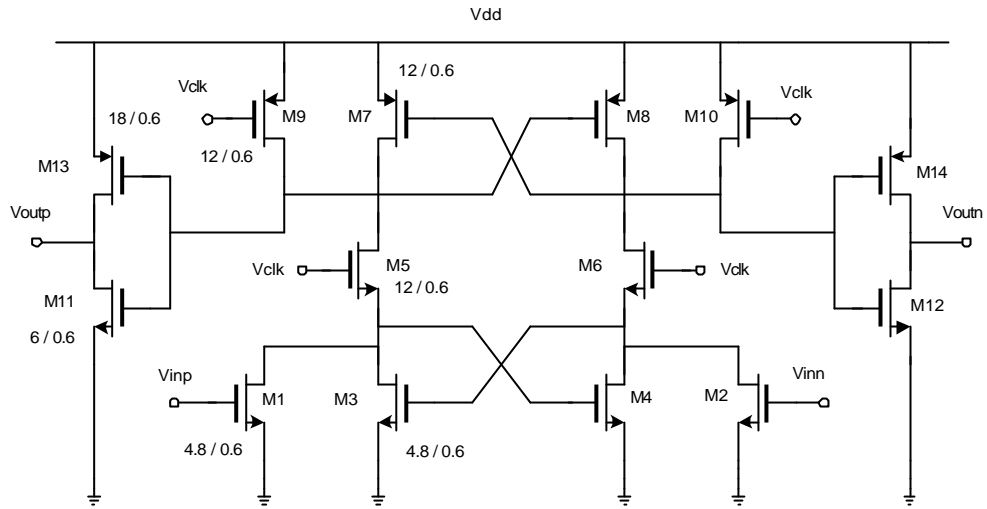

Fig. 3: Dynamic Range.

Table 1: Required specifications of the building blocks.

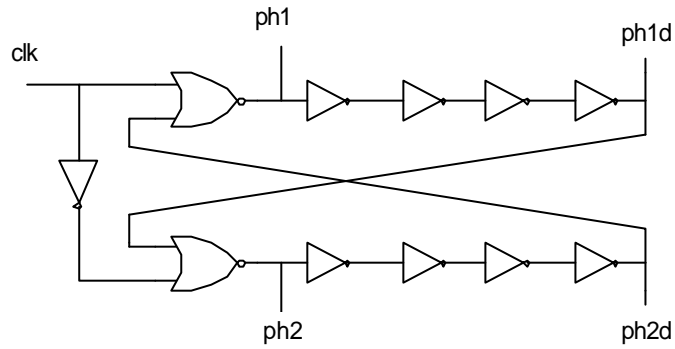|	
DC Gain of Op-Amps [dB]	60
Slew Rate [v/μs]	80
Unity Gain Bandwidth [MHz]	92
Input Referred Op-Amp Noise [μV_{rms}]	30
Switches Thermal Noise (KT/C) Sampling Capacitance (C_s)	1pF
Comparator Hystersis [v]	0.2

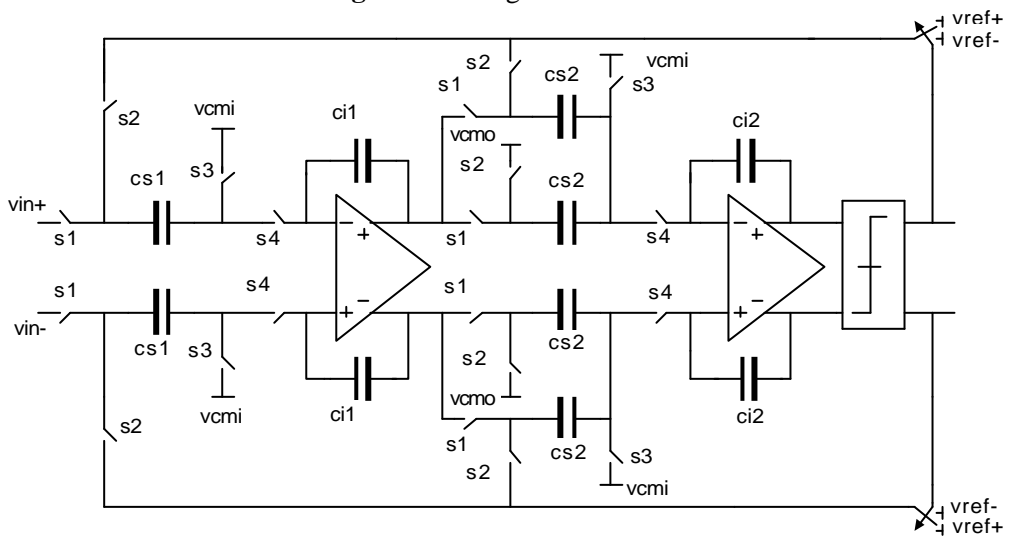**Fig. 4:** Folded cascode fully differential op-amp.

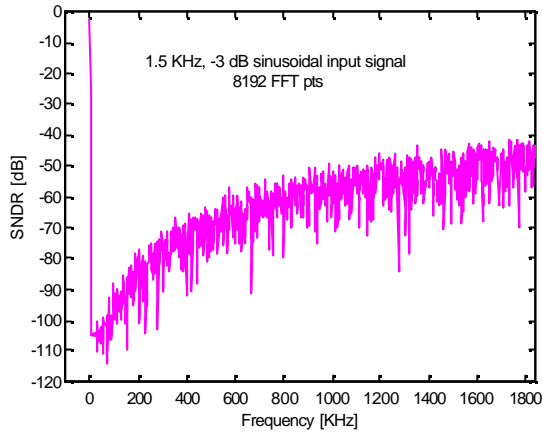**Fig. 5:** Common mode feedback circuit.

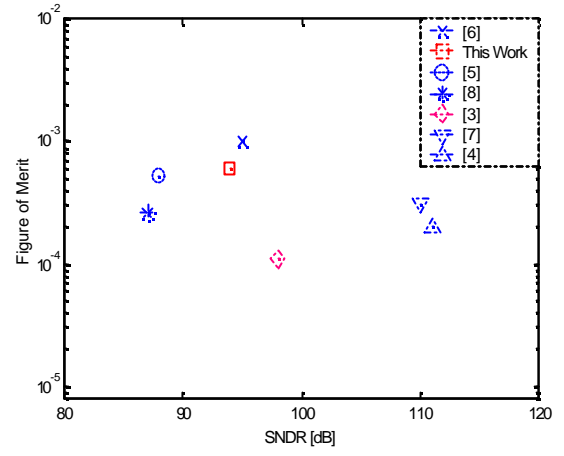**Fig. 6:** Dynamic latch type comparator.

Fig. 7: Clock generator.

Fig. 8: Circuit level schematic of the second-order modulator.

Fig. 9: Result of the simulated SNDR on the circuit level.

Fig. 10: Figure of merit versus SNDR of the references.

Table 2: Modulator performance.

Power Supply	3 V
Signal Bandwidth	24 KHz
Oversampling Ratio	256
Power Consumption	2.2 mW
SNDR	96 dB
Technology	0.6 um CMOS