MASH Sigma-Delta Modulators with Reduced Sensitivity to the Circuit Non-Idealities

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***Abstract*— In this paper several techniques are presented to significantly relax the analog circuit requirements such as the amplifiers dc gain and capacitors matching of multi-stage noise-shaping (MASH) sigma-delta modulators. In the first technique, one order redundant noise shaping is employed in the early stages and the first order shaped quantization error of the early stages is used as the input of the succeeding stages. In the second technique, a high order ΣΔ modulator is used in the first stage and the overall noise shaping is only performed by the analog filtering. Simulation results and mathematical analysis are provided to demonstrate the usefulness of the proposed structures.**

I. Introduction

High-speed sigma-delta A/D converters are widely used in both emerging wired and wireless communications applications. Broadband operation and low power consumption mandate a low oversampling ratio (OSR) for the ΣΔ modulator. To meet the required accuracy requirements under these conditions high-order noise shaping and multibit quantization are highly desirable. Multi-stage noise shaping (MASH) modulators enable high-order noise shaping without any stability problems and much reduced spurious idle tones. Nonetheless, MASH modulators are sensitive to the analog circuit imperfections such as the amplifiers limited dc gain and sampling capacitors' mismatch. In this paper, a few solutions are presented to alleviate the performance degradation of the MASH ΣΔ modulators due to the analog circuits' imperfections.

II. General MASH Structure

Figure 1 shows a general structure of cascade of two high-order single-stage modulators where $L_{si}(z)$, $L_{ni}(z)$, and $E_i(z)$ denote the signal and noise loop filters and the quantization error of the i-th stage, respectively. $H_1(z)$ and $H_2(z)$ compose the digital cancellation logic. By assuming a unity signal transfer function (STF) and the ideal noise-differencing noise transfer function (NTF) in both modulator stages and the digital cancellation filters given by

$$H_1(z)=1\,,\qquad H_2(z)=\left(1-z^{-1}\right)^{L_1}/\hat{\beta} \tag{1}$$

the overall output of the cascaded modulator will be:

$$Y(z)=X(z)+\delta_\beta\left(1-z^{-1}\right)^{L_1}E_1(z)-\left(1-z^{-1}\right)^{L_1+L_2}E_2(z)/\hat{\beta} \tag{2}$$

where L_1 and L_2 are the order of the first and second stage modulators, respectively. $\hat{\beta}$ is the digital estimate of the analog β coefficient and generally $\beta=\hat{\beta}\,(1-\delta_\beta)$ where δ_β represents the mismatch between these coefficients.

As is clear, the first stage quantization error is attenuated by the order of the first stage modulator and leaks in the overall output due to the mismatch. For p-dB signal-to-quantization noise ratio (SQNR) degradation of the modulator due to the leakage of the first stage quantization error, the maximum amount of the mismatch is given by:

$$\delta_\beta \le \sqrt{\left(10^{p/10}-1\right)\left(\frac{(2L_1+1)}{2(L_1+L_2)+1}\right)}\left(\frac{\pi}{OSR}\right)^{L_2}\left(\frac{1}{\beta}\right)\times\left(\frac{2^m-1}{2^n-1}\right) \tag{3}$$

where m and n are the number of the quantization bits in the first and second stage modulators, respectively.

Figure 2 illustrates the block diagram of a conventional MASH 2-2 modulator. A unity STF is employed in both stages. By employing the unity STF, the effects of the circuit non-idealities such as the amplifier nonlinear dc gain and limited output swing are significantly reduced since only the quantization noise is processed by the integrators [1]. The second stage NTF zeros are placed at the inband frequencies by using a resonator based structure to enhance the noise shaping ability of the modulator. The optimal point of the inband zeros is obtained by setting the coefficient α as:

$$\alpha = 2-2\cos\left(0.8452\pi/OSR\right) \tag{4}$$

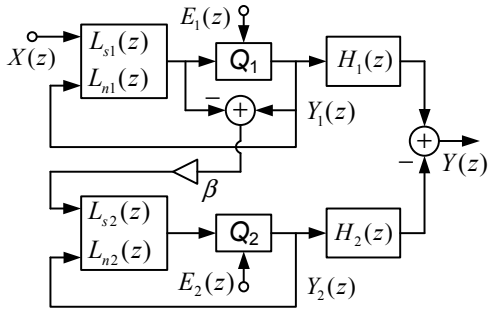

Fig. 1: Block diagram of the traditional two-stage MASH ΣΔ modulator.

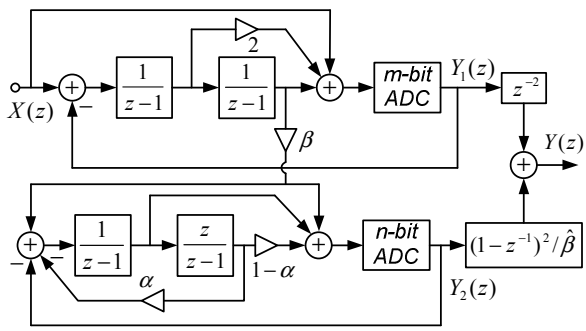

Fig. 2: Block diagram of the traditional MASH 2-2 unity STF ΣΔ modulator.

III. Proposed MASH Structures

A. Redudancy in the Early Stages

Figure 3 shows the block diagram of the first proposed MASH ΣΔ modulator. In this structure, the first order shaped quantization error of the first stage modulator, $V_1(z)$, is used as the input of the second stage modulator instead of the quantization error. The order of the first stage modulator is selected one order higher than that of the used in the conventional modulator for the same cascaded order. In this architecture, a unity STF is also used to realize the modulator of both stages due to its considerable advantages. Moreover, the ideal noise-differencing function is employed to implement the NTF of both stages. By assuming the digital cancellation filters as

$$H_1(z)=z^{-L_1},\quad H_2(z)=\left(1-z^{-1}\right)^{L_1}/\hat{\beta} \tag{5}$$

and considering the input of the second stage modulator to be

$$V_1(z)=-\beta\, z^{-L_1}\left(1-z^{-1}\right)E_1(z) \tag{6}$$

the overall output of the cascaded modulator is given by:

$$Y(z)=z^{-L_1}X(z)+z^{-L_1}\delta_\beta\left(1-z^{-1}\right)^{L_1+1}E_1(z)+\left(1-z^{-1}\right)^{L_1+L_2}E_2(z)/\hat{\beta} \tag{7}$$

where the order of the first and second stage modulators is (L_1+1) and L_2, respectively.

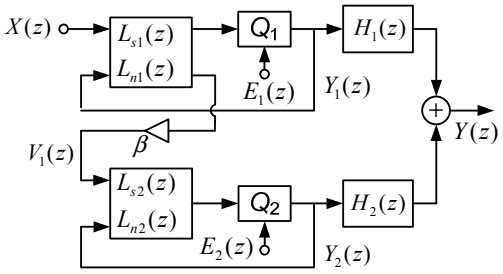

Fig. 3: Block diagram of the proposed MASH ΣΔ modulator with redundancy in the first stage.

As is seen, the noise shaping order of the cascaded modulator is L_1+L_2 and that is one order less than the sum of the order of both modulator stages. In other words, one order redundancy is used in the first stage modulator. This makes the first stage quantization error leakage in the cascaded modulator output to be attenuated by L_1+1 order which is one order higher than that of the conventional one with the same second stage quantization error shaping.

Similarly, for p-dB SQNR degradation of the modulator due to the leakage of the first stage quantization error we have:

$$\delta_\beta \le \sqrt{\left(10^{p/10}-1\right)\left(\frac{\left(2L_1+3\right)}{2\left(L_1+L_2\right)+1}\right)}\left(\frac{\pi}{OSR}\right)^{L_2-1}\left(\frac{1}{\beta}\right)\times\left(\frac{2^m-1}{2^n-1}\right) \tag{8}$$

Compared to the relation given in (3) the maximum amount of the mismatch in the proposed MASH structure that can be tolerated for the same SQNR degradation is higher than the conventional topology by the following ratio:

$$T=\sqrt{\left(2L_1+3\right)/\left(2L_1+1\right)}\,\left(OSR/\pi\right) \tag{9}$$

As an example, for OSR=16 and L_1=2, the mismatch of the proposed MASH structure can be 6 times higher than the conventional one for the same SQNR degradation. Therefore, the analog circuit requirements such as the amplifiers dc gain and capacitors matching of the proposed MASH modulator are considerably relaxed.

The proposed MASH 3-2 ΣΔ modulator which has the same noise shaping ability of the conventional MASH 2-2 structure is illustrated in Fig. 4. The overall output of this structure is given by:

$$\begin{aligned}Y(z)&=z^{-2}X(z)+z^{-2}\left(1-z^{-1}\right)^3\left(1-\beta/\hat{\beta}\right)E_1(z)\\&+\left(1-z^{-1}\right)^2\left(1-(2-\alpha)z^{-1}+z^{-2}\right)E_2(z)/\hat{\beta}\end{aligned} \tag{10}$$

which corresponds to the fourth order noise shaping as the conventional MASH 2-2 modulator while the first stage quantization error leakage is third order attenuated. So, the proposed MASH 3-2 modulator needs the relaxed analog circuit requirements at the cost of using only one extra integrator in the first stage modulator.

In the proposed MASH 3-2 structure, a third-order modulator with an FIR based NTF and unity STF proposed in [2] is employed as the first stage. The main advantage of this topology over the conventional feedforward single-loop architectures is the minimum terminating paths to the input of the quantizer which makes the passive implementation of the adder preceding the quantizer more feasible. It is worth mentioning that although it is possible to remove the adder preceding the quantizer by topologies proposed in [3, 4], however, since in this case the input signal will be processed at least by the last integrator, the maximum input signal level will be considerably decreased and hence a lower dynamic range will be obtained. In the second stage, a resonator based modulator is used in order to place the second stage NTF zeros at the inband frequencies. The optimal value of α given is also given by relation (4).

It is worth mentioning that the same behavior is achieved with a MASH 3-1 architecture shown in Fig. 5 which does not need an additional integrator in the second stage. Nonetheless, the proposed MASH 3-2 structure has two main advantages over the conventional MASH 3-1 modulator. First, it is possible to spread two of the NTF zeros at the inband frequencies resulting in more than 11 dB higher SQNR. Second, the conventional MASH 3-1 structure needs an extra DAC and a few other paths to extract the first stage quantization noise whereas this is not required in the proposed MASH 3-2 modulator.

It is also worth to mention that the performance of the conventional MASH 3-2 is the same as the proposed MASH 3-2 after considering the effects of the circuit's imperfections. However, since in the proposed MASH 3-2 the input of second stage modulator is simply the output of the second integrator of the first stage, its realization is simpler than the conventional MASH 3-2.

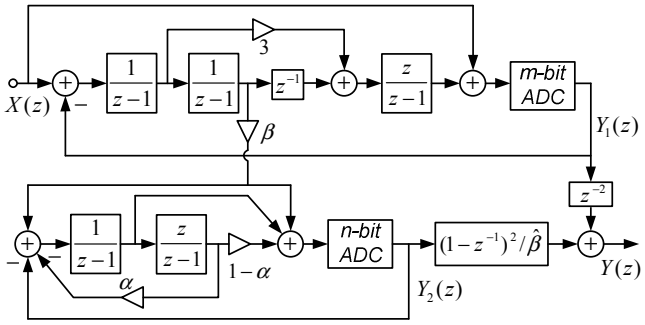

Fig. 4: Block diagram of the proposed MASH 3-2 ΣΔ modulator with one order redundancy in the first stage.

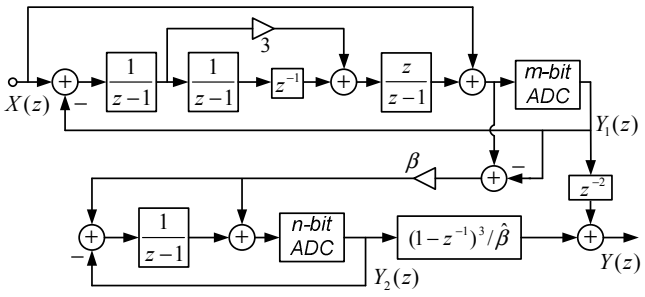

Fig. 5: Block diagram of the traditional MASH 3-1 unity STF ΣΔ modulator.

B. High-Order SMASH Structures

An alternative sigma-delta modulator that reduces the sensitivity to the quantization noise leakage of the first stage modulator has been recently proposed in [5] and called sturdy MASH (SMASH). In this structure, the output of the second stage modulator is digitally injected to the most insensitive node of the first stage modulator which is the output of the first stage quantizer. Hence, the effect of the first stage quantization error can be completely cancelled or shaped by the overall modulator's order depending on the second

stage STF. The second stage quantization noise is shaped by the overall order of the modulator. Since, in this structure, there is not any need for digital cancellation logic and a simple digital adder is required, the sensitivity to the mismatch between the analog and digital filters is reduced.

However, in the firstly proposed SMASH 2-2 structure in [5], the effect of the first stage quantization noise is only fourth order shaped like the second stage quantization noise. This results in 6-dB SNDR degradation compared to the conventional MASH 2-2 modulator. Besides, the proposed SMASH 2-2 in [5] needs at least one extra highly linear digital-to-analog converter (DAC) in the added feedback path to the first stage input. Moreover, in the proposed SMASH 2-2 in [5] it is not possible to employ a scaling coefficient between the modulator stages in order to enhance the overall noise shaping ability.

The above-mentioned drawbacks of the originally proposed SMASH 2-2 structure have been resolved by employing a unity STF in both modulator stages in [6]. Figure 6 shows the proposed unity STF SMASH modulator in [6] with inband NTF zeros in the second stage. The overall output of this structure is given by:

$$Y(z) = X(z) + \left(1-z^{-1}\right)^2\left(1-\beta/\hat{\beta}\right)E_1(z) - \left(1-z^{-1}\right)^2\left(1-(2-\alpha)z^{-1}+z^{-2}\right)E_2(z)/\hat{\beta} \quad (11)$$

where the optimal value of α is also given by relation (4).

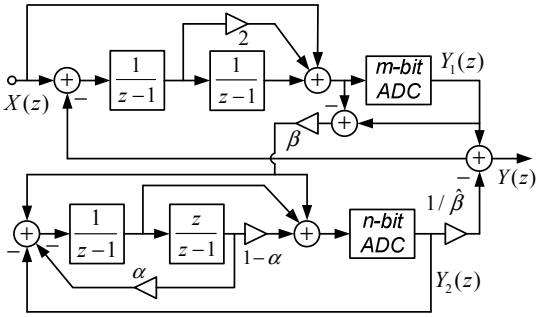

Fig. 6: Block diagram of the SMASH 2-2 unity STF ΣΔ modulator with inband NTF zeros in the second stage.

Interestingly, in this structure, the first stage quantization noise ideally is not processed in both modulator stages. Instead, the quantization noise of the second stage is processed in both stages. Hence, the stability of the overall modulator is mainly determined by the resolution of the second stage quantizer.

However, the SMASH 2-2 modulator shown in Fig. 6 suffers from two main drawbacks. Firstly, a digital adder is placed at the critical feedback path of the first stage modulator. The delay introduced by this adder will considerably limit the sampling frequency of the modulator since all of the quantization, digital addition, and DAC linearization operations should be started just after the input signal sampling phase and completed in the non-overlapping period between two clock phases. It is worth mentioning that this is necessary in all modulator structures that employ the unity STF by directly feed-forwarding the input signal to the quantizer input. However, in SMASH 2-2 shown in Fig. 6 the adder is significantly worsening the situation. A unit delay can be employed in the input signal sampling paths using a double sampling technique as proposed in [3] to extend the time available for the above-mentioned feedback operations. Secondly, one bit higher resolution is needed in the first stage modulator DAC since the outputs of both stages are digitally added. This complicates the DAC linearization technique and hence limits the DAC resolution of both stages to less than 4-5 bits.

In order to increase the order of SMASH modulators, a combination of SMASH and the traditional MASH modulators has been presented in [7]. In this paper, alternative structures are presented for high order SMASH modulators. In the proposed architectures, a high order modulator is employed in the first stage instead of the conventional second order one. Increasing the first stage modulator's order reduces the first stage quantization noise leakage and hence demands a moderate dc gain in the amplifiers as discussed in [8, 9] at the cost of the slightly reduced stability and input signal level. Nonetheless, by employing a unity STF and the efficient single-loop structures in the first stage, the maximum input level of the modulator can be comparable to those of the lower order modulators.

The proposed SMASH 3-2 is shown in Fig. 7 where a unity STF is employed in both stages and four of NTF zeros are optimally placed at the inband frequencies. The effect of the first stage quantization noise is completely cancelled by employing a unity STF in the second stage. The third-order single-loop structure proposed in [2] is used as the first stage and in the second stage a resonator based modulator is employed. The overall output of this structure is given by:

$$Y(z) = X(z) + \left(1-z^{-1}\right)\left(1-(2-\alpha_1)z^{-1}+z^{-2}\right)\left(1-\beta/\hat{\beta}\right)E_1(z) - \left(1-z^{-1}\right)\left(1-(2-\alpha_1)z^{-1}+z^{-2}\right)\left(1-(2-\alpha_2)z^{-1}+z^{-2}\right)E_2(z)/\hat{\beta} \quad (12)$$

where the optimal values of α_1 and α_2 are obtained as follows:

$$\alpha_1 = 2-2\cos\left(\frac{0.5385\pi}{OSR}\right), \quad \alpha_2 = 2-2\cos\left(\frac{0.9062\pi}{OSR}\right) \quad (13)$$

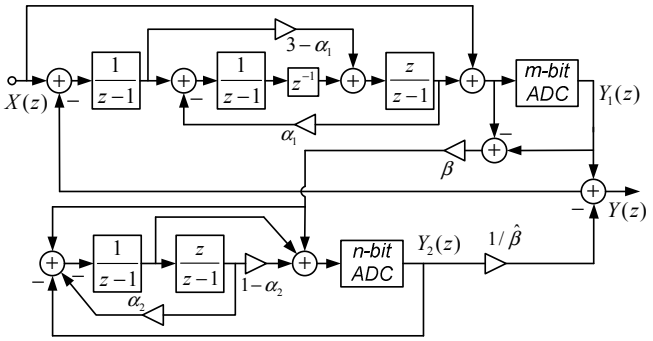

Fig. 7: Block diagram of the proposed SMASH 3-2 unity STF ΣΔ modulator.

IV. Simulation Results

The proposed MASH ΣΔ modulator shown in Figs. 4 and 7 along with the traditional unity STF MASH 2-2, SMASH 2-2 structures shown in Figs. 2 and 6 were simulated using MATLAB and Simulink. The number of quantization bits in both stages was 4 and β = 4. Circuit non-idealities including the amplifier finite dc gain, capacitor mismatch, and amplifier limited output swing were included in the Simulink models.

Figures 8 and 9 show the simulated signal-to-noise and distortion ratio (SNDR) versus the first integrator dc gain. As is seen the proposed MASH 3-2 ΣΔ modulator needs about 10 dB lower dc gain in the first integrator than the conventional MASH 2-2 structure for the same SNDR degradation. The dc gain requirements of SMASH structures are more relaxed and a 30 dB dc gain in the first integrator is sufficient to avoid a considerable SNDR degradation.

In Figs. 10 and 11 the simulated SNDR versus the input signal amplitude is illustrated. The proposed MASH 3-2 structure has about 7 dB higher SNDR than the conventional MASH 2-2 topology although it achieves about 1.2 dB lower overload level factor. The overload level factor of the SMASH 2-2 and SMASH 3-2

modulators are about -1.5dBFS and -2.5dBFS, respectively. The lower overload level factor of the proposed MASH modulators is due to their higher order loop filter in the first stage.

Figure 12 shows the SNDR degradation versus the mismatch between the analog interstage coefficient, β, and its corresponding estimate in the digital logic cancellation. The proposed MASH 3-2 modulator is more robust against this mismatch as theoretically expected. The sensitivity of SMASH modulators due to this mismatch is like the conventional MASH modulators since the first stage quantization error leakage is shaped by the similar order as demonstrated by analytical calculations.

Table I summarizes the normalized maximum output swing of the integrators. As is seen, since the input signal is not processed by the integrators due to the unity STF of both stages, the output swing of the integrators in the proposed MASH modulators is less than half of the reference voltage, and hence, these structures can be well suited for low voltage applications.

V. Conclusions

Two novel MASH ΣΔ modulators were presented. The proposed structures relax the analog circuit requirements by employing a higher order modulator in the first stage and one order redundancy in the overall structure or using a higher order SMASH modulator. This makes the proposed architectures most suitable for broadband and low-voltage A/D converters realized in deep sub-micron digital CMOS technologies.

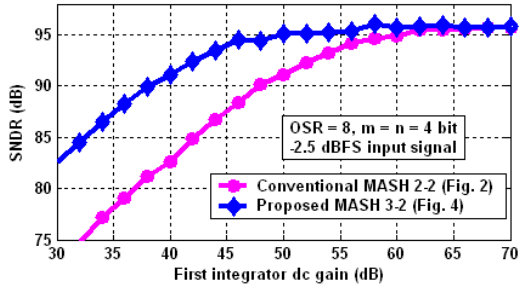

Fig. 8: SNDR versus the first integrator dc gain for the proposed MASH 3-2 and conventional MASH 2-2.

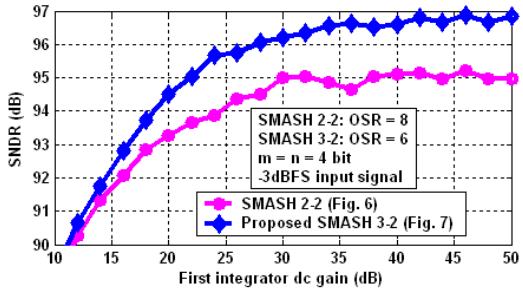

Fig. 9: SNDR versus the first integrator dc gain for the proposed SMASH 3-2 and conventional SMASH 2-2.

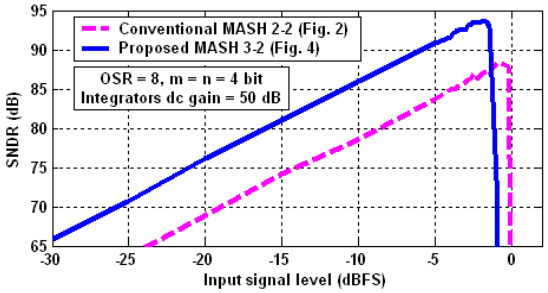

Fig. 10: SNDR versus the input signal amplitude for the proposed MASH 3-2 and conventional MASH 2-2.

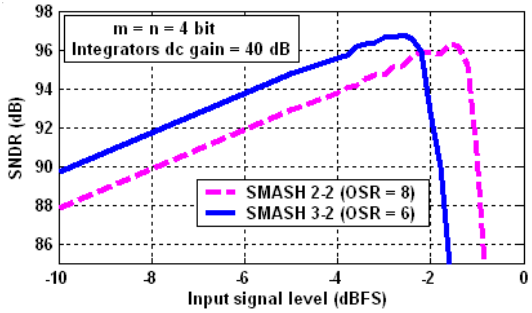

Fig. 11: SNDR versus the input signal amplitude for the proposed SMASH 3-2 and conventional SMASH 2-2.

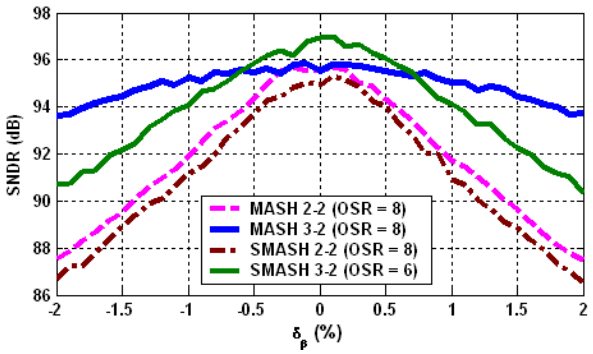

Fig. 12: SNDR degradation versus the mismatch between analog interstage coefficient β and its corresponding digital estimate.

Table I: Required output swing in the integrators relative to ± 1V reference.

Topology	1st-Intg.	2nd-Int.	3rd-Intg.	4th-Intg.	5th-Intg.
MASH 2-2 Fig. 2	±0.124	±0.0625	±0.125	±0.0625	----
MASH 3-2 Fig. 4	±0.24	±0.122	±0.41	±0.125	±0.0625
SMASH 2-2 Fig. 6	±0.11	±0.055	±0.125	±0.0625	----
SMASH 3-2 Fig. 7	±0.185	±0.088	±0.31	±0.124	±0.0625

References

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