DOUBLE-SAMPLED CASCADED SIGMA-DELTA MODULATOR TOPOLOGIES FOR LOW OVERSAMPLING RATIOS†

*Mohammad Yavari, Omid Shoaei, and Angel Rodriguez-Vazquez**

IC Design Laboratory, ECE Department, University of Tehran, Tehran 14395-515, Iran
* Instituto de Microelectrónica de Sevilla (IMSE-CNM), 41012 Seville, Spain
Email: myavari@ut.ac.ir

ABSTRACT

This paper presents novel double-sampling cascaded sigma-delta modulator topologies for wideband applications. The proposed modulator structures employ finite impulse response (FIR) noise transfer function (NTF) to achieve the aggressive noise shaping with an additional zero at the half of the sampling frequency to alleviate the quantization noise folding. Cascading of the proposed modulator structures is very simple without any additional circuit requirements.

1. INTRODUCTION

With the recent developments in both wired and wireless communications, there is a need to design analog-to-digital converters (ADCs) at MHz speeds with high linearity at low voltage environments. Sigma-delta modulators and pipelined ADCs are the two main candidates for high-resolution and high-speed applications. Pipelined converters need some type of calibration or error correction techniques to achieve accuracies beyond 12-bits, resulting in increased complexity and power dissipation.

Sigma-delta ADCs are the main candidates for high resolution applications due to their inherent immunity to the circuit non-idealities [1]. In order to employ them in broadband applications, a low oversampling ratio (OSR) should be employed. But, the reduction of OSR decreases the accuracy of the modulator, drastically. So, novel modulator structures are needed to alleviate the reduction of resolution in low OSR applications.

A useful approach in switched-capacitor realizations of the modulators is to employ the double-sampling technique [2]. In this method, the circuit operates during both phases of the clock. Hence, the effective sampling frequency of the system is twice that of the clock frequency. This results in doubling the OSR or the available time for settling of the integrators if OSR is fixed. Figure 1 shows a single-ended double-sampling integrator. In this circuit, two distinct capacitors are used to sample the input signal. The capacitor C_{S1} is used to sample the input signal at the phase ϕ_1 while at this interval the stored charge on C_{S2} is transferred into the integrating capacitor, C_I. At the next phase, ϕ_2, C_{S2} samples the input signal and C_{S1} transfers its stored charge into C_I. Hence, in both phases of the clock, the sampling and integrating is performed resulting in doubling the effective sampling rate of the system.

The signal transfer function of the double sampling integrator with an ideal opamp can be written as

$$V_{out}[n] = V_{out}[n-1] + \frac{C_S}{C_I} V_{in}[n-1] + \frac{(-1)^n \Delta C_S}{2 C_I} V_{in}[n-1] \qquad (1)$$

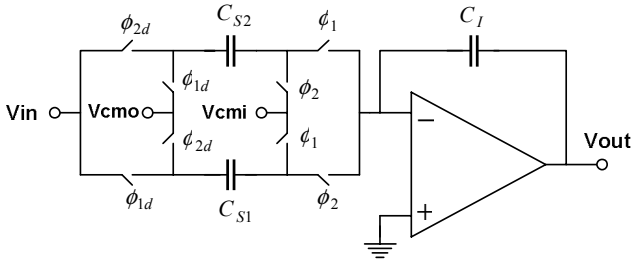

Fig. 1: A single-ended double-sampling integrator.

where $C_S = (C_{S1} + C_{S2})/2$, $\Delta C_S = (C_{S1} - C_{S2})$, and time $n = 0$ occurs when ϕ_2 is high [3]. The first two terms of the right side in (1) implements an ideal sample delaying integrator. But, the last term in (1) is the product of the input signal and $(-1)^n$ which indicates a modulation between the input signal and a sampled cosine at the half of the sampling frequency ($f_s/2$) through any mismatch between the sampling capacitors. If the input is a low frequency signal, this mismatch does not affect the inband frequencies. However, since the DAC output has a large high frequency quantization noise, this noise is folded into the inband frequencies if any mismatch exists between the DAC sampling capacitors. Therefore, the SNDR is degraded. This is the main drawback of double sampling modulators.

Several techniques have been proposed to alleviate the quantization noise folding in doubled-sampled modulators such as employing the fully floating method in the feedback DAC paths and/or placing a zero at the half of the sampling frequency ($f_s/2$) of the NTF, etc [3-5]. However, both techniques affect the modulator's NTF and signal transfer function (STF) and hence the modulator's noise shaping ability. So, their effects should be considered in the design of the modulator's NTF to achieve an aggressive noise shaping. In this paper, efficient high order double sampling cascaded sigma-delta modulators are proposed.

2. PROPOSED MODULATOR TOPOLOGIES

The general structure of a sigma-delta modulator is shown in Fig. 2 where $H(z)$ is the loop transfer function and its NTF is given by

$$NTF(z) = \frac{1}{1 + H(z)} \qquad (2)$$

The NTF of the proposed second-order double-sampling sigma-delta modulator is considered as an FIR filter:

$$NTF(z) = (1 - z^{-1})^2 (1 + z^{-1}) \qquad (3)$$

So, $H(z)$ is obtained as follows:

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$$H(z) = \frac{z^{-1}}{1-z^{-1}}\left(1 + \frac{z^{-1}}{1-z^{-2}}\right) \quad (4)$$

Hence, the structure of the proposed second-order modulator will be as shown in Fig. 3. This structure is composed of an integrator, a resonator, and a quantizer. A resonator is used instead of an integrator to realize a zero of NTF at $f_s/2$.

In this structure, the signal transfer function (STF) is unity. Unity gain STF in a sigma-delta ADC has many advantages such as the followings. First, the effects of the circuit non-idealities such as the limited opamp DC gain and nonlinearities are reduced since only the quantization noise is processed by the integrators [6]. Second, the dynamic range is increased because the only elements that have to accommodate the full input signal swing are the switches and the quantizer and the output swing of the opamps does not limit the input signal amplitude. Third, the integrators need small output swings.

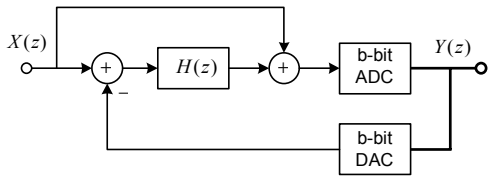

Fig. 2: General structure of a sigma-delta modulator.

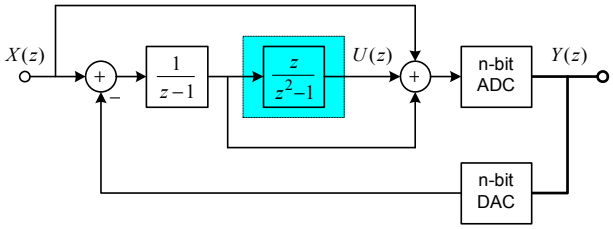

Fig. 3: The proposed second-order double-sampling modulator.

The double-sampling resonator with a unit delay can be implemented using only one opamp as proposed in [5]. So, only two opamps like the conventional second-order modulator are needed to realize the circuit of the proposed second-order modulator. The paths terminating to the input of the quantizer can be realized using a passive switched-capacitor circuit.

To cascade the proposed second order modulator, the output of the resonator can be used directly since it is only a function of the quantization noise and is as follows:

$$U(z) = -z^{-2}\, E_Q(z) \quad (5)$$

where $E_Q(z)$ is the quantization error and is assumed as an additive white noise. The structure of the proposed cascade 2-2 is shown in Fig. 4. This architecture employs the proposed second order as the first stage to achieve the double sampling with much reduced sensitivity to the sampling paths mismatch. In the second stage another second order modulator with unity gain STF and FIR NTF is used. The NTF zeros of the second stage are placed into the inband frequencies to achieve the aggressive noise shaping in low OSRs.

It can readily be shown that the sampling paths mismatch of the first integrator is shaped by the first order. The sampling paths mismatch of the resonator, third and fourth integrators are shaped second, third and fourth orders, respectively. On the other hand, due to the employing a multibit quantizer the out-of-band quantization noise will be lower than the case of using a single bit quantizer. Therefore, the multibit quantization also reduces the sensitivity of modulator to the sampling paths mismatch.

It is worth mentioning that the order of the proposed cascaded modulators can simply be extended to high orders efficiently. For example, in cascade 2-2-2 the proposed second-order modulator is used in the first stage. The second and third-stages can employ the conventional second-order structure with NTF's zeros optimized at the inband frequencies for aggressive noise shaping.

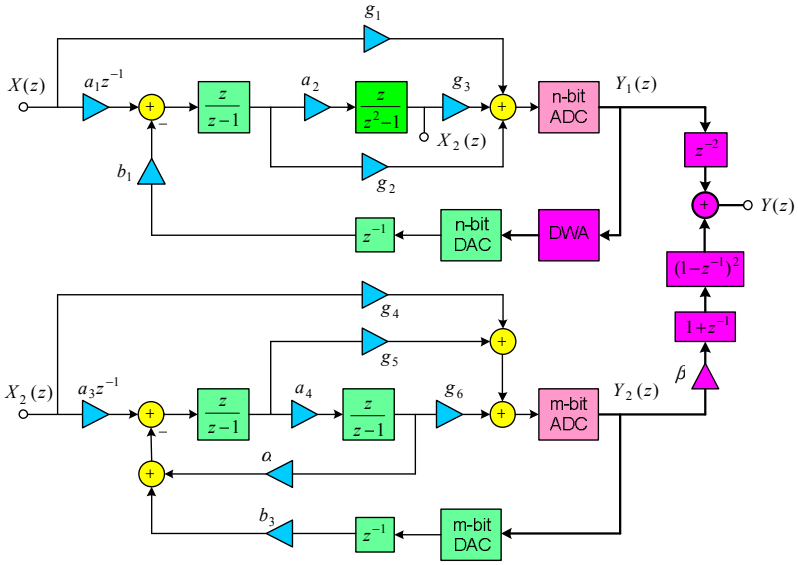

Figure 4: The proposed double-sampling cascade 2-2 modulator topology.

3. SYSTEM-LEVEL SIMULATION RESULTS

To show the usefulness of the proposed cascade 2-2 double-sampling modulator topology, its system level architecture taken into account the circuit non-idealities was simulated with MATLAB. In these simulations, the OSR and quantizer resolutions of the first and second stages were selected as 8, 5-bit and 3-bit, respectively. The coefficient α is needed to place two zeros of NTF at the inband frequencies. The design method proposed by Schreier [7] is used to obtain the value of α in order to place the inband zeros at the optimal points. The other coefficients are obtained such that the NTF of both stages become the high pass FIR filters. Then, signal scaling is performed to get the signal swing about full scale range at the quantizers' input. This results in the second stage quantization noise to be decreased by 16 times. So, the modulator coefficients are as follows:

$$a_1=b_1=2,\ a_2=2,\ g_1=1,\ g_2=1/2,\ g_3=1/4,\ a_3=2, b_3=1/2,\\ a_4=1,\ g_4=4,\ g_5=2,\ g_6=16/9,\ \alpha=1/9,\ \beta=1/16 \qquad (6)$$

Figure 5 shows the ideal output spectrum of the proposed cascade 2-2 modulator. The resultant maximum SNDR is about 97-dB. With including the circuit non-idealities the maximum SNDR is about 94-dB as shown in Fig. 6. These non-idealities include the DC gain of the first integrator and resonator of 70 dB, the DC gain of third and fourth integrators of 50 dB, 0.2% mismatch between the coefficients a_1, b_1 and a_2 , 1% mismatch between the other coefficients, 0.1% mismatch between sampling paths of the first integrator, and 0.5% mismatch between sampling paths of the other blocks. Simulation results indicate that the signal swings at the output of the integrators and resonator are much less than the reference voltage level as it is shown in Fig. 7 due to the unity-gain STF and also feedforward paths. This results in demanding low swing analog building blocks making the circuit design more relaxed especially in low voltage applications.

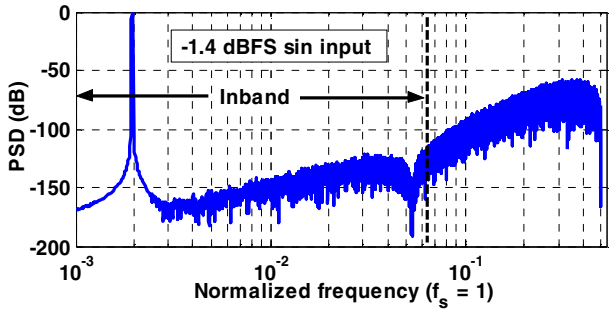

Figure 5: Simulated ideal output spectrum.

As mentioned before, the main concern of double-sampled modulators is the quantization noise folding due to the sampling paths mismatch. Figure 8 shows the SNDR degradation versus the mismatch of the sampling paths. As it is seen the SNDR degradation of the proposed cascade 2-2 is negligible even with a 0.1% mismatch between the sampling paths of the first integrator. The paths mismatch of the remaining blocks does not affect the SNDR of the modulator considerably as it is seen in Fig. 8. However, it should be noted that since the sampling capacitors of the first integrator are large due to the circuit noise considerations, a paths mismatch of about 0.1% is readily realizable.

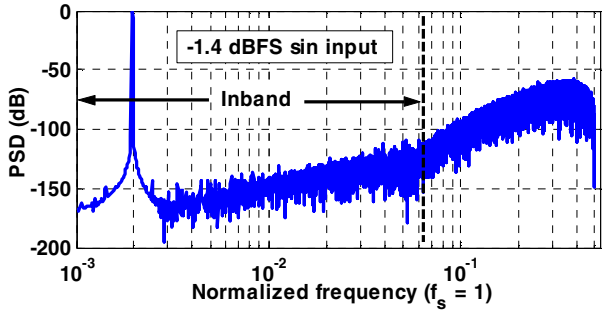

Figure 6: Output spectrum including the circuit non-idealities.

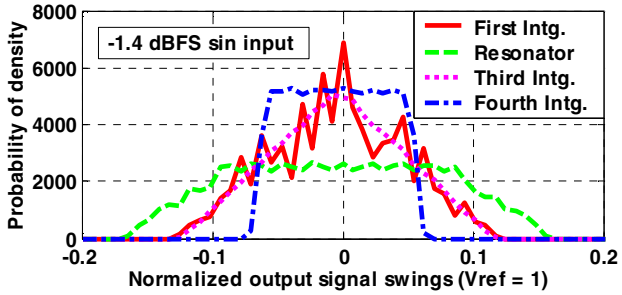

Figure 7: Building blocks output swings.

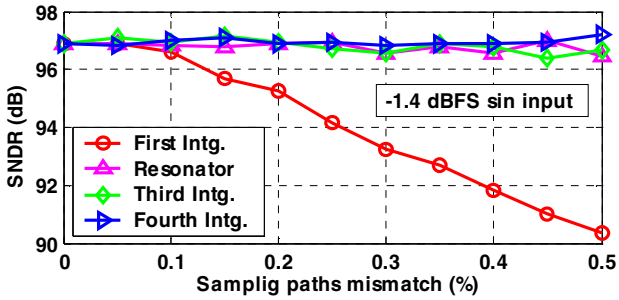

Fig. 8: SNDR degradation versus the sampling paths mismatch.

4. CIRCUIT IMPLEMENTATION

Figure 9 shows the switched-capacitor realization of the proposed second-order modulator. As it is seen the first integrator can be implemented using the conventional double-sampling integrators. The double-sampling resonator is realized by employing two integrating capacitors in a conventional double-sampling integrator. Each of these capacitors is used only in one clock phase. The addition of the signals preceding the quantizer can be implemented by a passive switched-capacitor circuit as shown in Fig. 9. In this circuit, the comparators' reference voltages are also subtracted from the input signal of the comparators to make the desired decision.

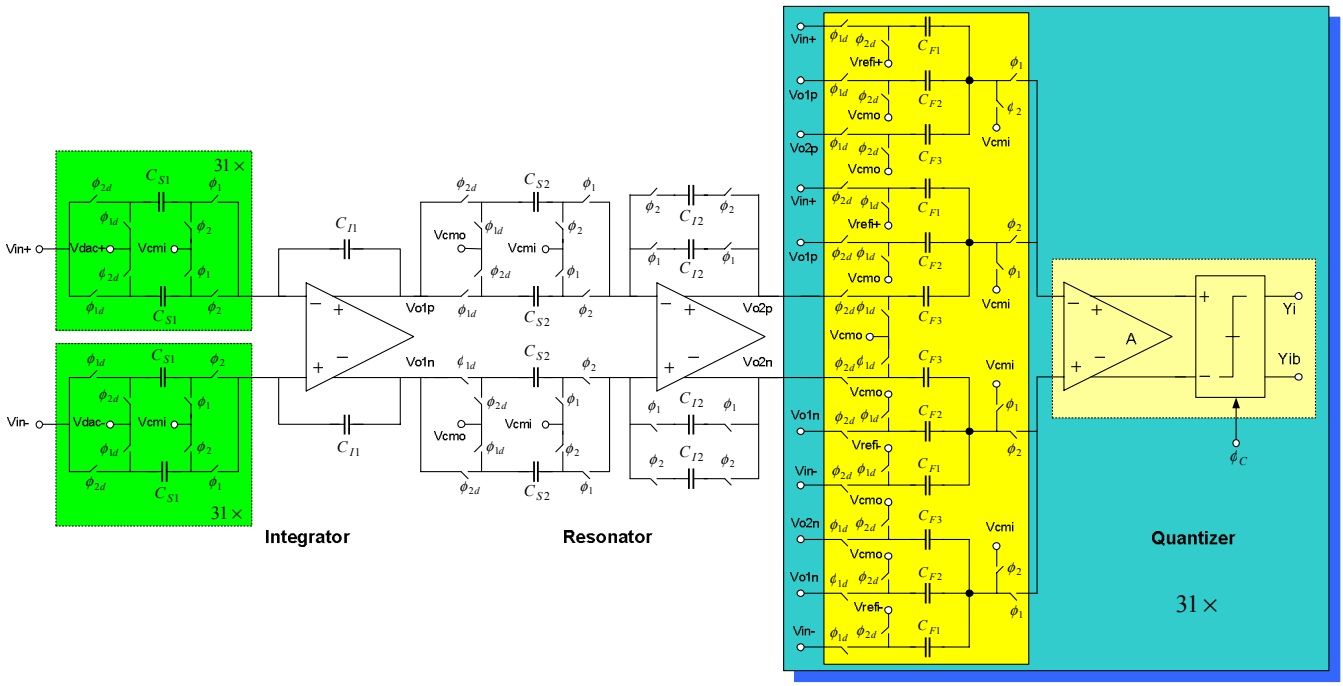

Fig. 9: Switched-capacitor implementation of the proposed second-order modulator.

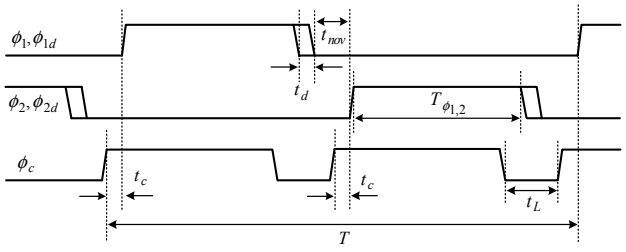

Fig. 10: Clock waveforms.

Figure 10 shows the clock waveforms. Two non-overlapping clock phases and their delayed versions are used for sampling and integrating. Another clock phase is needed in the comparators. As shown in Fig. 10, ϕ_c is used to regenerate the latches of the comparators. When ϕ_c is low, the latches are in regeneration. As ϕ_c goes to high, the latches are in the reset mode. This clock phase can be realized by a simple gating of the main non-overlapping clocks.

It is worth mentioning that since the charge transferring of the DAC sampling capacitors is performed without any delay, the unit feedback delay of the first integrator is devoted to the quantizer and DAC linearization technique. To compensate the errors resulted from the DAC unit elements mismatch, DAC linearization techniques such as DWA can also be used [1].

5. CONCLUSIONS

In this paper, novel double-sampled second-order and cascaded sigma delta modulator topologies for broadband applications were proposed. To alleviate the quantization noise folding effect into the signal band and to achieve the aggressive noise shaping with low OSRs, an FIR NTF with an additional zero at $f_s/2$ was used. Unity-gain STF was employed to decrease the modulator's sensitivity to the circuit non-idealities. Only one multibit DAC is needed in the feedback loop which greatly decreases the circuit implementation complexity.

6. REFERENCES

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