HIGH-ORDER SINGLE-LOOP DOUBLE-SAMPLING SIGMA-DELTA MODULATOR TOPOLOGIES FOR BROADBAND APPLICATIONS

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ABSTRACT

This paper presents novel low-voltage high order single loop sigma-delta modulator structures for wideband applications. The proposed architectures employ the technique of double-sampling to double the effective oversampling ratio (OSR) without increasing the sampling frequency. To alleviate the quantization noise folding into the inband frequency region which is a result of the mismatch between the sampling capacitors of the feedback's digital-to-analog converter (DAC) paths, a zero is placed at the half of the sampling frequency of the modulator's noise transfer function (NTF). The problem of this additional zero in the NTF is solved through the proposed modulator architectures with a very simple design procedure.

1. INTRODUCTION

Sigma-delta ADCs are the main candidates for high resolution due to their inherent immunity to the circuit non-idealities. In order to employ them in broadband applications, a low oversampling ratio (OSR) must be considered. But, the reduction of OSR decreases the accuracy of the modulator, drastically. So, novel modulator structures are needed to alleviate the reduction of resolution in low OSR applications.

A useful approach in switched-capacitor realizations of the modulators is to employ the double-sampling technique. In this method, the circuit operates during both phases of the clock. Hence, the effective sampling frequency of the system is twice that of the clock frequency. This results in doubling the OSR and/or the available time for settling of the integrators if OSR is fixed. Fig. 1 shows a single-ended double-sampling integrator. In this circuit, two distinct capacitors are used to sample the input signal. The capacitor C_{S1} is used to sample the input signal at the phase ϕ_1 while at this interval the stored charge on C_{S2} is transferred into the integrating capacitor, C_I. At the next phase, C_{S2} samples the input signal and C_{S1} transfers its stored charge into C_I. Hence, in both phases of the clock, the sampling and integrating is performed resulting in doubling the effective sampling rate of the system. Unfortunately, double-sampling sigma-delta modulators are sensitive to the mismatch between the two sampling capacitors, C_{S1} and C_{S2}. This results in folding the quantization noise into the signal band through the paths of the feedback DAC. Several techniques have been proposed to alleviate the quantization noise folding in doubled-sampled modulators such as employing fully floating method in the feedback DAC paths and/or placing a zero at the half of the sampling frequency of the NTF, etc [1-3].

The effect of placing a zero at the half of the sampling frequency ($f_s/2$) of the NTF should be considered in the design of the modulator's NTF. Its effect is not considerable in the first and second order modulators. But, the NTF of high order structures is affected drastically using both above-mentioned techniques resulting in ineffective and even unstable modulators. So, the design of a stable high order double-sampling modulator with a zero at $f_s/2$ would be complicated. In [4] a systematic procedure has been proposed to design the stable double-sampling modulators. But, this technique is complex and results in the modulator structures that are not efficient for wideband applications mainly due to the fact that they employ several multibit DACs in the modulator's loop which results in more area, power, and circuit complexity.

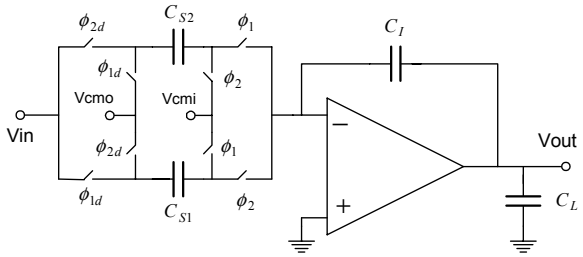

Figure 1: Single-ended double-sampling integrator.

In this paper, novel sigma-delta modulator topologies employing the double-sampling technique are proposed. The proposed modulator structures employ finite impulse response (FIR) NTF with a zero at $f_s/2$. The paper is organized as follows. Section (2) describes the derivations of the proposed modulator structures. In section (2) the circuit requirements to realize the proposed modulators are also described. Section (3) provides simulation results. The conclusions are given in section (4).

2. PROPOSED MODULATOR TOPOLOGIES

The general structure of a sigma-delta modulator is shown in Fig. 2 where $H(z)$ is the loop transfer function and its NTF is given by

$$NTF(z) = \frac{1}{1 + H(z)} \tag{1}$$

In this structure the signal transfer function (STF) is unity. Unity gain STF in a sigma-delta ADC has many advantages such as the followings. First, the effects of the circuit non-idealities such as the limited opamp DC gain and nonlinearities are reduced since only the quantization noise is processed by the integrators [5]. Second, the dynamic range is increased because the quantizer tracks the input signal through a direct path to the its input. Third, the integrators need small output swings since only the quantization noise is processed by them.

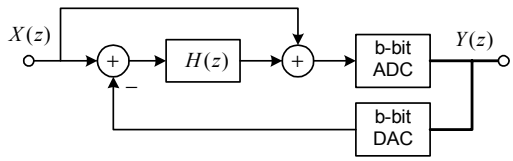

Figure 2: General structure of a sigma-delta modulator.

The loop transfer function, $H(z)$, can be obtained in term of the NTF as follows:

$$H(z)=\frac{1-NTF(z)}{NTF(z)} \tag{2}$$

The NTF of the proposed double-sampling sigma delta modulators is considered as FIR filter as follows:

$$NTF(z)=\begin{cases}(1-z^{-1})(1+z^{-1})\prod_{i=1}^{M}(1-\alpha_i z^{-1}+z^{-2}) & \text{if } L \text{ is odd}\\ (1-z^{-1})^2(1+z^{-1})\prod_{i=1}^{M-1}(1-\alpha_i z^{-1}+z^{-2}) & \text{if } L \text{ is even}\end{cases} \tag{3}$$

where M = [L/2] and L is the order of the modulator and is considered greater than two. For the second order structure only the first two terms of the NTF is assumed. A zero is placed at $f_s/2$ of the NTF through the term of $(1+z^{-1})$ to reduce the folding effect of the quantization noise into the signal band which is a result of the paths gain mismatch between the feedback DAC capacitors as discussed above. The term $(1-z^{-1})$ is needed to realize the input stage of the modulator as an integrator without any local feedback DAC. For odd order modulators only one zero of the NTF is placed at DC and the other zeros are located in the inband frequencies to shape out the quantization noise aggressively. For even order structures two zeros of the NTF are located at DC and the others at the inband frequencies. Another zero at DC is needed in even order modulators compared to the odd order structures in order to remove the requirement of the local feedback DAC around first pair of integrators. It is worth mentioning that the local feedback DAC around the first pair of integrators enhances the kT/C noise of the modulator, directly.

The loop transfer function, $H(z)$, of the proposed modulators is obtained with relations (2) and (3). For example, $H(z)$ of the second and third order modulators is as follows, respectively:

$$H_2(z)=\frac{z^{-1}}{1-z^{-1}}\frac{1+z^{-1}-z^{-2}}{1-z^{-2}}=\frac{z^{-1}}{1-z^{-1}}\left(1+\frac{z^{-1}}{1-z^{-2}}\right) \tag{4}$$

$$H_3(z)=\frac{z^{-1}}{1-z^{-1}}\left(\alpha+\frac{\alpha(\alpha-1)z^{-1}+\alpha(\alpha-2)z^{-2}+(1-\alpha)z^{-3}}{1+(1-\alpha)z^{-1}+(1-\alpha)z^{-2}+z^{-3}}\right) \tag{5}$$

As it is seen, the loop transfer function, $H(z)$, of the proposed modulators can be realized as an integrator and an infinite impulse response (IIR) filter. For example, the realization of the proposed third order modulator is shown in Fig. 3 where only one integrator and a third order IIR filter is used for its implementation. Although such realization of the proposed FIR NTF double-sampling modulators can be obtained using switched-capacitor circuits in CMOS technologies, but the number of the modulator coefficients becomes large for high order structures. So this realization will be more sensitive to the mismatch between the coefficients. The other drawback of this realization is the existing of three paths terminating to the input of the quantizer which demands a delay free gain stage. So, an efficient implementation which needs lower number of coefficients and minimum terminating paths to the quantizer input is proposed in the following. This realization uses only one first order IIR filter and more integrators to reduce the number of modulator coefficients.

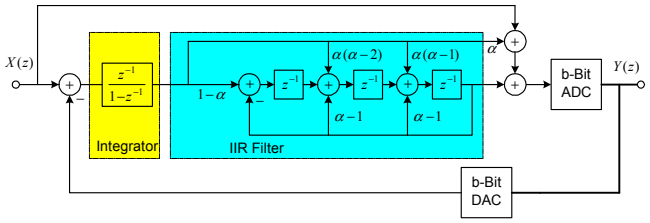

Figure 3: Third order double-sampling modulator.

The proposed NTF for double-sampling modulators can also be implemented efficiently as the combination of the integrators and only one first order IIR filter as shown for the third, fourth and fifth order modulators in Figs. 4, 5 and 6, respectively. In this realization, the summer at the input of the quantizer can be implemented with a passive switched-capacitor circuit as proposed in [5]. But, in the passive realization of this summer a loss of two is obtained where it should be compensated by the quantizer. This means that the voltage reference of the quantizer should be reduced by two making the design of the quantizer especially in low voltage circuits complicated. However, the realization of a 4-5 bit flash ADC with one bit higher accuracy which is used in the loop of sigma-delta modulators is not very complex. The realization of high order modulators can be obtained with a straight forward extension of the proposed structures. As it is seen to realize the even order modulators (see Fig. 5), the structure is somewhat different and needs other delays in the modulator feedforward paths coefficients. However, the term $(1+z^{-1})$ can be realized using fully floating technique as proposed in [1] without any effective extra circuit requirement.

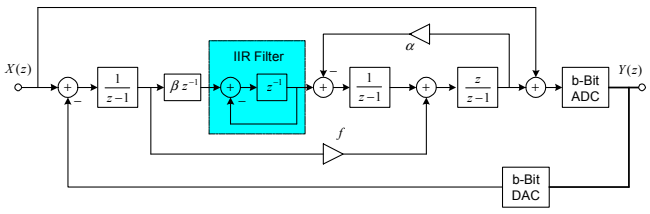

Figure 4: The proposed third order double-sampling modulator.

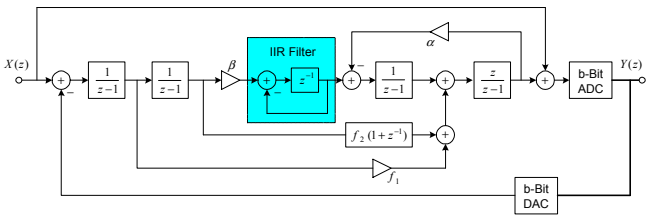

Figure 5: The proposed fourth order double-sampling modulator.

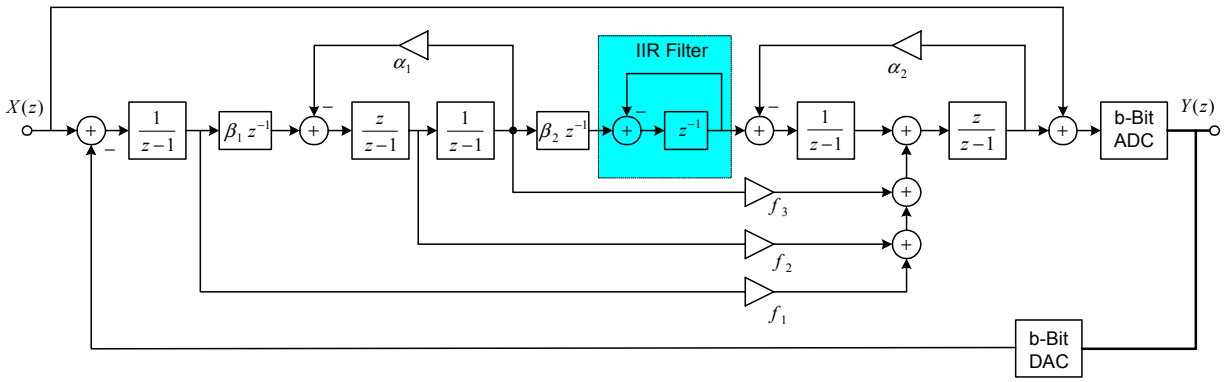

Figure 6: The proposed fifth order double-sampling modulator.

The coefficients of the proposed modulators to obtain the FIR NTF for the third, fourth and fifth order structures are as follows:

$$\beta = 1, \quad f = 2 - \alpha \qquad \text{for} \quad L = 3 \tag{6}$$

$$\beta = 1, \quad f_1 = 3 - \alpha, \quad f_2 = 1 \qquad \text{for} \quad L = 4 \tag{7}$$

$$\beta_1 = \beta_2 = 1, \quad f_1 = 4 - \alpha_1 - \alpha_2 \quad f_2 = f_3 = 3 - \alpha_1 \; (4 - \alpha_1) \qquad \text{for} \quad L = 5 \tag{8}$$

The coefficients α_i are needed to place some of NTF's zeros at the inband frequencies. The design method proposed by Schreier [6] can be used to obtain the values of α_i in order to place the inband zeros at the optimal points. The other coefficients are obtained such that the NTF become an FIR filter as given in the relations (6)-(8) for the proposed third, fourth and fifth order modulators.

To realize the IIR filters, the generic low-Q biquad structure can be used [7]. The unit delays of the feedforward paths can be implemented with appropriate designing of the clock phases in switched-capacitor circuits without any extra circuit [8].

3. SIMULATION RESULTS

To show the usefulness of the proposed modulator topologies, their system level architectures taken into account the circuit non-idealities were simulated. Simulation results of the proposed third, fourth and fifth order structures shown in Figs. 4, 5 and 6 are only presented here.

To get the optimal location of the inband zeros, MATLAB with Schreier's Delta-Sigma Toolbox [9] was used. The proposed modulators were designed for OSR = 8 and b = 5. The values of α = 0.092, α = 0.109 and α_1 = 0.125, α_2 = 0.045 were obtained for the third, fourth and fifth order modulators, respectively. The other coefficients of the modulators were determined from the relations (6), (7) and (8). Then, signal scaling was performed to limit the output swing of the integrators and the other blocks for a real implementation. A gain is placed in the input signal path of the first integrator to achieve the overload level factor of one for all three structures with a safety margin. The value of this gain is 0.875, 0.8 and 0.6 for the third, fourth, and fifth order architectures, respectively. The resultant ideal maximum SNDR for a 0-dBFS sinusoidal input is about 73 dB, 84.4 dB and 98 dB for the third, fourth and fifth order modulators, respectively. Figure 7 shows the output spectrum of the simulated modulators.

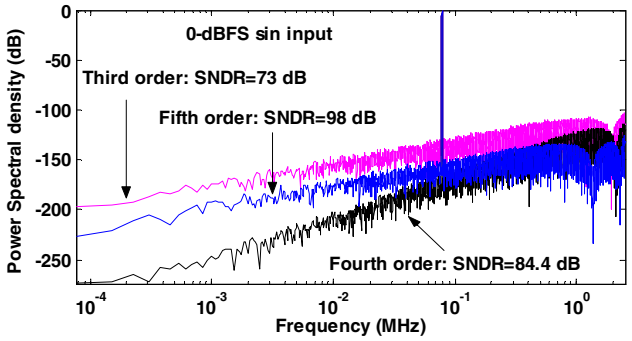

Figure 7: Power spectral density.

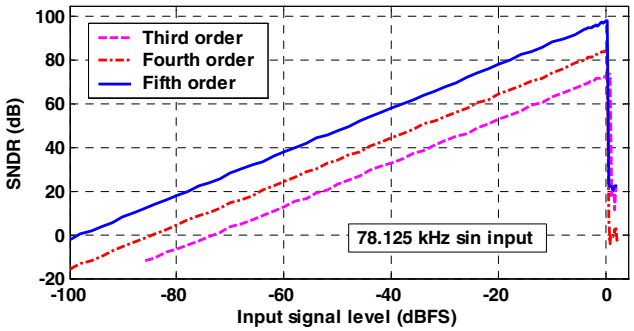

Figure 8: Dynamic range: SNDR vs. input signal level.

In Fig. 8 SNDR is shown versus the input signal level of the proposed modulators. As it is seen the proposed modulators are stable for an input signal with amplitude greater than of the feedback reference level. This is mainly due to a direct path from the input signal to the quantizer input which results in a wide input signal range.

Simulation results also show that the SNDR degradation versus the mismatch error of the modulator coefficients is negligible even with a coefficients mismatch of 5% if the gain of paths is completely matched.

The main concern of double-sampled modulators is the quantization noise folding due to the paths gain mismatches of the feedback DAC capacitors. Figure 9 shows SNDR versus the mismatch of the sampling paths of the first integrator. As it is seen the SNDR degradation of the proposed third order modulator is

negligible even with a 1% mismatch between the sampling paths. With a mismatch of 0.3%, SNDR of the proposed fourth order modulator degrades about 1 dB. However, the proposed fifth order is more sensitive to the mismatch between the sampling paths. With a mismatch of 0.05% between the sampling paths of the first integrator, SNDR degrades about 4 dB. The paths mismatch of the remaining blocks does not affect the SNDR of the fifth order modulator considerably even with a 0.2% mismatch. However it should be noted that since the sampling capacitors of the first integrator are large due to the circuit noise considerations, a paths mismatch of about 0.05% is realizable as well [2].

The other circuit requirements of the proposed architectures such as the amplifier finite DC gain are more relaxed and simulation results show that about 40 dB DC gain for the first integrator is sufficient to prevent any SNDR degradation with an enough margin (about 10 dB). The proposed architectures have small output swings compared to the conventional distributed feedback and weighted feedforward architectures [10] due to the unity-gain STF and also feedforward paths.

In these simulations ideal DAC elements have been assumed. However, in the real implementations, dynamic element matching (DEM) such as data weighted averaging (DWA) and calibration or correction techniques can be used to correct the DAC errors [10, 11]. It is worth mentioning that only one DAC is used in the proposed modulators and it is located at the input of the first integrator. The value of the sampling and feedback capacitors of this integrator are determined due to the kT/C noise considerations and their sizes are large in the high-resolution and low-voltage applications.

The main features of the proposed modulator structures are summarized as follows.

1. Due to the single loop structure they are suitable for very low-voltage applications because the proposed topologies demand the relaxed analog circuit requirements.
2. High speed applications can be obtained using low speed clock frequencies. This is achieved using the double-sampling technique.
3. Only one multibit DAC is used in the loop of the modulator. This decreases the circuit complexity, greatly.
4. FIR NTF is used to achieve the aggressive shaping of the quantization noise and a very simple design of the modulator transfer function. Most of the NTF zeros are placed at the inband frequency region to shape out the quantization aggressively.
5. Only two paths are terminated to the input of the quantizer. This results in the realization of the summer preceding the quantizer as a passive switched-capacitor circuit.

4. CONCLUSION

In this paper, novel single loop sigma delta modulator topologies for broadband applications in the low-voltage environments using only a low OSR were proposed. To alleviate the quantization noise folding effect into the signal band, an FIR NTF with an additional zero at $f_s/2$ was used. Unity-gain STF was employed to decrease the modulator's sensitivity to the circuit non-idealities. Only one multibit DAC is needed in the feedback loop which greatly decreases the circuit implementation complexity. To compensate the errors resulted from the DAC unit elements mismatch, DAC linearization techniques such as DWA can also be used.

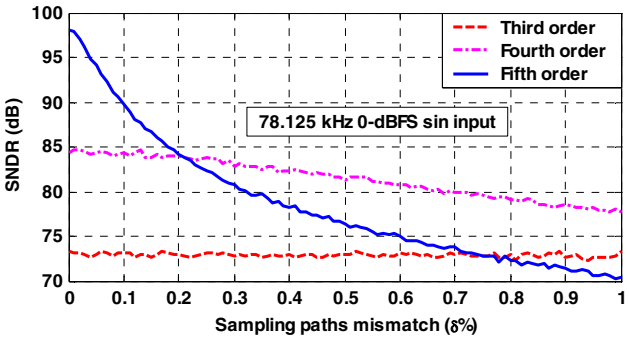

Figure 9: SNDR versus the mismatch of the sampling paths.

$$\delta = (C_{S1} - C_{S2})/(C_{S1} + C_{S2})$$

5. REFERENCES

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