LOW-VOLTAGE SIGMA-DELTA MODULATOR TOPOLOGIES FOR BROADBAND APPLICATIONS

Mohammad Yavari and Omid Shoaei

IC Design Lab, ECE Department, University of Tehran, Tehran 14395-515, Iran

E-mails: myavari@ut.ac.ir and oshoaei@ut.ac.ir

ABSTRACT

This paper presents a novel class of sigma-delta modulator topologies for low-voltage, high-speed, and high-resolution applications with low oversampling ratios (OSRs). The main specifications of these architectures are the reduced analog circuit requirements, large out-of-band gain in the noise transfer function (NTF) without any stability concerns to achieve high signal to noise ratio (SNR) with a low OSR, and unity-gain signal transfer function (STF) to reduce the harmonic distortions resulted from the analog circuit imperfections.

1. INTRODUCTION

With the recent developments in both wired and wireless communications, there is a need to design analog-to-digital converters (ADCs) at MHz speeds with high linearity at low voltage environments. Sigma-delta modulators and pipelined ADCs are the two main candidates for high-resolution and high-speed applications. Pipelined converters need some type of calibration or error correction techniques to achieve accuracies beyond 12-bits, resulting in increased complexity and power dissipation [1]. Several sigma-delta ADCs have been reported in the MHz range with resolutions of about 14-bits and beyond [2-6]. However, all of them operate on supply voltages greater than 1.8-V. In this paper a novel class of sigma-delta modulator architectures suitable for very low-voltage and high-resolution applications in the MHz ranges is proposed.

Section (2) reviews sigma-delta modulator architectures and discusses what type of them is suitable for low-voltage applications. The proposed class of modulator architectures is presented in section (3). Section (4) provides simulation results. Section (5) concludes the paper.

2. MODULATOR TOPOLOGIES

The main sigma-delta modulator topologies are classified as single-loop and cascaded architectures [7]. Cascaded architectures use combination of inherently stable first and second order modulators to achieve higher order noise shaping. But, they need high dc gain opamps to implement the used integrators to prevent the quantization noise leakage of the first stage ADCs which limit their usefulness in the low-voltage applications [4, 5]. Single-loop modulators demand lower dc gain opamps. Besides, their other circuit requirements are more relaxed compared to their cascaded counterparts at the expense of being more prone to instability and reduced signal-to-noise ratio. Stability is the main concern in the design of high order single loop modulators which relates to the NTF's out-of-band gain directly. Increasing the modulator's NTF's out-of-band gain enhances its resolution at the cost of degradation of its stability likelihood. On the other hand, reducing NTF's out-of-band gain increases the likelihood of success, but reduces the magnitude of the quantization noise attenuation provided by NTF and thus the theoretical resolution of the modulator [8].

Both single-loop and cascaded architectures can utilize either single-bit or multibit quantizers. In the design of sigma-delta modulators for high-speed applications a low oversampling ratio (OSR) must be used where this weakens the advantages of oversampling. To compensate for this loss in resolution a high order with a multibit modulator can be used. It is worth to mention that the impact of increasing the modulator order on the dynamic range (DR) diminishes as the oversampling ratio is reduced. In contrast, the effectiveness of increasing the internal quatizer resolution (using a multibit modulator) is independent of the OSR. Each extra bit of quantizer increases the modulator resolution about one bit independent of OSR. The other advantages of multibit quantization include reduced analog circuit requirements such as the OTA settling and enhanced modulator stability especially in high order single loop architectures. Multibit quantization improves the modulator stability and its input signal range. With multibit quantization one can achieve aggressive noise shaping and/or wide input signal range in high order modulator structures compared to their single bit quantization counterparts [9]. However, errors due to non-idealities in the feedback DAC add directly to the input signal and hence are not shaped by the modulator. Thus, the resolution of a multibit modulator is limited by the linearity of its multibit DAC unit elements. Fortunately, two signal processing techniques have been developed to correct the DAC non-idealities: dynamic element matching (DEM) and calibration or correction. In this paper data weighted averaging (DWA) one type of DEM is used to correct the DAC errors [10].

The two well-known high order single-loop modulators are distributed feedback (DFB) and weighted feedforward (WFF) architectures with local resonators [7]. One drawback of the DFB topology is that the integrators outputs contain significant amount of the input signal as well as the shaped quantization noise. In switched-capacitor (SC) implementations, the output swings must be limited to stay within the available supply range by proper scaling of the modulator coefficients. This results in large modulator coefficients spread and small integrators gain. Small integrator gain increases the integrating capacitance because the sampling capacitor is determined by kT/C noise

and/or matching requirements. So, the circuits used in distributed feedback topologies tend to be larger and more power hungry than those needed for the feedforward topologies. Similarly, large coefficients spread results in large capacitor requirement.

The main drawbacks of the DFB and WFF architectures are as follows: 1) One of the aggressive noise shaping and wide input signal range can be obtained only by using the multibit quantization. 2) Large integrators output swing which demands large swing OTAs for implementation. 3) High modulator coefficients spread compared to the proposed modulator architectures in this paper. High coefficients spread not only leads to more power and area consumption, but it is also an indication of high coefficient sensitivity and poor stability.

3. PROPOSED TOPOLOGIES

The proposed single loop modulator architectures in this paper can have aggressive noise shaping with wide input signal range that have not been possible using the previously reported high order single loop structures. Also, the needed circuits for implementation of the proposed architectures are more relaxed compared to the existing single loop architectures.

Figs. 1 and 2 show the proposed fourth and sixth order modulator topologies, where *f* is the gain of a feedforward path, *g* and β are the gains of the first and last integrators, respectively, and *H(z)* is an infinite impulse response (IIR) filter with the following transfer function:

$$H(z)=\frac{b_1 z^{-1}+b_2 z^{-2}}{1-a_1 z^{-1}-a_2 z^{-2}}. \quad (1)$$

It is worth to mention that the order of the modulator can be extended to even higher orders with a straightforward extension. For example the eighth order will use three IIR filters with two integrators.

The main features of the proposed modulator architectures are as follows. 1) Using IIR filters instead of conventional integrators in the middle of modulator architecture to implement an aggressive noise shaping NTF. Only two integrators are used: one at the input and the other at the end. 2) Unity gain STF to reduce the imperfections resulted from analog circuits non-idealities and eliminate the drawbacks resulted from phase nonlinearity of IIR filters and also to extend the stable input signal range to enhance the modulator's dynamic range. 3) Low output swing integrators and IIR blocks. 4) Simple relation between noise transfer function and its zeros. 5) Very low coefficients spread compared to the existing high order single loop modulators such as DFB and WFF topologies.

In the proposed architectures IIR filters are used to achieve a high out-of-band gain in the modulator's NTF similar to [2], resulting in aggressive noise shaping and hence the increased SNR and reduced tones at the modulator's output spectrum without any concern to instability. The major concern to select IIR filters in sigma-delta modulators is their nonlinear phase properties which results in harmonic distortion particularly notable at the presence of two strong tones at the modulator's input. In the proposed architectures, the phase nonlinearity was resolved making use of a unity-gain STF. Choosing a unity-gain STF not only reduces the harmonic distortions resulted from analog circuit imperfections such as finite dc gain opamps [11] but also the integrators and IIR blocks process only quantization noise which results in low output swing integrators and IIR blocks. Also unity gain STF extends the modulator's dynamic range through a direct path to the quantizer input. Simulation results indicate that about 4-dB improvement in DR is achieved by making the STF gain at unity. The proposed architectures use only one DAC which greatly reduces the circuit complexity at low-voltage applications. The forward paths terminated to the input of quantizer can be implemented using a passive switched-capacitor circuit as proposed in [11]. But, it can reduce the least significance bit (LSB) of quantizer whose design can be very complex in very low-voltage applications. Unlike the DFB modulator structure, the quantizer input in the proposed architectures senses input signal from two another lower delay paths: one directly and another through the *f* feedforward path. This causes that the quantizer senses the input signal jumps directly and stabilizes the modulator through the negative feedback fast, hence to enhance the modulator's dynamic range.

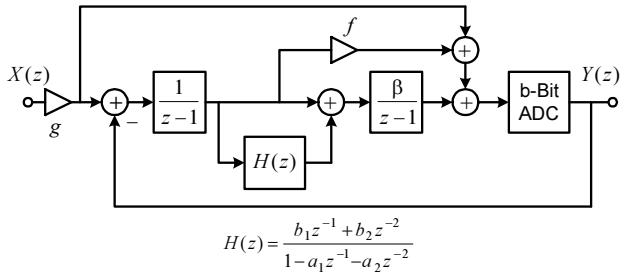

Figure 1: The proposed fourth order sigma-delta modulator topology.

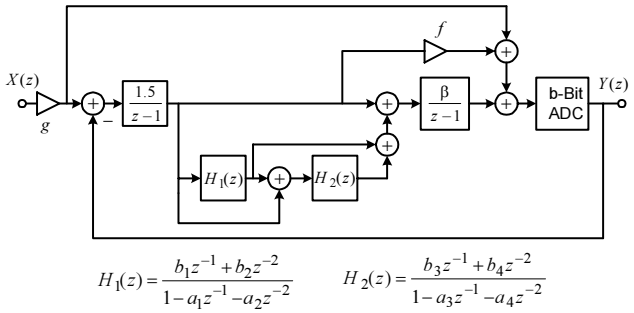

Figure 2: The proposed sixth order sigma-delta modulator topology.

It can be shown that the NTF of the proposed fourth and sixth order modulators coefficients are as follows:

$$H_{Q4}(z)=\frac{(z-1)^2(z^2-a_1 z-a_2)}{z^4+d_3 z^3+d_2 z^2+d_1 z+d_0} \quad (2)$$

$$d_3=-a_1+f-2 \quad (3)$$

$$d_2=-a_2+2a_1+\beta-f a_1+1-f \quad (4)$$

$$d_1 = 2a_2 - a_1 - \beta a_1 + \beta b_1 - f a_2 + f a_1 \quad (5)$$

$$d_0 = -a_2 - \beta a_2 + \beta b_2 + f a_2 \quad (6)$$

$$H_{Q6}(z) = \frac{(z-1)^2 (z^2 - a_1 z - a_2)(z^2 - a_3 z - a_4)}{z^6 + d_5 z^5 + d_4 z^4 + d_3 z^3 + d_2 z^2 + d_1 z + d_0} \quad (7)$$

$$d_5 = -(a_1 + a_3 + 2) + 1.5 f \quad (8)$$

$$d_4 = 1 + (2 - 1.5 f)(a_1 + a_3) - (a_2 + a_4 - a_1 a_3) - 1.5 f + 1.5 \beta \quad (9)$$

$$d_3 = (2 - 1.5 f)(a_2 + a_4 - a_1 a_3) + (a_1 a_4 + a_2 a_3) + (1.5 f - 1.5 \beta - 1)(a_1 + a_3) + 1.5 \beta (b_1 + b_3) \quad (10)$$

$$d_2 = a_2 a_4 + (1.5 f - 2)(a_1 a_4 + a_2 a_3) + (1.5 f - 1.5 \beta - 1)(a_2 + a_4 - a_1 a_3) + 1.5 \beta (b_2 + b_4 - b_1 a_3 - a_1 b_3 + b_1 b_3) \quad (11)$$

$$d_1 = (1 + 1.5 \beta - 1.5 f)(a_1 a_4 + a_2 a_3) + a_2 a_4 (1.5 f - 2) + 1.5 \beta (b_2 b_3 + b_1 b_4 - b_1 a_4 - b_2 a_3 - a_1 b_4 - a_2 b_3) \quad (12)$$

$$d_0 = a_2 a_4 (1 + 1.5 \beta - 1.5 f) + 1.5 \beta (b_2 b_4 - a_2 b_4 - a_4 b_2) \quad (13)$$

where $H_{Q4}(z)$ and $H_{Q6}(z)$ are the NTFs of fourth and sixth order proposed modulators, respectively.

4. SIMULATION RESULTS

To obtain the modulators coefficients MATLAB with Schreier's Delta-Sigma toolbox [12] was used. Sixth and fourth order modulators were designed with OSR=8 and b=5. It is worth to mention here that the OSR and number of quantizer bits were selected arbitrary to show the efficiency of proposed modulators.

Designed modulators' NTFs for fourth and sixth order architectures are as follows:

$$H_{Q4}(z) = \frac{(z-1)^2 (z^2 - 1.891 z + 1)}{z^4 - 0.660 z^3 + 0.570 z^2 - 0.017 z + 0.176} \quad (14)$$

$$H_{Q6}(z) = \frac{(z-1)^2 (z^2 - 1.937 z + 1)(z^2 - 1.868 z + 1)}{D(z)}$$

$$D(z) = z^6 - 1.996 z^5 + 2.231 z^4 - 1.467 z^3 + 0.671 z^2 - 0.179 z + 0.030 \quad (15)$$

Table 1 shows the modulators coefficients which were obtained with solving the equations (2-15) with MATLAB. The resultant maximum SNDR's are 103-dB and 86.5-dB for the sixth and fourth order modulators, respectively. The NTF's out-of-band gain of designed modulators is about 18-dB and 16-dB for the sixth and fourth order modulators, respectively, as opposed to the conventional single-loop DFB and WFF modulators that is much less than this.

In Fig. 3 SNDR versus input signal level of the proposed modulators is shown. The resultant DR's are 86 dB and 103 dB for the fourth and sixth orders, respectively. The overload level factor of the sixth order is about 0-dBFS where the fourth order is stable for input signals about 1.8 dB higher than the feedback reference levels. This is due to a direct path from the input signal to the quantizer input which results in a wide input signal range.

The proposed architectures have small output swings compared to the DFB and WFF architectures. Also the coefficients spread of the proposed architectures as shown in Table 1 is much less than the conventional DFB and WFF structures.

Table 1: Simulated Modulators coefficients.

Sixth order modulator coefficients					
a1	a2	b1	b2	f	g
1.937	-1	0.580	-0.500	2.539	0.5
a3	a4	b3	b4	β	
1.868	-1	0.288	-0.102	4.203	
Fourth order modulator coefficients					
a1	a2	b1	b2	β	f	g
1.891	-1	0.567	-0.460	4.128	3.231	0.5

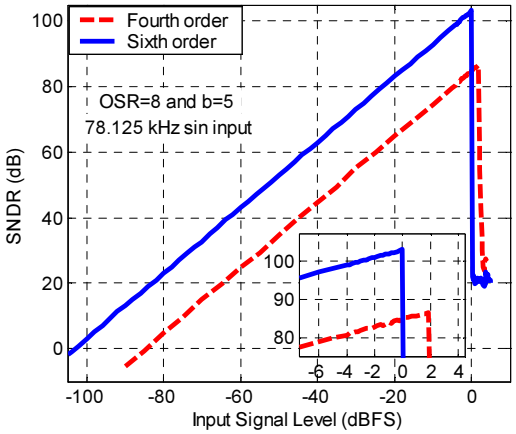

Figure 3: Dynamic range: SNDR versus input signal level.

Fig. 4 shows the SNDR degradation versus mismatch error of modulator coefficients. To obtain this plot the modulator coefficients were considered independent Gaussian random variables with mean values shown in Table 1 and variances as a variable indicating the mismatch error. The mismatch was considered as three time of standard deviation of these Gaussian random distributions. For each mismatch value two hundred simulations were performed and average SNDR was considered. As shown in Fig. 4 SNDR degradation is negligible with coefficient mismatches less than 1% which is well achievable with existing modern CMOS technologies. In these simulations ideal DAC elements have been used. In order to account the DAC errors in the simulations a mismatch of 0.1% between DAC unit elements was considered. This matching requirement can be achieved using large capacitors for DAC arrays. It is worth to mention that only one DAC is used in the proposed modulators and it is located at the input of first integrator. The values of sampling and feedback capacitors of this integrator are determined due to kT/C noise considerations and their sizes are large in the high-resolution applications. Fig. 5 shows the effect of DAC mismatch errors on the proposed modulators' performance. The SNDR degradation is about 6.5-dB and 14-dB for the fourth and sixth order modulators, respectively. Also strong tones appeared at the outputs which greatly decreases the

SFDR. DWA was used to compensate this degradation. As shown in Fig. 5 the loss of SNDR is at most 0.5-dB and 3-dB using DWA DAC linearization technique for the fourth and sixth order modulators, respectively, and the tones are removed nearly completely.

The other circuit requirements of the proposed architectures such as amplifier finite dc gain are more relaxed and simulation results show that the 40 dB dc gain for the first integrator is sufficient to prevent any SNDR degradation with enough margin (about 10 dB).

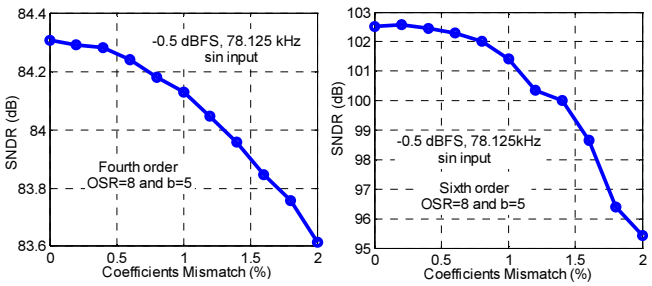

Figure 4: SNDR versus the modulators coefficients mismatch errors.

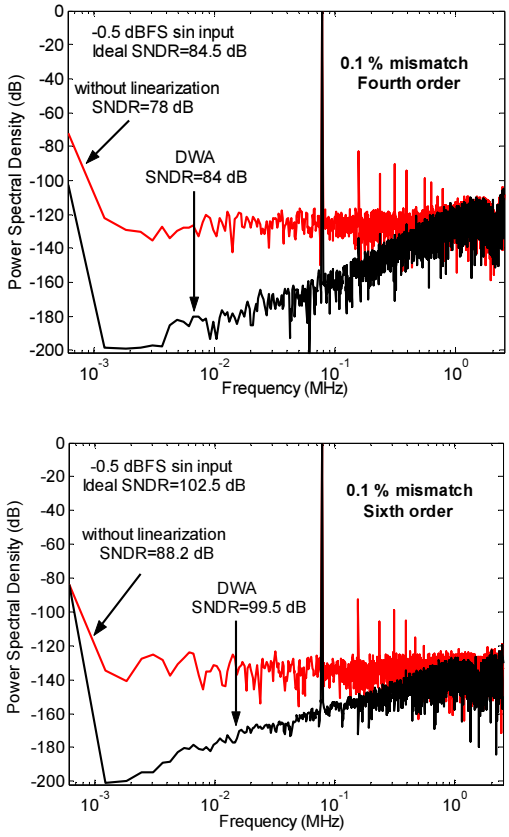

Figure 5: DAC errors effect on SNDR and its linearization with DWA.

5. CONCLUSIONS

In this paper a new class of single-loop multibit sigma-delta modulator topologies suitable for low-voltage and high-resolution applications in the MHz ranges was proposed using only a low OSR. They have unity-gain STF to alleviate the SNDR degradation due to circuit imperfections and high maximum out-of-band gain in their NTFs without any stability concerns to achieve the high SNDR with only a low OSR. Only one multibit DAC is needed in the feedback loop which greatly decreases the implementation complexity. To compensate the errors resulted from DAC unit elements, DAC linearization techniques such as DWA can be used.

6. ACKNOWLEDGMENTS

The authors would like to thank Professor G. Temes and Mr. J. Silva for useful comments.

7. REFERENCES

[1] J. M. Ingino and B. Wooley, "A continuously calibrated 12-b 10MS/s 3.3 V A/D converter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1920-1931, Dec. 1998.

[2] R. Jiang and T. S. Fiez, "A 1.8V ΔΣ A/D converter with 4MSample/s conversion," *ISSCC Digest Technical Papers*, Feb. 2002.

[3] Y. Geerts, M. Steyaert, and W. Sansen, "A high-performance multi-bit ΔΣ CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829-1840, Dec. 2000.

[4] I. Fujimori et al., "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8× oversampling," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820-1828, Dec. 2000.

[5] K. Vleugels, S. Rabii, and B. Wooley, "A 2.5-V sigma-delta modulator for broadband communications applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp.1887-1899, Dec. 2001.

[6] R. Reutemann, P. Balmelli, Q. Huang, "A 33mW 14b 2.5MSample/s ΣΔ A/D converter in 0.25μm digital CMOS," *ISSCC Digest Tech. Papers*, pp. 316-317, Feb. 2002.

[7] S. R. Northworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters*, Piscataway, NJ: IEEE Press, 1997.

[8] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Transactions on Circuits and Systems-II*, vol. 40, no. 8, pp. 461-466, Aug. 1993.

[9] P. Ju and K. Suyama, "Design considerations in high-order multi-bit sigma-delta modulators," *IEEE International Symposium on Circuits and Systems*, pp. 389-392, June 1997.

[10] R. T. Baird and T. Fiez, "Linearity enhancement of multibit delta-sigma A/D and D/A converters using data weighted averaging," *IEEE Transactions on Circuits and Systems, II,* vol. 42, no.12, pp. 753-762, Dec. 1995.

[11] J. Silva, U. Moon, J. Steensgaard, and G. Temes, "Wideband low-distortion delta-sigma ADC topology," *IEE Electronics Letters*, vol. 37, no. 12, pp. 737-738, July 2001.

[12] R. Schreier, *Delta-Sigma Toolbox, available at: http://www.mathworks.com/matlabcentral/fileexchange*.