Very Low-Voltage, Low-Power and Fast-Settling OTA for Switched-Capacitor Applications

Mohammad Yavari and Omid Shoaei

IC Design Lab, ECE Department, University of Tehran, Tehran, Iran
P.O. +98-21- 14395-515
Email: mmyavari@yahoo.com

ABSTRACT

This paper presents a new fully differential operational trans-conductance amplifier (OTA) for very low-voltage and fast settling switched capacitor circuits in digital CMOS technology. The proposed two-stage OTA is a hybrid class A/AB that combines a folded cascode as the first stage with active current mirrors as the second stage. Due to the class AB operation in the second stage, slew limiting only occurs in the first stage resulting in lower power dissipation for switched-capacitor circuits. It also employs the cascode compensation scheme for fast settling.

1. INTRODUCTION

The trend toward lower operating supply voltages and lower power consumption in mixed signal ICs has three strong motivations: 1) portable equipment capable of operating with minimum number of battery cells to reduce volume and weight, 2) voltage limitations resulted from smaller feature sizes of modern IC technologies, and 3) longer operating periods without battery recharging or replacement.

Design of high performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in an analog circuit is the operational amplifier. The realization of a CMOS operational amplifier that combines high dc gain with high unity gain bandwidth has been a difficult problem especially in low voltage circuits. The high dc gain requirement leads to multistage designs or cascoding of transistors with long channel devices biased at low current levels, whereas the high unity gain frequency requirement calls for a single stage design with short channel devices biased at high bias current levels. Cascoding is a well-known means to enhance the dc gain of an amplifier without degrading the high frequency performance. But cascoding is not possible in the low voltage circuits, so a two-stage OTA is proposed to satisfy the high dc gain requirement for high speed applications in this paper.

In [1] a two-stage OTA has been used in a sigma-delta modulator for digital audio applications. The first stage of this OTA is a folded cascode and the second stage is a common source amplifier. Slew limiting in this OTA occurs in both stages. Therefore, in switched capacitor applications due to the large load capacitance of the OTA, the bias current of the second stage should be large which increases the power dissipation.

In [2] a two-stage class A/AB amplifier has been used in a sigma-delta modulator for audio applications. This OTA combines a simple differential pair as the first stage with active current mirrors as the second stage. The class AB operation in the second stage that causes the slew limiting only occur in the first stage. So it reduces the static power consumption. This OTA uses the standard miller compensation for stability and sufficient phase margin. Also the non-dominant pole of this OTA is twice the two-stage class A amplifier.

It has been shown that the cascode compensation scheme yields a higher amplifier bandwidth compared to the conventional miller compensation [3]. In this design a two-stage class A/AB OTA with cascode compensation has been proposed. The class AB structure of the second stage reduces the OTA's power consumption and the cascode compensation enhances its speed.

In section (2) the new merged OTA structure with common mode feedback (CMFB) circuits is introduced. Design procedure for this OTA is described in section (3). Section (4) presents simulation results. Finally, conclusions are summarized in section (5).

0-7803-7573-4/02/$17.00 © 2002 IEEE

2. PROPOSED OTA

Fig.1 shows the proposed OTA structure. The first stage is a folded cascode amplifier with PMOS input transistors. PMOS input differential pair allows the use of ground as the opamp input common mode voltage, *Vcmi*. This, in turn, allows the use of relatively small NMOS transistors in designing the switches that are connected to *Vcmi*. The second stage is a class AB amplifier with active current mirrors. Due to class AB operation of this stage, slew limiting only occurs in the first stage. The second stage currents are chosen so that the non-dominant poles are sufficiently high in frequency to ensure stability. Because of push-pull operation, the lowest non-dominant pole in the class A/AB design is governed by the time constant formed by approximately twice the trans-conductance of the output PMOS transistors, $M_{9,10}$ and the load capacitance. Thus the output branch current can be about half that used in the two-stage class A circuit for the same non-dominant pole frequency. When this fact is exploited together with the use of gain in the second stage current mirrors, a significant reduction in power dissipation can be achieved relative to the two-stage class A topology. The mirror pole and zero will eventually degrade the phase margin of the circuit. For increasing the mirror pole and zero frequencies in the active current mirrors NMOS transistors have been used in this design.

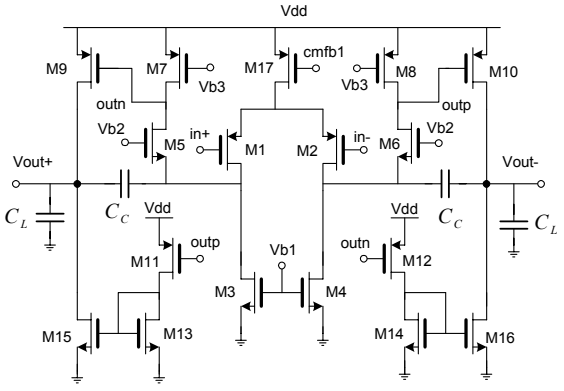

Fig. 1: Proposed OTA Structure.

Common mode feedback (CMFB) is required in fully differential amplifiers to define the voltage at high impedance output nodes [4]. The common mode output voltage of the first stage is not coupled to the common mode output of the second stage. Therefore, two independent feedback circuits are needed to establish the common mode voltages at the outputs of the first and second stages. The first stage CMFB circuit is shown in Fig. 2. *Vcm1* is the quiescent bias voltage for the tail current source. *Vcmo1* is the common mode output voltage of the first stage, which is set by a replica bias current so as to establish the desired quiescent currents in the second stage. The second stage CMFB circuit as shown in Fig. 3, senses the common mode output voltage with a switched capacitor network similar to that used in the first stage CMFB. The output common mode voltage is then used to control two common source amplifiers, Mc1 and Mc2 that drive the output nodes.

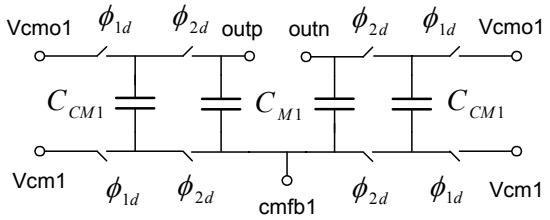

Fig. 2: First stage CMFB circuit.

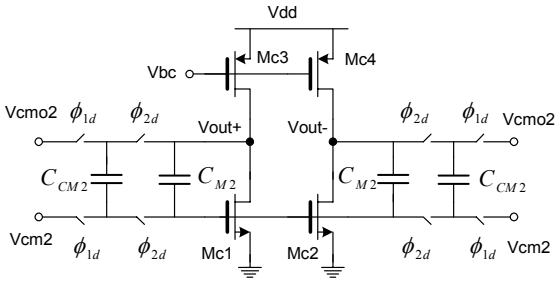

Fig. 3: Second stage CMFB circuit.

Some form of compensation is needed to maintain stability in a two-stage amplifier. The standard miller compensation has a pole splitting effect, which moves one pole to a lower frequency and another to a higher frequency [5]. The two-stage amplifier shown in Fig. 1 employs the cascode compensation scheme, which creates a dominant pole and two complex poles at a higher frequency. This scheme of compensation yields a higher amplifier bandwidth compared to the standard miller compensation at cost of more complex design procedure for the settling behavior of the amplifier. Since the cascode compensation scheme creates an amplifier with four closed loop poles, the design equations become significantly more complicated than those of a single-stage or conventional miller compensated two-stage amplifier. This implies that for practical designs some form of computer optimization constrained by the tradeoffs in the design equations will be necessary.

3. DESIGN PROCEDURE

This section investigates the various noise, speed and power tradeoffs in the design of the proposed OTA.

3.1. Noise

The open loop input referred thermal noise of the OTA can be approximated by

$$\overline{V_n^2} = \frac{16KT\gamma}{3g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right) \qquad (1)$$

where γ is the noise enhancement factor for short channel transistors [6].

In order to reduce the noise, the overdrive voltage of transistors $M_{3,4}$ and $M_{7,8}$ should be increased, where it is possible. Flicker noise can be reduced by using as large as possible input and load transistors or double correlated sampling technique.

3.2. DC Gain

The low frequency gain of the OTA in Fig. 1 is the product of the first and second stage gain.

$$\begin{aligned} A_{dc} &\approx g_{m1}\left\{r_{ds7}\| \left[g_{m5} r_{ds5} (r_{ds1}\| r_{ds3})\right]\right\} \\ &\quad \times (g_{m9}+g_{m15}) \times (r_{ds9}\| r_{ds15}) \qquad (2) \\ &\approx g_{m1} r_{ds7} g_{m9} r_{ds9} \end{aligned}$$

The transistor output resistance, r_{ds} is proportional to the channel length of the device. Since M_7 and M_8 are not in the signal path, they can be made long channel to achieve higher dc gain.

3.3. Linear Settling

The OTA needs to have a sufficient bandwidth for the signal to linearly settle to the desired accuracy within a definite period. The proposed OTA has three zeros and four poles in the closed loop topology as shown in Fig. 4, approximately defined as follows

$$\omega_t \approx \frac{\beta g_{m1}}{C_C} \qquad (3)$$

$$\begin{aligned} |\omega_{p2}| &\approx \frac{g_{m9}+g_{m15}}{C_L+(1-\beta)C_I} \\ \beta &\approx \frac{C_I}{C_I+C_S} \end{aligned} \qquad (4)$$

$$|\omega_{p3}| \approx \frac{g_{m5}}{C_C+C_{gs5}+C_{gd1}+C_{gd3}+C_{db1}} \qquad (5)$$

$$\omega_{p4} \approx \frac{g_{m13}}{C_{gs13}+C_{gs15}+C_{gd11}+C_{db11}+C_{db13}} \qquad (6)$$

$$\omega_{z1} \approx \frac{2g_{m13}}{C_{gs13}+C_{gs15}+C_{gd11}+C_{db11}+C_{db13}} \qquad (7)$$

$$\begin{aligned} \omega_{z2,3} &\approx \pm\sqrt{\frac{g_{m5}\,g_{m9}}{C_1 C_C}} \\ C_1 &\approx C_{gd3}+C_{gd5}+C_{gs9} \end{aligned} \qquad (8)$$

For the amplifier to remain stable, the three non-dominant poles should be made much larger than the unity gain bandwidth, therefore we must have

$$g_{m9},\, g_{m15} \succ\succ \frac{\beta g_{m1}[C_L+(1-\beta)C_I]}{C_C} \qquad (9)$$

$$g_{m5} \succ\succ \beta\, g_{m1} \qquad (10)$$

Increasing the gain in the current mirrors does lower the mirror pole and zero. Therefore a reasonable gain in the current mirror transistors should be used in the high speed applications.

3.4. Slew Rate

The slew limit only occurs in the first stage, so we have

$$SR = \frac{2I_{DS1}}{C_C} \qquad (11)$$

where I_{DS1} is the drain-source current of the input transistors.

4. SIMULATION RESULTS

The proposed OTA has been designed in a 0.25µm digital CMOS technology for a switched integrator as shown in Fig. 4. The bootstrapped switches proposed in [1] have been used in this design. The threshold voltages of this technology for NMOS and PMOS transistors are 0.55V and -0.65V, respectively. Fig. 5 shows the simulated open loop dc gain and phase margin. In Fig. 6 the settling behavior of the proposed OTA has been shown. Table 1 summarizes the simulated performance.

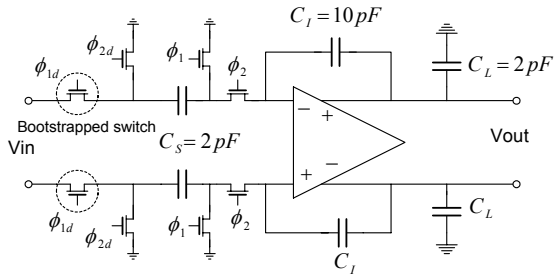

Fig. 4: Fully differential switched capacitor integrator.

5. CONCLUSIONS

In this paper a new merged two-stage class A/AB OTA has been proposed. Because of class AB operation of the second stage, the currents in this stage are determined so that the non-dominant poles and zeros are sufficiently large in frequency to maintain stability, that is the currents are not constrained by the slew rate limiting of the OTA. For moving the mirror pole and zero to high frequency, NMOS transistors have been used in the active current mirrors. It also employs cascode compensation instead of standard miller counterpart to improve the speed.

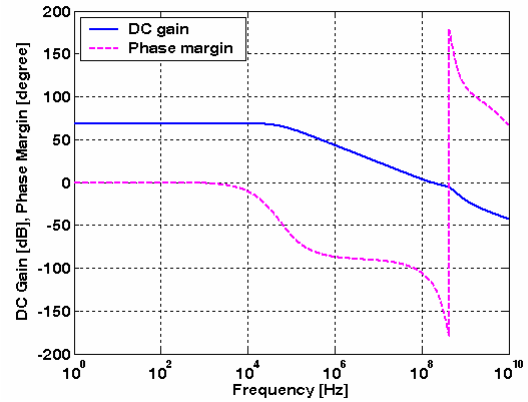

Fig. 5: Simulated open loop dc gain and phase margin.

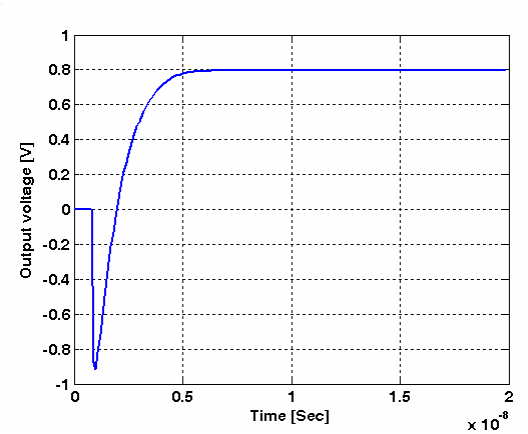

Fig. 6: Settling simulated result.

Table 1: Simulation results.

Parameter	Value
Vdd	1.2 V
DC Gain	68.5 dB
Unity Gain Bandwidth	165 MHz
Phase Margin	65 degree
Compensation Capacitance	3 pF
Load Capacitance	4 pF
Slew Rate	329 V/μs
Settling Time (0.01%)	11 ns
Output Voltage Swing	0.9Vpp
Input Referred Thermal Noise	4.5×10^{-16} V^2/Hz
Power Consumption	5.8 mW

6. ACKNOWLEDGMENT

This work was supported in part by a grant from University of Tehran research budget.

7. REFERENCES

[1] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping," IEEE J. Solid-State Circuits, vol. 36, no. 3, pp. 349-355, March 2001.

[2] Shahriar Rabii and B. Wooley, "A 1.8-V digital-audio sigma-delta modulator in 0.8-μm CMOS," IEEE J. Solid-State Circuits, vol. 32, no. 6, pp. 783-796, June 1997.

[3] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," IEEE J. Solid-State Circuits, vol. 18, Dec. 1983.

[4] D. Johns and K. Martin, *Analog integrated circuit design*, John wiley & sons, 1997.

[5] Behzad Razavi, *Design of analog CMOS integrated circuits*, McGraw-Hill, 2000.

[6] R. Jindal, "Hot-electron effects on channel thermal noise in fine-line NMOS field-effect transistors," IEEE Trans. Electron Devices, vol. ED-33, pp. 1395-1397, Sep. 1986.