A 3.3V High-Resolution Sigma-Delta Modulator for Digital Audio

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Abstract

This paper discusses the architecture and circuit requirements for a CMOS Sigma-Delta modulator that provides digital audio performance. The performance objective is to achieve a dynamic range of 110 dB (18-bit resolution) for a 25 KHz signal bandwidth while operating from a single 3.3V power supply.

Index terms: Sigma-Delta modulation, digital audio, high resolution.

1. Introduction

Sigma-Delta modulation is a robust means of implementing high-resolution analog to digital converters in VLSI technology [1]. By combining oversampling and feedback to shape the noise, and then using a digital low-pass filter to attenuate the noise that has been pushed out-of-band, it is possible to achieve a dynamic range as high as 18-bit. Moreover, oversampling architectures are potentially a power efficient means of implementing high-resolution A/D converters. In effect, an increase in sampling rate can be used to reduce the number and complexity of the analog circuits required in comparison with Nyquist rate architectures, transferring much of the signal processing into the digital domain where power consumption can be dramatically reduced simply by scaling the technology and reducing the supply voltage.

Such ADC's like professional audio are usually classified as high-end and require 18-bit resolution. Several Sigma-Delta ADC's with 18-bit resolution have been previously reported [2], [3], [4], however all operate with 5V power supply to take advantage of the larger signal swing. In this paper a new Sigma-Delta modulator architecture that can achieve 18-bit resolution with a single 3.3V power supply is presented. Also the circuit requirements for the implementation of this proposed architecture is derived.

2. MODULATOR ARCHITECTURE

Sigma-Delta modulator architectures may be classified as either single loop, which use one A/D and D/A converter along with a series of integrators, or multistage (MASH), which consist of a cascade of single loop Sigma-Delta modulators. Both single loop and cascade architectures may employ either single bit or multi bit A/D and D/A converters.

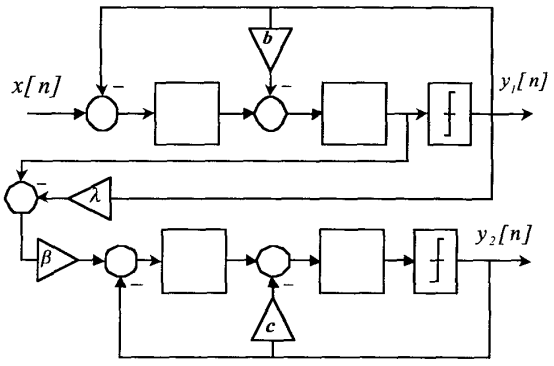
A single loop Sigma-Delta modulator with more than two integrators will suffer from unstable oscillations for large level inputs, therefore they cannot be chosen for higher overload level modulators. An important advantage of using a multi bit quantizer is that the integrator settling requirements are greatly relaxed since the amplitude of the maximum step change in the integrator input is smaller than with a 1-bit quantizer. Therefore, the integrator seldom slew limits, and the time available for linear settling is maximized. This, in turn, implies a savings in power. Finally, the amplitude of spectral tones is greatly diminished because the total quantization noise is lower, and the quantizer is not continuously in an overload condition. The obvious drawback of multi bit quantization modulators is the need for high linearity in the feedback DAC. Unfortunately, much of the power savings of multi bit quantization are lost owing to the complexity of the techniques that must be used to linearize the output of this DAC.

Cascade architectures use combination of inherently stable first and second order Sigma-Delta modulators to achieve higher order noise shaping. Since stability criteria are relaxed as compared to the higher order loops, the cascade modulators approach the dynamic range more than higher order single loop implementations at the cost of a higher sensitivity to the non-idealities of the building blocks [5]. The cascaded modulators that can achieve 18-b resolution with a single 3.3V power supply for digital audio are the 2-2 and 2-1-1 with oversampling ratios of 128 and 2-1 with oversampling ratio of 256.

3. SYSTEM LEVEL CONSIDERATIONS

A. Modulator Architecture

Fig. 1 shows the 2-2, 2-1-1 and 2-1 cascaded Sigma-Delta modulator architectures.



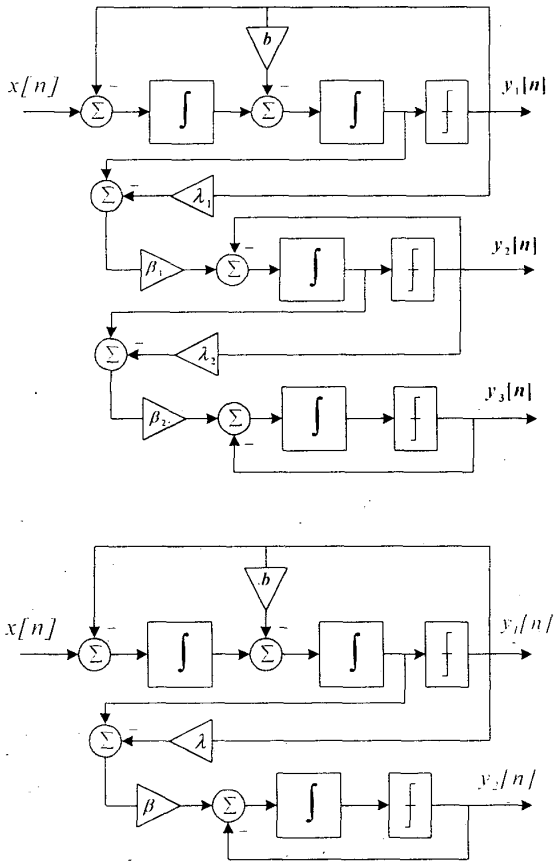


Fig. 1: Block diagram of 2-2, 2-1-1 and 2-1 cascaded Sigma-Delta modulators.

In the design of high-resolution Sigma-Delta modulators the major concern that limits the accuracy is the analog noise (thermal and flicker noise). Analog noise determines power dissipation and analog circuit size. Flicker noise can be reduced by circuit techniques such as double correlated sampling. Thermal noise is generated from the non-zero on resistance of the switches and the thermal noise of the op-amp. For fully differential modulators, the SNR due to KT/C noise of the switches can be written as:

$$SNR_{KT/C} = \frac{(2 \times OL \times V_{ref})^2}{2} \frac{C_s \times OSR}{4KT} \qquad (1)$$

Where C_s, V_{ref}, OSR and OL, are the sampling capacitance, reference voltage, oversampling ratio and overload level factor, respectively. The maximum swing of the integrators (op-amps) determines the reference voltage; therefore for a low power design the overload level factor should be increased where it is possible. For decreasing the thermal noise of operational amplifiers, a low noise op-amp should be used. A two stage OTA that the first stage is a telescopic and second stage is a differential pair has the maximum swing and low input referred noise [6].

The SNR due to input referred thermal noise of this OTA is:

$$SNR = \frac{(2 \times OL \times V_{ref})^2}{2} \frac{3 \times OSR \times C_s}{2KT} \frac{1 + C_s/C_I}{\gamma \times (1 + g_{m2}/g_{m1})} \qquad (2)$$

Where γ is the noise enhancement factor of short channel devices. C_I is the integrating capacitance of the first integrator. C_s is the compensation capacitance of the OTA and g_{m1}, g_{m2} are the trans-conductance of the input and load transistors.

Relations (1) and (2) indicate that the 2-1 cascaded modulator with OSR of 256 has the better performance than the two other cascaded architectures due to these noise problems.

Main drawback of cascaded modulators is the sensitivity to matching error between analog and digital parameters. The matching error increases quantization noise, therefore degrades the SNR. In Fig. 2 the effect of this matching error is shown. This figure indicates that the 2-1 cascaded modulator has the lowest sensitivity than the others. It should be noted for decreasing the power dissipation of the modulator, the sampling capacitances should be scaled in the next integrators. The matching error percent determines the size of sampling capacitance of the third integrator.

Therefore for a low power design, the 2-1 cascaded modulator with OSR of 256 is a best architecture and is considered in this paper.

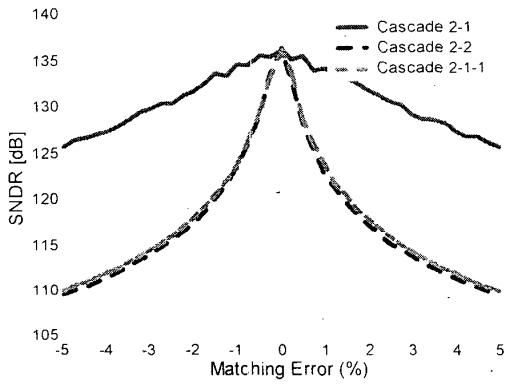


Fig. 2: SNDR versus matching error.

B. Modulator Design

In this section computer simulations that model the non-linearity of the quantizer are used to select the system gains, b, β, λ, shown in Fig. 1 for the 2-1 cascaded modulator. The value of these gains is chosen with the objective of maximizing the dynamic range of the modulator under the assumption that the circuit noise floor is −113.5 dB with considering the sampling capacitance of the first integrator of 10-pF. This amounts to maximizing the modulator overload level without increasing the quantization noise floor above the circuit noise. Another consideration in choosing the system gains is to ensure that the baseband quantization noise is independent of the input signal, thereby avoiding the presence of spurious tones and signal dependence in the noise floor.

Choosing of b=2.5 is a reduction in spectral tones in the output of the first stage, that was noted in [7]. Fig. 3 shows the effect of different values of β and λ on the overload level. The highest overload level is the –0.55 dB (i.e. the maximum input amplitude in which the SNR degrades no more than 6 dB from the maximum SNR [5]) for β=0.125 and λ=2. Unfortunately this combination of gains increases the-quantization noise. The next highest overload level of –1 dB is achieved when β=0.25 and λ=2, however Fig. 4 shows that in the case of β=0.25 and λ=1 quantization noise is more independent of input signal power than the case of β=0.25 and λ=2, therefore the system gains of b=2.5, β=0.25 and λ=1 is considered in this paper. This selection gives overload level of –1.15 dB.

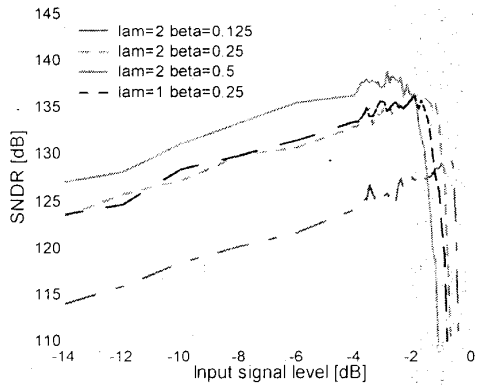


Fig. 3: Dynamic range for different values of β and λ.

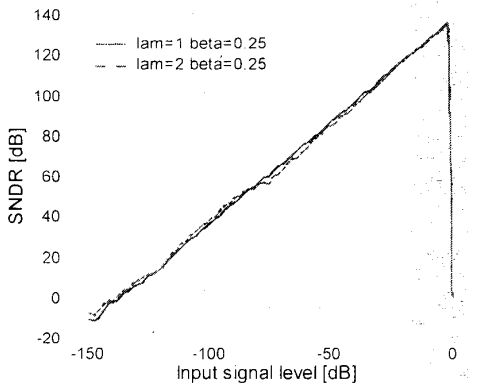


Fig. 4: SNDR vs. input power showing signal dependence in noise floor.

An important consideration in the design of a sigma-delta modulator is the size of the integrators output swing as the modulator input approaches full scale. Fig. 5 shows the integrator gains that are scaled. The objective of signal scaling is to allow a large modulator input signal range to maximize the SNR due to KT/C noise. Table 1 shows the scaled integrator gains derived in this work. It should be noted in [8] a 2-1 cascaded modulator with overload level of –1.3 dBFS has been designed earlier.

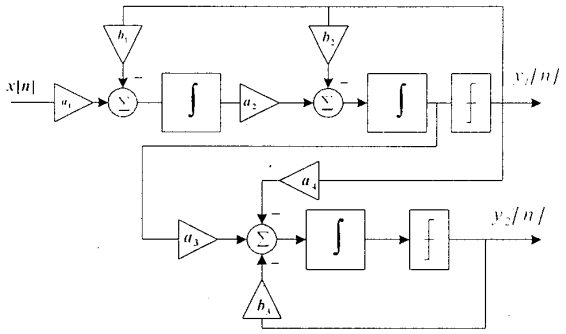


Fig. 5: A 2-1 cascaded sigma-delta modulator with integrator gains.

Table 1: Integrator gains.

Integrator Gain	Value
a_1	0.2
b_1	0.2
a_2	0.5
b_2	0.25
a_3	0.25
b_3	0.1
a_4	0.05

C. Circuit Requirements

The main circuit non-idealities that degrade the SNDR of the modulator include: switches thermal noise, op-amp noise, finite DC gain of the integrators, finite bandwidth and slew rate of the op-amps. With modeling each of the non-idealities, the proposed 2-1 cascaded modulator has been simulated at behavioral level simulation [9]. Table 2 shows the effect of these non-idealities on the SNDR individually. Figs. 6 and 7 show the power spectral density and dynamic range of the proposed modulator including all of the non-idealities that has shown in table 2. The resultant SNDR and DR are the 112 and 114 dB, respectively, that is suitable for achieving the 18-bit resolution.

Table 2: Circuit level requirements.

Integrator Non-ideality	SNDR [dB]
Ideal modulator	136
Switches thermal noise Sampling capacitance (C_s=10pF)	113.6
Input referred op-amp noise V_n=20μV_{rms}	118
Finite DC gain of first integrator A_0=80 dB	131.4
Finite unity gain bandwidth GBW=85 MHz	128
Slew rate (SR=150 V/μs)	126

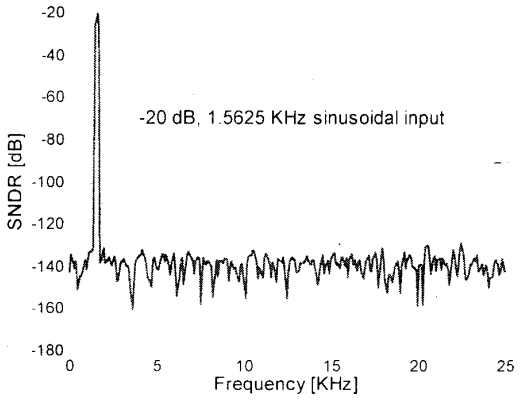


Fig. 6: Power Spectral Density.

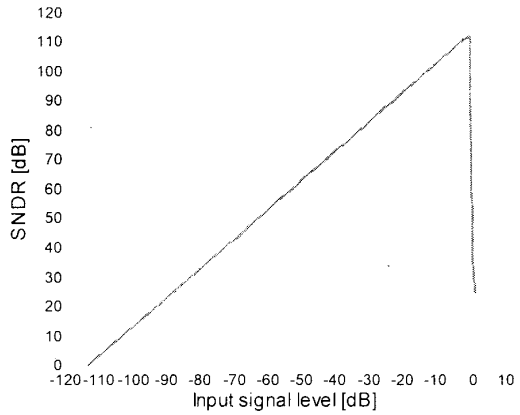


Fig. 7: Dynamic Range.

4. CONCLUSION

In this paper a 2-1 cascaded sigma-delta modulator with OSR of 256 for digital audio has been proposed that achieves 114 dB dynamic range with a single 3.3V power supply. The proposed modulator has the highest overload level of −1.15 dB that is needed in high-resolution noise limited performance sigma-delta modulators. This modulator has the lowest sensitivity to matching error between analog and digital parameters than the other cascaded sigma-delta modulators. Also the circuit requirements for implementing this modulator have been derived.

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