A 1.2-V, 1.6-mW, 107-dB Dynamic Range, and 99.5-dB SNDR Sigma-Delta Modulator for Digital Audio in 0.25-μm CMOS

Mohammad Yavari

IC Design Lab, ECE Department, University of Tehran, Tehran 14395-515, Iran
E-mail: yavari@ece.ut.ac.ir
Homepage: http://eng.ut.ac.ir/iclab/members/yavari/yavari.htm

Abstract

This paper presents a 1.2-V, 1.6-mW, and high-resolution sigma-delta modulator for digital audio. It uses a modified low-swing integrator outputs 4th order single-loop topology. Modulator coefficients are optimized for higher overload level factor and low power. A low-power two-stage class A/AB OTA with modified common mode feedback (CMFB) circuit in the first stage is used in the first integrator. To reduce the power consumption, a simple folded-cascode OTA is used in the last three integrators. Simulation results with OSR of 100 give SNDR and dynamic range (DR) of 99.5 dB and 107 dB including the circuit noise in the 25 kHz signal bandwidth, respectively. The circuit is implemented in a 0.25-μm standard CMOS technology.

Index terms: Sigma-Delta Modulation, Operational Amplifiers, Switched-Capacitor Circuits.

1. Introduction

High-order sigma-delta modulators are the most suitable techniques for A/D converters for low-speed and high-resolution applications due to reduced antialiasing filter and analog implementation requirements. Also by trading accuracy with speed, sigma-delta modulators allow high performance to be achieved without any tolerance analog components.

The trends toward lower operating supply voltages and low-power consumption in mixed-signal IC's has three strong motivations: 1) portable equipment capable of operating with minimum number of battery cells to reduce volume and weight, 2) voltage limitations resulted from smaller feature sizes of modern IC technologies, and 3) longer operating periods without battery recharging or replacement.

Such applications like digital audio are usually classified as high-end and require high-resolution analog-to-digital converters (ADC's) [1][2][3][4][5]. Design of high-resolution and low-voltage sigma-delta modulators is a new challenge for analog designers. In this paper a very low-voltage, low-power and high-resolution sigma-delta modulator is designed. It uses a new modified 4th order single loop topology and low-power two-stage class A/AB OTA in the first integrator with inherent CMFB circuit in the first stage. The circuit requirements for the implementation of this modulator are designed in a 0.25μm standard CMOS technology and simulated in all process corners including the temperature and power supply variations.

In section (2) the proposed modulator architecture is described. Section (3) describes the design of building blocks of the modulator. Simulation results are reported in section (4). Section (5) concludes the paper.

2. Modulator Architecture

Sigma-delta modulator architectures may be classified as either single loop, which use one A/D and D/A converter along with a series of integrators, or multistage (MASH), which consist of a cascade of single loop modulators. Both single loop and cascade architectures may employ either single bit or multi bit A/D and D/A converters.

Cascade architectures need a high dc gain op-amp in the implementation of the integrators to prevent the quantization noise leakage of the first stage ADC's. Achieving a high dc gain op-amp in the very low-voltage applications is very difficult. For example a dc gain of at least 80 dB is needed for design of a cascaded modulator in [5]. Thus cascaded architectures are not a suitable candidate in the very low-voltage applications.

The obvious drawback of multi bit quantizer modulators is the need for high linearity in the feedback digital-to-analog converter (DAC). Some DAC linearization techniques have recently been proposed such as dynamic element matching and DAC error shaping. But these techniques introduce spectral tones in the baseband, which greatly reduces signal to quantization plus distortion ratio (SNDR) especially for large level input signals. Also these techniques greatly increase the complexity of the design. They are suitable for high-speed applications, where the oversampling ratio cannot be chosen large.

Single loop sigma-delta modulators need lower DC gain OTA and other circuit requirements compared to cascaded counterparts. However a single loop ΣΔ modulator with more than two integrators will suffer from unstable oscillations for large level inputs. In other words they have low overload level factor. It should be noted that in the design of high-resolution ΣΔ modulators, the major concern that limits the accuracy is the analog noise. To achieve a higher SNR due to KT/C noise of the switches, the overload level factor should be increased where it is possible. Some techniques have been proposed to improve the overload level of single loop modulators. In [6][7] the local feedback (LFB) technique has been applied for overload prevention. An LFB consists of a tri-level quantizer and a tri-level DAC, which is connected across a single integrator. The LFB continuously monitors the integrator output, and controls the integrator output swing by feeding back a quantized error signal to the its summing node. The quantizer has three levels, so it feeds back error signals ± 1 only for large level inputs when overload occurs, otherwise remains idle by feeding back zero. The quantization noise of the LFB can be cancelled by a logic similar to the noise cancellation logic (NCL) of cascaded ΣΔ modulators. The drawback of using this technique in a high-order single loop modulator is the necessity of an LFB around the first integrator (integrator closest to the input) to avoid instability. In this case mismatch between the LFB and the corresponding digital coefficient in NCL causes direct quantization noise leakage to the output without any suppression by noise shaping. Thus, for a large level input when the LFB is active, rapid SNDR degradation near full-scale still occurs. Overload is only replaced by severe quantization noise leakage.

Another technique to improve the overload level is to design a modulator with reduced gain in the passband of the noise transfer function. However, reducing this gain degrades the SNDR. Thus, a tradeoff between overload, stability, SNDR, and modulator order should be considered. The SNDR can be improved by distributing the zeros of noise transfer function around the signal bandwidth. In this work, this technique is used to improve the overload level factor.

In this paper a modified 4^{th} order single loop ΣΔ modulator similar to [4] is designed. Fig. 1 shows the proposed modulator architecture. It has a combined topology of both feedback and feed-forward paths. Thus the modulator combines the advantage of distributed feedback (DFB) and distributed feed-forward (DFF) modulators. DFB modulators have higher input level factor than DFF. But they need small integrator coefficients to prevent overloading, which maximizes the power consumption due to increased integrating capacitances. It should be noted that the sampling capacitance of the first integrator is determined by KT/C noise of the switches. By using the feed-forward paths in this topology the integrator coefficients can be large, which reduces the power dissipation.

The modulator topology in [4] has large swing at the third integrator output. This is due to the weak feedback factor α, which causes a large input to this integrator. The large swing of the third integrator output also reduces the overload level factor and need a large swing OTA for implementation. In this paper a new path has been added to the modulator architecture to reduce the output swing of this integrator (β feedback in Fig. 1). This enhances the amount of negative feedback, and hence reduces the input of the third integrator. With this modification one can achieve both low-swing integrator outputs and high overload level factor. Fig. 2 shows the histogram of the integrator outputs for the modulator of Fig. 1 when the feedback reference levels are normalized to ±1 with and without adding negative β feedback. The input signal is a 2.44140625 kHz, -1.8 dBFS sinusoidal.

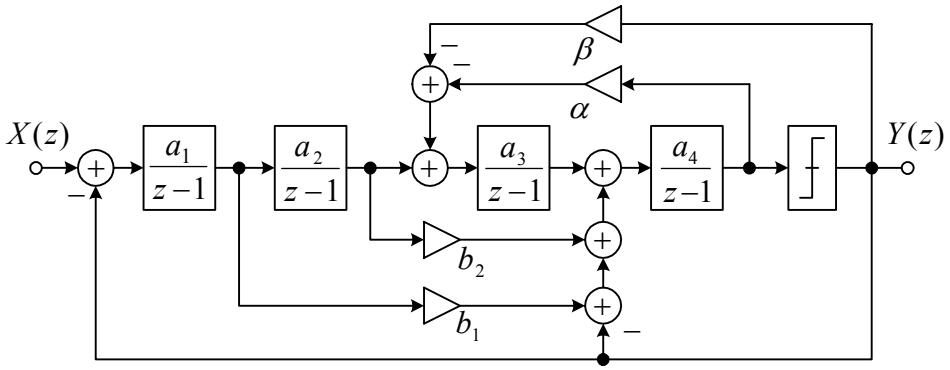

Figure 1. Proposed 4th order single loop modulator architecture.

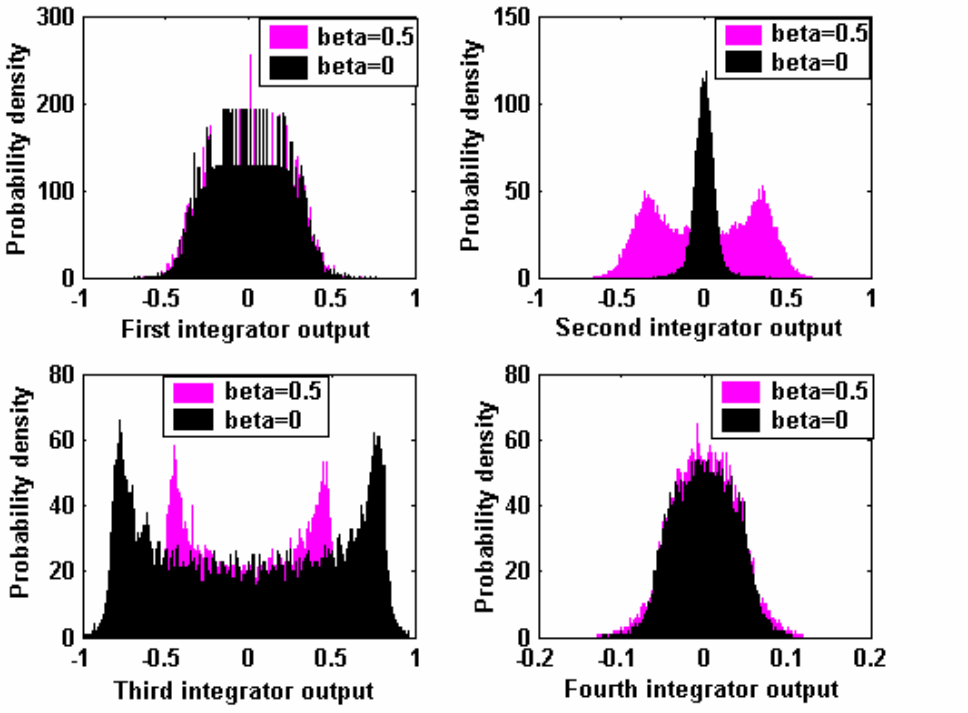

Figure 2. Histogram of the integrator outputs.

The loop coefficients a_i's, b_i's, α and β determine the pole locations of the noise transfer function whereas α, a_3 and a_4 determine the position of the complex zero pair. The remaining zeros are at DC. The feedback around the last two integrators forms a resonator. By the proper choice of the feedback factor, α, the complex zeros can be situated to give optimum noise suppression in the baseband. All of the integrators have a unit delay for fast settling. The designed coefficients of the modulator are:

$$a_1 = 1/3, \quad a_2 = 3/25, \quad a_3 = 1/10, \quad a_4 = 1/25, \quad b_1 = 1, \quad b_2 = 0.8, \quad \alpha = 1/5, \quad \beta = 0.5$$

3. Modulator Design

The main circuit non-idealities that degrade the SNDR of a modulator include: switches thermal noise, opamp noise, finite DC gain of the integrators, finite unity gain bandwidth, and slew rate of the opamps. With modeling each of the non-idealities as reported in [8], the proposed 4th order single loop modulator was simulated at behavioral level. Table 1 shows the effect of these non-idealities on the SNDR individually. The resultant SNDR is 101.5 dB including all of the non-idealities shown in Table 1. In these simulations, input signal is a 2.44140625 kHz, -2 dBFS sinusoidal.

Table 1. Circuit level requirements.

Integrator Non-idealities	SNDR [dB]
Ideal modulator	112
Switches thermal noise (C_s = 5 pF)	102.5
Input referred op-amp noise (V_n = 10 μVrms)	109
Finite DC gain of first integrator (A_{dc} = 60 dB)	110
Finite unity gain bandwidth (UGBW = 30 MHz)	110.5
Slew Rate (SR = 25 V/μs)	111
Including all of non-idealities	101.5

The modulator is simulated using switched-capacitor techniques. The circuit is fully differential in order to suppress undesired common mode signals such as substrate and power supply noises and clock feed-through. To achieve the desired SNDR, sampling and compensation capacitors of 5-pF and 8-pF are chosen for the first integrator, respectively, due to KT/C and OTA thermal noises.

3.1 Operational Transconductance Amplifier

A fully differential two-stage class A/AB OTA similar to [2] as shown in Fig. 3 is used to implement the first integrator. This OTA combines a simple differential pair as the first stage with active current mirrors as the second stage. PMOS input differential pair allows the use of near ground as the op-amp common mode input, V_{cmi}. This, in turn, allows the use of relatively small NMOS transistors to design the switches that are connected to V_{cmi}. Another advantage of using PMOS input differential pair is its low input referred noise compared to a folded cascode as the first stage.

The second stage is a class AB amplifier with active current mirrors. Due to class AB operation of this stage, slew limiting only occurs in the first stage. The second stage currents are chosen so that the non-dominant poles are sufficiently high in frequency to ensure stability. Because of push-pull operation, the lowest non-dominant pole in the class A/AB design is governed by the time constant formed by approximately twice the transconductance of the output NMOS transistors, $M_{5,6}$ and the load capacitance.

Thus the output branch current can be about half that used in the two-stage class A circuit for the same non-dominant pole frequency. When this fact is exploited together with the use of gain in the second stage current mirrors, a significant reduction in power dissipation can be achieved relative to the two-stage class A topology. The mirror pole and zero will eventually degrade the phase margin of the circuit. To increase the mirror pole and zero frequencies in the active current mirrors a low current gain is used in this design. It also uses standard miller compensation. The simulated opamp unity gain bandwidth is 41 MHz with a phase margin of 81° and the DC gain of 70 dB.

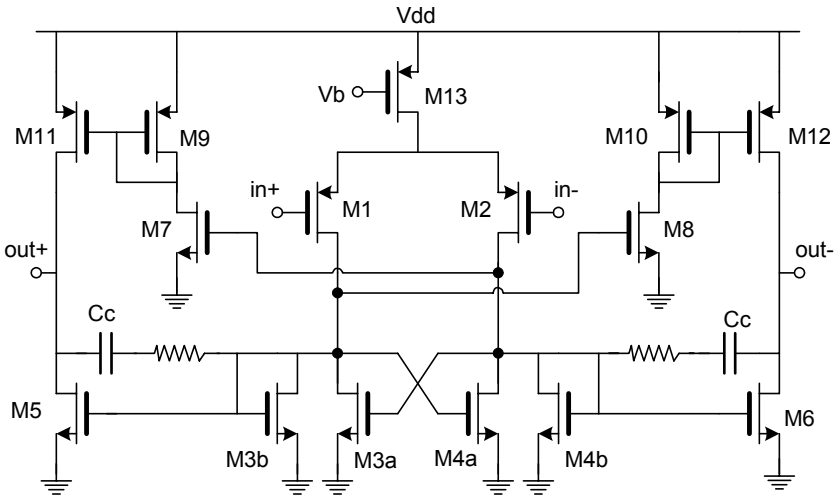

Figure 3. A two-stage class A/AB OTA.

Common-mode feedback (CMFB) circuit is required in fully differential amplifiers to define the voltages at the high-impedance output nodes. The CMFB circuit of the first stage is replaced by the cross-coupled connection of transistors M_{3a}, M_{3b}, M_{4a} and M_{4b} similar to [3][9]. The conductance g_{m3b} seen at the gate of transistors M_{3b} and M_{4b} is cancelled by the opposite action of the parallel transistors M_{3a} and M_{4a}, respectively. This negative feedback connection causes the differential signal at the output of the first stage to see a high load impedance. On the other hand for the common mode signal, the output conductance is limited by $g_{m3a} + g_{m3b}$. This is a low impedance and thus the first stage does not require an additional CMFB circuit.

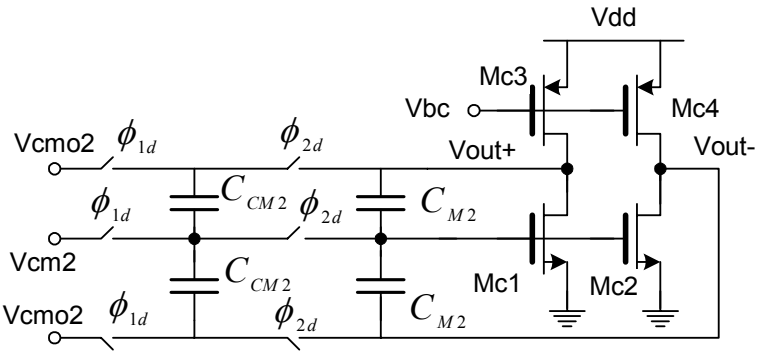

Figure 4. Second stage common mode feedback.

For the second stage a simple CMFB circuit as shown in Fig. 4 is used. It senses the common mode output voltage with a switched capacitor network. The output common mode voltage is then used to control two common source amplifiers M_{C1} and M_{C2} that drive the output nodes.

Due to low-swing integrator outputs a simple folded-cascode OTA is used in the implementation of the last three integrators.

3.2 Comparator

The main problem of a low-voltage comparator is to do the reset. A sigma-delta modulator does not need a comparator with high resolution, but requires low hystersis, so a good reset is important. Fig. 5 shows a simple low-voltage comparator that is used in this work [10].

It consists of a differential pair with input DC level at 0.2V feeding into an NMOS regenerative latch transistors. The outputs are reset to Vss. A simple switched capacitor circuit is needed to shift the common mode level of last integrator output which is around half of power supply voltage to common mode input of the comparator which is 0.2V in this work. The outputs of the comparator are inverted and stored in an SR latch that is implemented with CMOS NAND gates. Inverters buffer the output of the SR latch that drive NMOS switches connected to the negative reference voltage and PMOS switches connected to the positive reference voltage of digital to analog converters. The simulated modulator employs feedback reference voltages equal to the supply voltages due to achieving the highest dynamic range.

3.3 Switches

The gate-source bootstrapping technique is used to allow low-voltage operation of simple NMOS switches. Fig. 6 shows the transistor implementation of the bootstrap circuit [3]. Capacitor Coff is charged to Vdd during ϕ_2 through transistors MN3 and MP4 while the main switch MNSW is cutoff through transistors MN5 and MNT5. During ϕ_1, Coff is placed around the gate-source terminals of MNSW through transistors MN1 and MP2. Transistor MN6S triggers MP2 ON at the beginning of ϕ_1 while transistor MN6 keeps it ON as the voltage on node A rises to the source voltage. Transistor MNT5 has been added to prevent the gate-drain voltage of MN5 from exceeding Vdd during ϕ_1 while it is OFF. This circuit allows switch operation (transistor MNSW) from rail to rail while limiting all gate-source voltages to Vdd avoiding any oxide overstress. It also guarantees maximum switch conductance independently of the switched potential and enhances considerably the switch linearity. In order to prevent the drain-gate voltage of transistor MNSW exceeding Vdd at the switching moment, an additional transistor MN8 has been added on the drain side of MNSW, such that the switch MNSW becomes completely symmetrical. The gate voltage is thus clamped at a voltage Vdd higher than the terminal of the lowest voltage.

The integrators need a 2-phase non-overlapping clock (with delays) to minimize signal dependent charge injection errors. Since the settling time of the integrator circuits is shorter during the sampling phase than the charge transfer phase, clocking with 50% duty cycle does not take full advantage of the circuit speed during the sampling phase. So a duty cycle of 30% for sampling (phase 1) and 60% for charge transfer (phase 2) is used. The remaining 10% of clock period is used to separate the different clock edges so as to overlap the phases.

4. Simulation Results

The proposed 4^{th} order single loop ΣΔ modulator in this paper was simulated in a 0.25-μm standard CMOS technology. The threshold voltages of this process are 0.55-V and –0.65-V for NMOS and PMOS transistors, respectively. The modulator samples at 5 MHz with 25 kHz signal bandwidth and oversampling ratio of 100. All of the simulations were performed with HSPICE including 20% bottom plate parasitic capacitances and –40°C to 85°C temperature variations in all process corners. Plots of SNDR and DR are shown in Fig. 7. The resultant SNDR and DR are 99.5 dB and 107 dB, respectively. Table 2 summaries the performance of the simulated modulator.

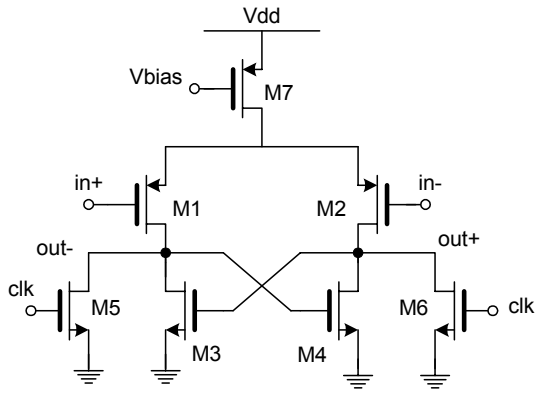

Figure 5. A simple dynamic latch comparator.

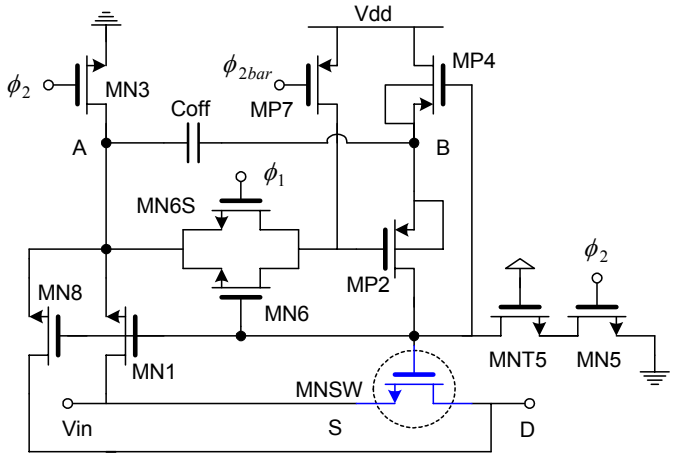

Figure 6. Clock bootstrapping circuit.

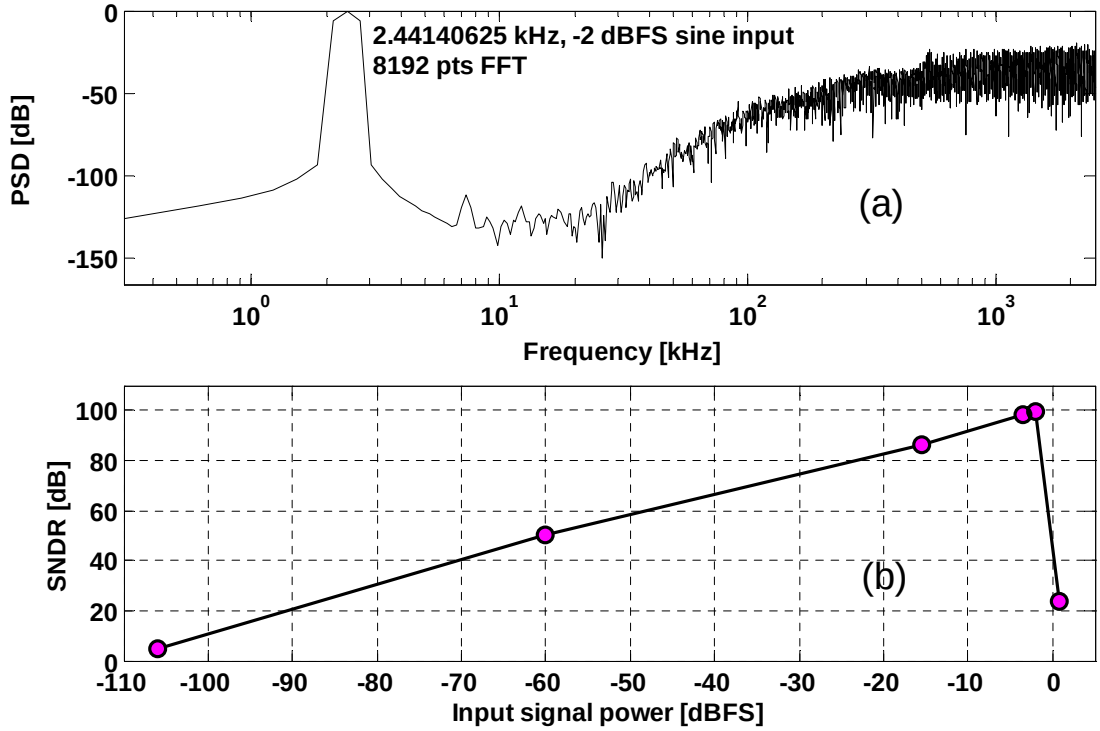

Figure 7. (a) Power spectral density, (b) Dynamic range.

5. Conclusions

In this paper a modified 4th order single loop sigma-delta modulator has been designed for very low-voltage audio applications. The modulator has low integrator output swings and large first integrator coefficients, which reduce the power consumption. A two-stage class A/AB OTA has been used to implement the first integrator. Class AB operation of second stage of a two-stage OTA causes the slew limiting only to occur in the first stage, which reduces the power consumption of OTA in the switched capacitor applications due to large load capacitance. A simple folded-cacode OTA has been used in the

last three integrators. This modulator has been simulated in a 0.25-μm standard CMOS technology. The simulated SNDR and DR are 99.5 dB and 107 dB, respectively.

Table 2. Modulator performance summary.

Power supply voltage	1.2 V
Power dissipation First OTA 2^{nd}, 3^{rd}, and 4^{th} stage OTA's Other parts	1.6 mW 1.1 mW 0.41 mW 0.09 mW
Oversampling ratio	100
Signal bandwidth	25 kHz
Clock frequency	5 MHz
SNDR @ -2 dBFS input	99.5 dB
DR and Overload level (OL)	107 dB, -1.8 dBFS
Process	0.25-μm standard CMOS

6. References

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