A High-Resolution & Low-Voltage Sigma-Delta Modulator in 0.6μm CMOS for Digital Audio

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ABSTRACT

This paper presents a 3.3-V, 18 bit Sigma-Delta modulator for digital audio, which has been simulated in a 0.6 μm double poly, triple metal CMOS process using poly-poly capacitors in all process corners and considering ±10% power supply and -40°C to 85°C temperature ranges. The integral gain coefficients of a 2-2 cascaded modulator have been developed for achieving higher overload level factor that is needed for high-resolution noise limited performance modulators. Simulation results give *SNDR* of 111 dB and 110 dB in typical and worst case, respectively with considering of the circuit noise.

Index terms: Sigma-Delta modulation, *KT/C* noise, Cascode compensation, Operational amplifier.

1. INTRODUCTION

Sigma-Delta modulation is a robust means of implementing high-resolution analog to digital converters in VLSI technology [1]. By combining oversampling and feedback to shape the noise, and then using a digital low-pass filter to attenuate the noise that has been pushed out-of-band, it is possible to achieve a dynamic range as high as 18-bit. Moreover, oversampling architectures are potentially a power efficient means of implementing high-resolution A/D converters. In effect, an increase in sampling rate can be used to reduce the number and complexity of the analog circuits required in comparison with Nyquist rate architectures, transferring much of the signal processing into the digital domain where power consumption can be dramatically reduced simply by scaling the technology and reducing the supply voltage.

Such ADC's like professional audio are usually classified as high-end and require 18-bit resolution. Several Sigma-Delta ADC's with 18-bit resolution have been previously reported [2], [3], [4], however all operate with 5-V power supply to take advantage of the larger signal swing. In this paper a new Sigma-Delta modulator architecture that can achieve 18-bit resolution with a single 3.3-V power supply is presented. The circuit requirements for the implementation of proposed architecture has been designed in a 0.6 μm 5-V double poly triple metal (DPTM) digital CMOS process.

2. MODULATOR ARCHITECTURE

Sigma-Delta modulator architectures may be classified as either single loop, which use one A/D and D/A converter along with a series of integrators, or multistage (MASH), which consist of a cascade of single loop Sigma-

Delta modulators. Both single loop and cascade architectures may employ either single bit or multi bit A/D and D/A converters.

A single loop Sigma-Delta modulator with more than two integrators will suffer from unstable oscillations for large level inputs, therefore they can not be chosen for higher overload level modulators. An important advantage of using a multi bit quantizer is that the integrator settling requirements are greatly relaxed since the amplitude of the maximum step change in the integrator input is smaller than with a 1-bit quantizer. Therefore, the integrator seldom slew limits, and the time available for linear settling is maximized. This, in turn, implies a savings in power. Finally, the amplitude of spectral tones is greatly diminished because the total quantization noise is lower, and the quantizer is not continuously in an overload condition. The obvious drawback of multi bit quantization modulators is the need for high linearity in the feedback DAC. Unfortunately, much of the power savings of multi bit quantization are lost owing to the complexity of the techniques that must be used to linearize the output of this DAC.

Cascade architectures use combination of inherently stable first and second order Sigma-Delta modulators to achieve higher order noise shaping. Since stability criteria are relaxed as compared to the higher order loops, the cascade modulators approach the dynamic range more than higher order single loop implementations at the cost of a higher sensitivity to the non-idealities of the building blocks [5].

In the design of high-resolution Sigma-Delta modulators the major concern that limits the accuracy is the analog noise (thermal and flicker noise). Analog noise determines power dissipation and analog circuit size. Flicker noise can be reduced by circuit techniques such as double correlated sampling. Thermal noise is generated from the non-zero on resistance of the switches and the thermal noise of the op-amp. For fully differential modulators, the *SNR* due to *KT/C* noise of the switches can be written as:

$$SNR_{KT/C} = \frac{(2 \times OL \times V_{ref})^2}{2} \frac{C_s \times OSR}{4\,KT} \qquad (1)$$

where C_s, V_{ref}, *OSR* and *OL*, are the sampling capacitance, reference voltage, oversampling ratio and overload level factor, respectively. The maximum swing of the integrators (op-amps) determines the reference voltage; therefore for a low power design the overload level factor should be increased where it is possible.

In this paper a 2-2 cascaded Sigma-Delta modulator with *OSR* of 128 has been designed. Fig. 1 shows the 2-2 cascaded Sigma-Delta modulator architecture.

In this section computer simulations that model the non-linearity of the quantizer are used to select the system gains, *b*, *c*, β and λ as shown in Fig. 1 for the 2-2 cascaded modulator. The value of these gains is chosen with the objective of maximizing the dynamic range of the modulator under the assumption that the circuit noise floor is –114 dB with considering the sampling capacitance of the first integrator of 10-pF and V_{ref} of 1.35 V. This amounts to maximizing the modulator overload level without increasing the quantization noise floor above the circuit noise. Another consideration in choosing the system gains is to ensure that the base band quantization noise is independent of the input signal, thereby avoiding the presence of spurious tones and signal dependence in the noise floor.

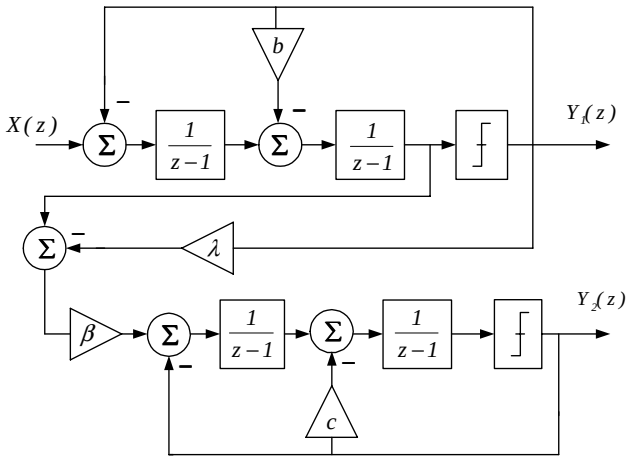

Fig. 1: Block diagram of 2-2 cascaded Sigma-Delta modulator.

Choosing *b* and *c* of 2.5 is a reduction in spectral tones in the output of a second-order modulator, that was noted in [6]. Fig. 2 shows the effect of different values of β and λ on the overload level. The highest overload level is the –0.6 dBFS (i.e. the maximum relative input amplitude in which the *SNR* degrades no more than 6 dB from the maximum *SNR* [5]) for β=0.125 and λ=2. It should be noted in [2] and [3] a 2-2 cascaded modulator with local feedback has been designed for higher overload level, however in this case *SNDR* is very sensitive to matching of analog and digital parameters.

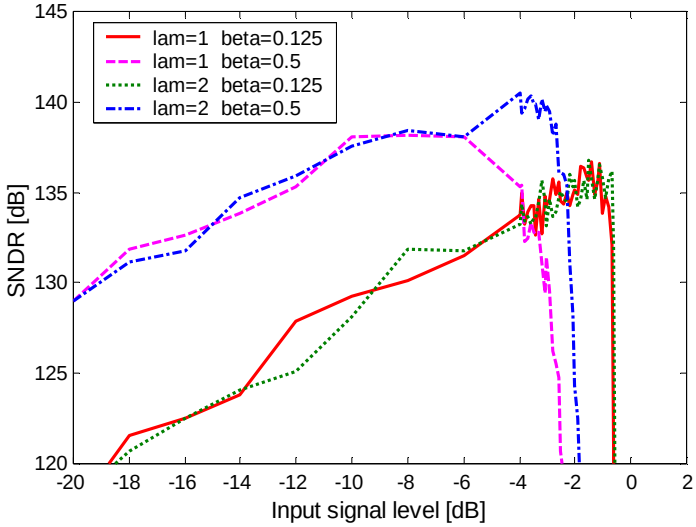

Fig. 2: Dynamic range for different values of β and λ.

An important consideration in the design of a Sigma-Delta modulator is the size of the integrators output swing as the modulator input approaches full scale. Fig. 3 shows the integrator gains, which has been scaled. The objective of signal scaling is to allow a large modulator input signal range to maximize the *SNR* due to *KT/C* noise. The complete design procedure of this modulator has been written in [7].

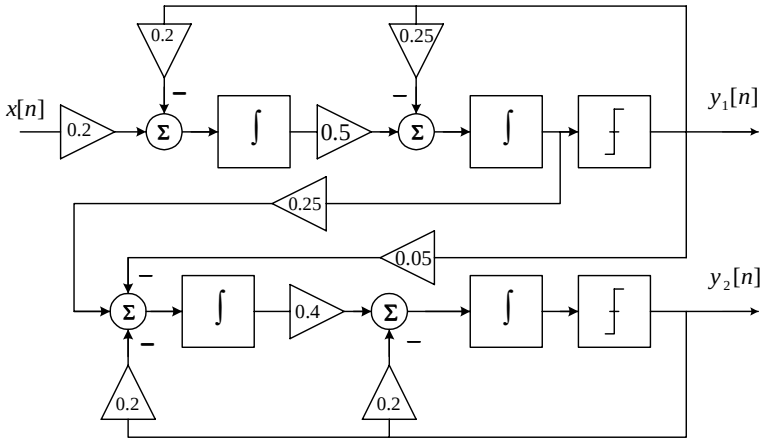

Fig. 3: A 2-2 cascaded Sigma-Delta modulator with integrator gains.

3. MODULATOR DESIGN

The main circuit non-idealities that degrade the *SNDR* of the modulator include: switches thermal noise, op-amp noise, finite DC gain of the integrators, finite bandwidth and slew rate of the op-amps. With modeling each of

the non-idealities, the proposed 2-2 cascaded modulator has been simulated at behavioral level simulation [8]. Table 1 shows the effect of these non-idealities on the *SNDR* individually. The resultant *SNDR* is 112 dB including all of the non-idealities shown in Table 1.

Table 1: Circuit level requirements.

Integrator Non-ideality	SNDR [dB]
Ideal modulator	136
Switches thermal noise, Sampling capacitance (C_s=10pF)	114
Input referred op-amp noise, V_n=3μV_{rms}	118
Finite DC gain of first integrator, A_0=80 dB	124
Finite unity gain bandwidth, UGBW=65 MHz	128
Slew rate (SR=120 V/μs)	126

Switched-capacitor integrators are the key circuit building block in a Sigma-Delta modulator. The design goal is to choose a low-power operational amplifier topology that can meet the requirements of the 2-2 cascade modulator and to optimize device sizes and bias points to minimize power dissipation. For negligible quantization noise leak due to finite amplifier DC gain, the first two amplifiers require gain of 80 dB or greater. Since this gain is on the order of $(g_m r_o)^3$, a two stage amplifier must be employed. From a power dissipation perspective, the following amplifier characteristics are needed: 1) maximum output swing, which suggests a common source second stage, 2) all NMOS signal path for fast settling with large capacitors, 3) minimum number of current legs, 4) minimum number of devices that contribute significant thermal noise, 5) a maximum bandwidth compensation loop and 6) fully-differential 2nd-stage for better common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). The amplifier in Fig. 4 achieves the desirable low-power characteristics. The first stage is a telescopic amplifier, and this is followed by differential pair in the second stage. The telescopic topology has a number of advantages over its folded-cascode counterpart. It has fewer noise-contributing devices, fewer current legs and a wider bandwidth for a given current level.

The amplifier has an all NMOS signal path. NMOS devices are approximately three times faster than PMOS devices because of the difference between the electron and hole mobilities. Since speed and power directly trade off, a higher speed amplifier will dissipate less power for a fixed settling constraint. The disadvantage with NMOS input devices is the higher flicker noise. In this design, large size input devices has been used for having a reasonable flicker noise. The second stage is made fully differential instead of a quasi-differential common-source stage for a number of reasons. Having a tail current device eliminates the need for a power-hungry inversion stage for the common-mode feedback amplifier. This allows the use of dynamic switched-capacitor common-mode feedback circuits, which does not dissipate any static power. The fully differential second-stage amplifier also eliminates the need for a dynamic level shift between the output of the first stage and the input of the second stage [9]. In addition this fully differential topology improves the PSRR and CMRR.

Some form of compensation is needed to maintain stability in a 2-stage amplifier. The standard Miller compensation has a pole-splitting effect, which moves one pole to a lower frequency and another to a higher frequency. The 2-stage amplifier in Fig. 4 employs the cascode compensation scheme [10], which creates a dominant pole and two complex poles at a higher frequency. It has been shown the cascode compensation scheme yields a higher amplifier bandwidth compared to the conventional Miller compensation. The simulated op-amp unity gain bandwidth is 100 MHz with a phase margin of 74° and the DC gain is 95 dB.

Common-mode feedback (CMFB) is required in fully differential amplifiers to define the voltages at the high-impedance output nodes. The amplifier employs dynamic or switched capacitor common-mode feedback. The fully differential second stage eliminates the need for an inversion in the common-mode feedback loop. Fig. 5 shows the common-mode feedback loop for the second stage of the amplifier. Capacitors C_M are used to sense the output

common-mode voltage. During ϕ_{2d}, switched capacitors C_{CM} define the appropriate DC voltage on the sense capacitors. For having sufficient gain in the common-mode feedback circuit a diff pair has been added in Fig. 5. References V_{ref2} and V_{refb2}, which are at the same nominal voltage, are separated to maintain a stable bias on the gate of M_{C1} while the capacitors C_{CM} are switched onto V_{refb2}. Minimum size devices are used for the CMOS switches in the common-mode feedback circuit. Simulation results show that the CMFB loop has a phase margin of 72°. A similar common-mode feedback is designed for the first stage of the amplifier. The nominal output common-mode voltage, V_{CMO}, is 1.7-V for this design.

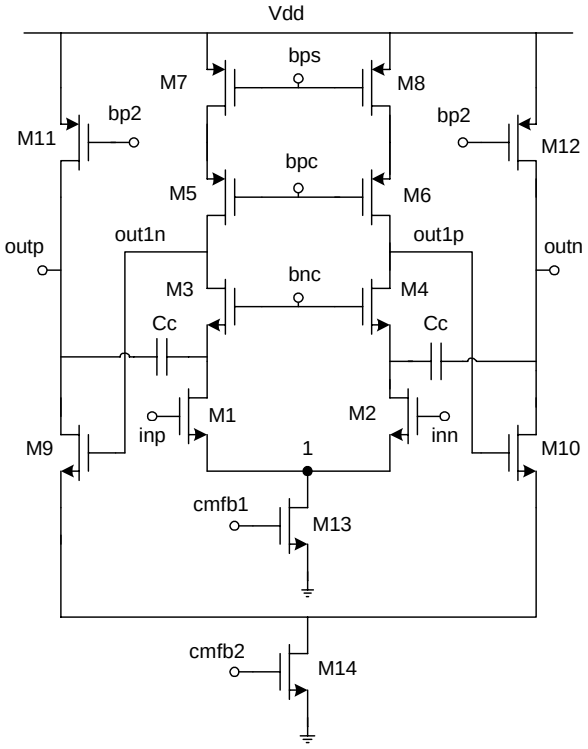

Fig. 4: Fully differential 2-stage OTA.

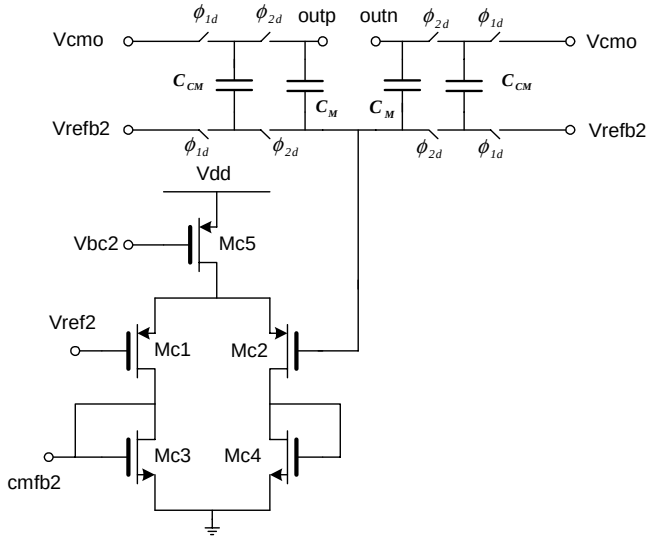

Fig. 5: Common-mode feedback.

The second major component of the modulator is the comparator. The performance of the modulator is relatively insensitive to comparator offset and hystersis, since the effects of these impairments in the first and second comparators are attenuated by the second-order and fourth-order noise shaping, respectively. A simple dynamic comparator as shown in Fig. 6 is used to perform a single-bit conversion. During phase 2, when the latch signal is low, the differential outputs are reset to V_{DD}. As the latch signal turns high, the differential inputs control the resistance of the triode devices, M_{C1} and M_{C2}. Based on this differential resistance, the outputs of the cross-coupled inverters (M_{C3}, M_{C4}, M_{C7} and M_{C8}) flip in the appropriate direction. The outputs of the dynamic latch are stored in an *SR* latch that is implemented with CMOS NAND gates. Inverters buffer the outputs of the *SR* latches used in the comparators that drive NMOS switches connected to the negative reference voltage and PMOS switches connected to the positive reference voltage.

The integrators need a 2-phase non-overlapping clock (with delays) to minimize signal-dependent charge injection errors. The sampling operation at the input of the third integrator causes a brief disturbance at the output of the second integrator. If the regenerative latch in the first stage quantizer enters the regeneration phase before the output of the second integrator has recovered, an erroneous result may be produced. To avoid this problem, an early phase of ϕ_1, labeled ϕ_{1E}, is used to strobe the first-stage comparator. The timing of the phases and the speed of the latch are such that the subsequent sampling by the third integrator does not cause the latch to error.

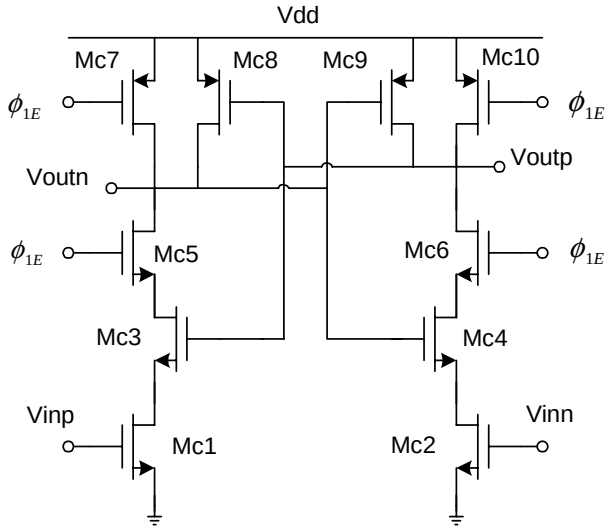

Fig. 6: Regenerative comparator.

4. SIMULATION RESULTS

The 2-2 cascaded Sigma-Delta modulator as shown in Fig. 3 has been simulated in a 0.6 μm double-poly triple metal (DPTM) CMOS process with poly-poly capacitors. The threshold voltages of this process are 0.85-V and –0.8-V for NMOS and PMOS transistors, respectively. The modulator samples at 6.4 MHz with 50 KHz Nyquist rate. All of the simulations have been performed with considering 20% bottom plate parasitic capacitance with HSPICE. Plots of *SNDR* and *DR* are shown in Figs. 7 and 8, respectively. The resultant *SNDR* and *DR* are 111 dB, 114 dB in the typical and 110 dB, 112 dB in the worst-case process corners, respectively. The simulated performance of the modulator is summarized in Table 2. It should be noted that the architecture of building blocks of the modulator in this work are different from [2,3,4].

5. CONCLUSION

In this paper a new 2-2 cascaded Sigma-Delta modulator with a maximized overload level factor was proposed, which is less sensitive to matching of digital and analog coefficients. It has overload level factor about –0.6 dBFS. The modulator has been designed in a 0.6-μm DPTM 5-V digital CMOS process with a single 3.3-V power supply. The resultant *SNDR* and *DR* are 111 dB and 114 dB, respectively. The modulator total power consumption is 65

mW. The power efficiency of the ADC's that has been obtained in the recent years, are compared with following figure of merit and shown in Fig. 9.

$$FM = \frac{4KT \times SNDR \times f_N}{P} \qquad (2)$$

where P and f_N are the total power dissipation of the converter and Nyquist rate, respectively, and $SNDR$ is expressed as a ratio rather than in dB.

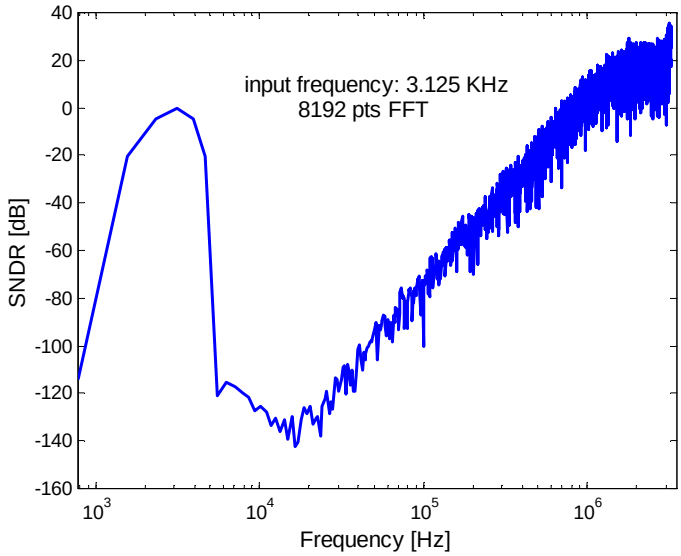

Fig. 7: Power spectral density.

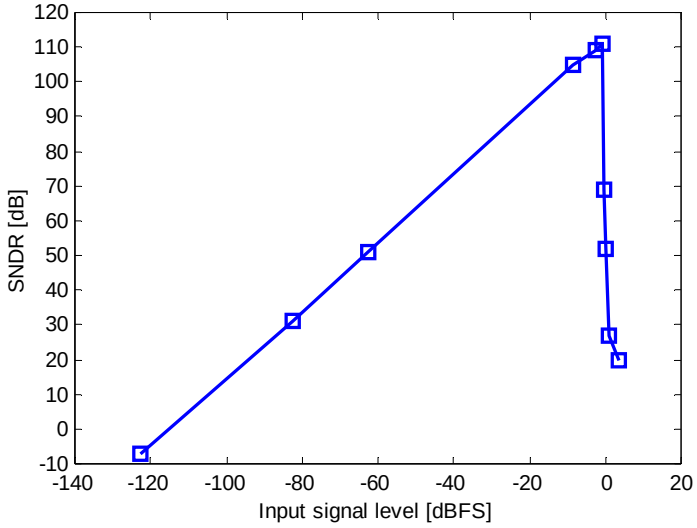

Fig. 8: Dynamic range.

Table 2: Simulated performance summary.

Parameter	Value
Dynamic Range	114 dB
Peak *SNDR*	110 dB
Overload level factor	-0.6 dBFS
Sampling rate	6.4 MHz
Signal bandwidth	25 KHz
Power supply voltage	3.3-V
Power dissipation	65 mW
Technology	0.6um, 5-V digital, DPTM CMOS

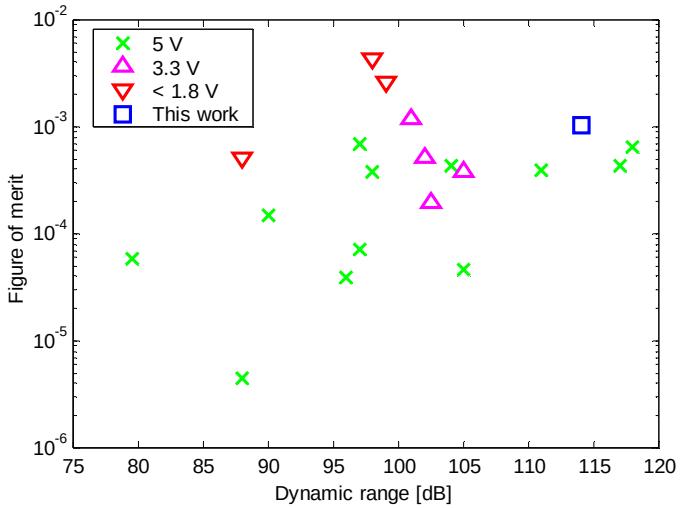

Fig. 9: Figure of merit vs. dynamic range.

REFERENCES

[1] S. R. Northworthy, R. Schreier, and G. C. Temes, "Delta-Sigma Data Converters," Piscataway, NJ: IEEE Press, 1997, ISBN 0-7803-1045-4.

[2] I. Fujimori, "A Single-Chip Stereo Audio Delta-Sigma A/D Converter with 117 dB Dynamic Range," IEICE Trans. Fundamentals, Vol. E83-A, No. 2, Feb. 2000.

[3] I. Fujimori et al., "A 5-V Single-Chip Delta-Sigma Audio A/D Converter with 111 dB Dynamic Range," IEEE J. Solid-State Circuits, Vol. 32, March, 1997.

[4] K. Y. Leung et al., "A 5V, 118dB ΔΣ Analog-to-Digital Converter for Wideband Digital Audio," ISSCC, 1997.

[5] A. Marques et al., "Optimal Parameters for ΔΣ Modulator Topologies," IEEE Trans. on circuits and systems-II, Sep. 1998.

[6] L. A. Williams, and B. A. Wooley, "A Third-Order Sigma-Delta Modulator with Extended Dynamic Range," IEEE J. Solid-State Circuits, Vol. 29, March 1994.

[7] Mohammad Yavari, *The Design of High-Resolution Sigma-Delta Analog to Digital Converters for Digital Audio*, MS.c. Dissertation thesis, ECE Department, University of Tehran, Sep. 2001.

[8] S. Brigati et al., " Modeling Sigma-Delta Modulator Non-idealities in SIMULINK," ISCAS, 1999.

[9] A. R. Feldman, B. E. Boser, and P. R. Gray, " A 13-Bit, 1.4-MS/s Sigma-Delta Modulator for RF Baseband Channel Applications," IEEE J. Solid-State Circuits, Vol. 33, Oct. 1998.

[10] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," IEEE J. Solid-State Circuits, Vol. 18, Dec. 1983.