A NOVEL FULLY-DIFFERENTIAL CLASS AB FOLDED-CASCODE OTA FOR SWITCHED-CAPACITOR APPLICATIONS

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ABSTRACT

This paper presents a new single-stage fully-differential class AB folded-cascode operational transconductance amplifier (OTA) for low-voltage and fast-settling switched-capacitor circuits in pure digital CMOS technology. The proposed OTA employs class AB operation in both the input-stage and output current source transistors resulting in large slew rate, enhanced unity-gain bandwidth and DC gain. The method to build the class AB operation in the output current source transistors is very simple which does not need any extra circuit and power consumption. HSPICE simulation results are presented to show the usefulness of the proposed OTA's structure.

1. INTRODUCTION

Design of high performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in analog circuits is the operational amplifier. Operational amplifiers are widely employed to drive large capacitive loads in many switched-capacitor applications such as the integrators, gain stages, etc. For high speed applications, fast-settling OTAs are required, which demand both high unity-gain bandwidth and slew rate. In class A OTAs the slew rate is limited by the bias currents. For example in folded-cascode OTA assuming equal currents of I_b in both input and cascode transistors, the slew rate can be considered as $SR = 2I_b/C_L$, where C_L is the load capacitor. So, a trade-off exists between the static power dissipation and the slewing behavior of a class A OTA. However, in class AB OTAs the slew rate is not limited by the quiescent currents since when a large input signal is applied, large currents are generated provided that the circuit is designed properly.

In this paper a single-stage class AB folded-cascode OTA which employs class AB operation in both the input-stage and output current source transistors is proposed which results in large slew rate. This technique also enhances the OTA's unity gain bandwidth and DC gain. Section (2) presents the proposed OTA structure. In section (3) circuit simulation results are discussed. Finally, conclusions are presented in section (4).

2. PROPOSED OTA TOPOLOGY

Figure 1 shows the proposed OTA structure. It employs the class AB operation in both input-stage and output current source transistors. To build the input-stage class AB operation, the proposed OTA uses two matched input transistors M1 and M2 cross-coupled by two constant voltage sources generated by two flipped voltage follower (FVF) cells acting as DC level shifters [1, 2, 6]. FVF cells composed of Mc1-Mc6 are used to build the floating voltage sources due to their very low output resistance instead of the conventional common drain structures [3]. Under quiescent conditions, i.e. when no input signal is applied, the gate voltage of input transistors M1 and M2 is the same. In this case, $V_{SG1} = V_{SG2} = Vb$, and both transistors carry equal currents which are controlled by Vb. Vb can be chosen slightly greater than the MOS threshold voltage which results in low quiescent currents. When an input signal is applied, a large current is generated in one of the input transistors. If for instance vin+ increases and vin- decreases, the source voltage of M2 increases whereas the voltage at the source of M1 decreases by the same amount. So, the drain current of M1 decreases while the drain current of M2 increases. Hence, the maximum current of M1 and M2 is independent of quiescent current when an input signal is applied.

To build the class AB operation in the output current source transistors, the gates of M9 and M10 are connected to those of Mc6 and Mc5, respectively, which results in large currents to flow during the slewing in one of cascode branches. If for instance, vin+ is greater than vin-, the drain current of M1 will be decreased while the drain current of M2 will be increased by the same amount. The drain current of Mc5 will be increased, and so M10, while the drain current of Mc6 and M9 will be decreased. On the

other hand, it can be also explained that the gate voltage of M3 and M4, cmfb, will be increased due to the sudden increment of the drain current and voltage of M2 through coupling of the gate-drain capacitor of M4 as it is seen in Fig. 2(a). The drain voltage of M2 increases greatly due to the enhancement of its drain current which results in raising the gate voltage of M3 and M4 through the gate-drain capacitance of M4. So, the drain current of M3 and M4 will be increased as shown in Fig. 2(b). Hence, the current of M10 will be forced to the positive output node, vout+, and the negative output node will be discharged by the current of M3. It is worth to mention that the increased drain current of M4 will be provided by M2 since due to the sudden increment of drain voltage of M2, the transistor M6 will be forced to cut-off. A similar improvement in the value of slew rate is obtained when a large negative input signal is applied to the proposed OTA. Therefore, a large slew rate will be obtained during both the positive and negative OTA's slewings.

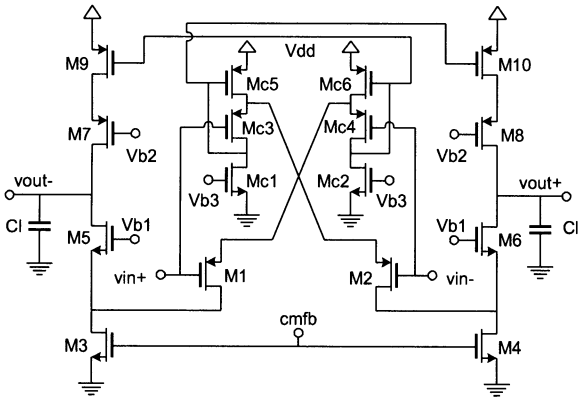

Figure 1: The proposed OTA.

If the gates of M9 and M10 are connected to a fixed bias voltage, their currents will be remained fixed during the OTA's slewing. In this case, when a large positive input signal is applied to the OTA, the positive output node will be charged only by the DC bias current of M10. So, the slew-rate of the proposed OTA will be much larger than that of folded-cascode OTA which employs class AB operation only in its input transistors.

The class AB operation of output current source transistors, M9 and M10, also enhances the OTA's small signal DC gain and unity-gain bandwidth. When a small signal is applied to the OTA's input, this signal also appears across the gate-source of output current source transistors, M9 and M10 through the FVF buffer cells, which in turn results in enhancing the DC gain of OTA. Also the effective transconductance of the input transistors are increased from $g_{m1,2}$ to about $g_{m1,2} + g_{m9,10}$ which enhances the OTA's unity-gain bandwidth by the same amount. It is worth mentioning that the class AB operation of the input-stage results in doubling the effective transconductance of input transistors, and hence doubling the unity-gain bandwidth and DC gain.

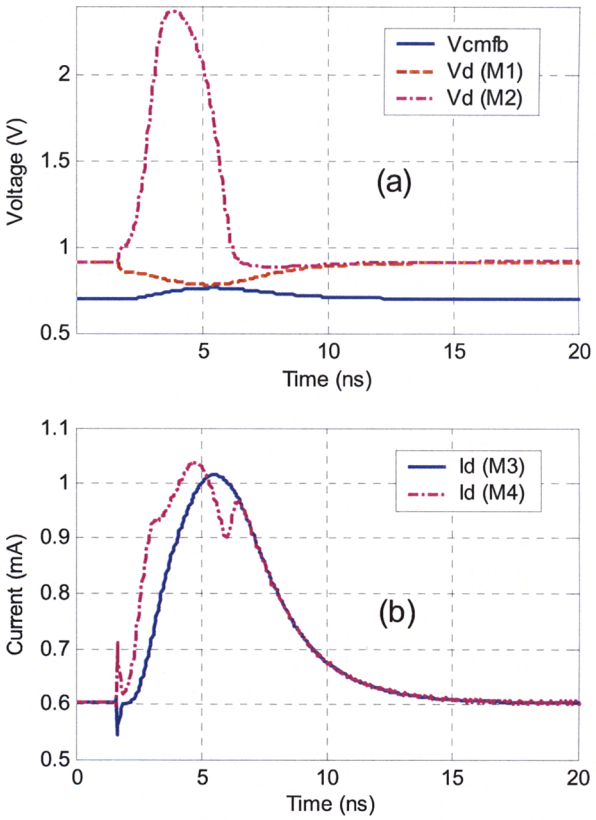

Figure 2: (a) Drain voltages of M3 and M4 and cmfb node voltage, and (b) drain currents of M3 and M4 during the positive slewing period.

The proposed OTA has the lowest power supply voltage requirement which is about $V_{GS} + V_{eff}$ where V_{eff} is the drain-source saturation voltage of an MOS transistor. To get a large output signal swing, a two-stage OTA can be utilized where the first stage can be the proposed OTA in this paper and the second stage is a common-source topology with a class AB operation. Cascode compensation and/or hybrid cascode compensation can be used to stabilize this two-stage OTA in fast-settling applications [4].

A simple switched-capacitor common mode feedback (CMFB) circuit such as proposed in [5] is used to define the common-mode voltage of output nodes of the proposed OTA.

3. SIMULATION RESULTS

To verify the usefulness of the proposed OTA, it was designed using a 0.25µm BSIM3v3 level 49 mixed-signal CMOS models with HSPICE for a switched-capacitor integrator with sampling and integrating capacitors of 2.5-pF and 10-pF, respectively. The load capacitance was 10-pF and 7.5-pF in AC open loop and transient closed loop simulations, respectively. The designed device sizes and circuit parameters are shown in Table 1. Figure 3 shows the frequency response of the proposed OTA including the conventional folded-cascode OTA called OTA1 here and the folded-cascode OTA with class AB operation only in its input-stage called OTA2 here. The settling performance of all three simulated OTAs is shown in Fig. 4. A summary of the simulation results is shown in Table 2. In these simulations, equal values for the transistors' dimensions and bias currents have been used. Simulation results show that the proposed OTA achieves unity-gain bandwidth of about three times that of the conventional folded-cascode (OTA1) and about two times that of the folded-cascode OTA employing class AB operation only in its input-stage (OTA2). Its settling time is much less than the other two topologies due to its large slew rate and also unity-gain bandwidth. The proposed OTA also achieves about 3.6-dB and 10-dB DC gain greater than the class AB input-stage and conventional folded-cascode OTAs, respectively. The slew rate of class AB input-stage OTA is about the same as that of the conventional folded-cascode since when a positive input signal is applied, its positive output node is charged only by the bias current of M10.

Table 1: Circuit Parameters.

Parameter	Proposed OTA	OTA2	OTA1
$(W/L)_{M1, M2}$	50/0. 4	50/0. 4	50/0. 4
$(W/L)_{M3, M4}$	80/0.5	80/0.5	80/0.5
$(W/L)_{M5, M6}$	40/0. 4	40/0. 4	40/0. 4
$(W/L)_{M7, M8}$	100/0. 5	100/0. 5	100/0.5
$(W/L)_{M9, M10}$	50/0. 5	50/0.5	50/0.5
$(W/L)_{Mc1, Mc2}$	20/0.25	20/0.25	---
$(W/L)_{Mc3, Mc4}$	20/0.4	20/0.4	---
$(W/L)_{Mc5, Mc6}$	60/0.5	60/0.5	---
$(W/L)_{11}$	---	---	100/0.5

4. CONCLUSION

In this paper a novel fully-differential class AB folded-cascode OTA was proposed. The proposed OTA topology offers enhanced slew rate, unity-gain bandwidth, and DC gain by employing a simple technique to build the class AB operation in the output current source transistors in addition to using the conventional class AB input-stage. The method to build the class AB operation in the output current source transistors is simply realized by proper connection between the input-stage and the output stage nodes with no extra transistors and power dissipation.

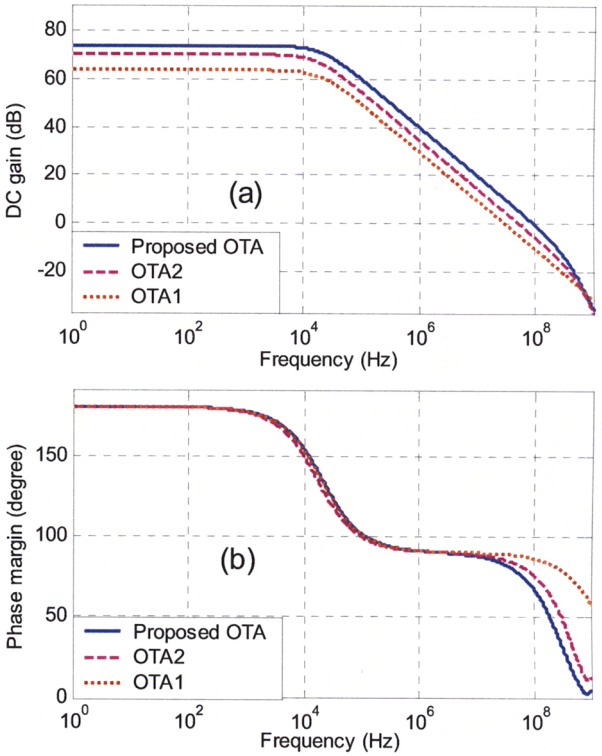

Figure 3: Frequency response simulation results: (a) DC gain and (b) phase margin.

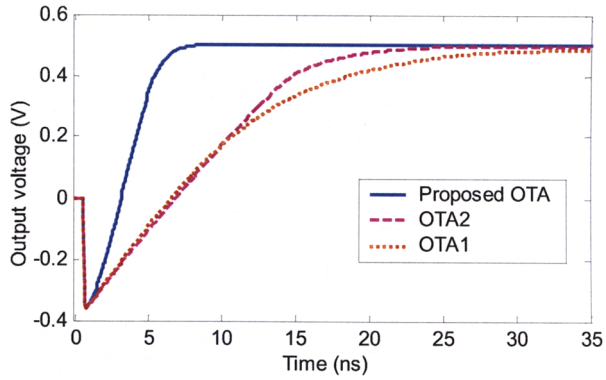

Figure 4: Settling simulation results when a large positive step signal is applied to the inputs of the integrator.

Table 2: Simulation results summary.

Parameter	Proposed OTA	OTA2	OTA1
DC gain (dB)	73.6	70	63.5
Unity gain bandwidth (MHz)	94.3	52.6	30
Phase margin (degree)	68.8	82.7	89.8
Slew rate (V/μs)	197	56	57
0.01% settling time (ns)	7.2	23.6	31.9
V_{DD} (V)	3	3	3
Power dissipation (mW)	4.33	4.36	4.35

5. REFERENCES

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