A NEW COMPENSATION TECHNIQUE FOR TWO-STAGE CMOS OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

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ABSTRACT

This paper presents a new compensation method for fully differential two-stage CMOS operational transconductance amplifiers (OTAs). It employs a hybrid cascode compensation scheme, merged Ahuja and improved Ahuja style compensations, for fast settling. A design procedure for minimum settling time of the proposed compensation technique for a two-stage class A/AB OTA is described. To demonstrate the usefulness of it, three design examples are considered.

1. INTRODUCTION

Design of high performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in an analog circuit is the operational amplifier. The realization of a CMOS operational amplifier that combines high dc gain with high unity gain bandwidth has been a difficult problem especially in low voltage circuits. The high dc gain requirement leads to multistage designs or cascoding of transistors with long channel devices biased at low current levels, whereas the high unity gain frequency requirement calls for a single stage design with short channel devices biased at high bias current levels. Cascoding is a well-known means to enhance the dc gain of an amplifier without degrading the high frequency performance. But cascoding is not possible in the low voltage circuits. Another technique to achieve both high DC gain and unity gain bandwidth is to employ gain boosting [1], [2]. But in this technique at least four transistors should be cascoded at the output, which decreases the output voltage swing. In the other hand, a two-stage OTA can be used to satisfy the high dc gain requirement for high-speed applications.

Design of two-stage opamps needs some forms of compensation to maintain the stability. It has been shown that the cascode compensation scheme yields a higher amplifier bandwidth compared to the conventional miller compensation [3]. In this paper a hybrid cascode compensation technique is proposed which results in fast settling in two-stage opamps.

In section (2) a two-stage class A/AB OTA structure with new compensation method is considered and analyzed and a set of system parameters is also obtained. Design procedure for this OTA with its proposed compensation method is described in section (3). Section (4) presents simulation results. Finally, conclusions are summarized in section (5).

2. PROPOSED COMPENSATION TECHNIQUE

Fig. 1 shows a two-stage class A/AB OTA structure [4]. The first stage is a folded cascode amplifier with PMOS input transistors. The second stage is a class AB amplifier with active current mirrors. Due to class AB operation of this stage, slew limiting only occurs in the first stage which results in low power consumption.

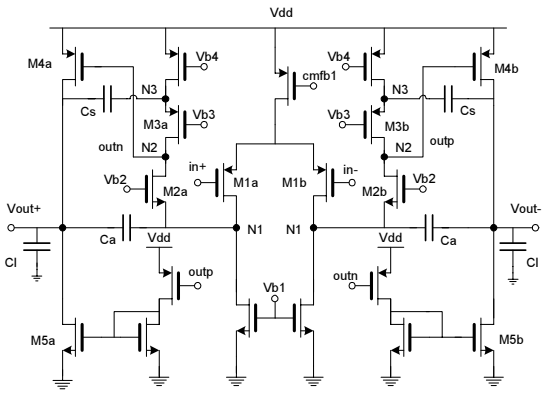

Fig. 1: A two-stage class A/AB OTA with proposed compensation method.

Frequency compensation is needed to maintain stability in a two-stage amplifier. The standard miller compensation has a pole splitting effect, which moves one pole to a lower frequency and the other to a higher frequency [5]. The two-stage amplifier shown in Fig. 1 employs the hybrid cascode compensation scheme, merged Ahuja [3] and improved Ahuja style [6] compensation methods, which creates two real poles, two complex poles at a higher frequency, and three zeros. This scheme of compensation yields a higher amplifier bandwidth compared to the standard miller and conventional cascode compensation techniques at the cost of more complex design procedure for the settling behavior of the amplifier. Since the proposed compensation scheme creates an amplifier with four

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closed-loop poles and three zeros, the design equations become significantly more complicated than those of a single-stage or conventional miller and cascode compensated two-stage amplifier. This implies that for practical designs some form of computer optimization constrained by the tradeoffs in the design equations will be necessary.

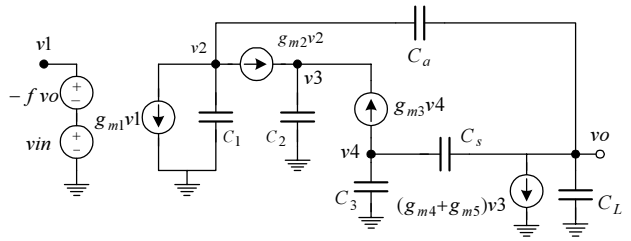

Fig. 2: Closed-loop small-signal equivalent circuit.

Fig. 2 shows the closed-loop small-signal equivalent circuit for pole and zero analysis of the proposed OTA shown in Fig. 1, where C_1, C_2, C_3, and C_L represent the parasitic capacitances of nodes N_1, N_2, N_3, and the output node of the circuit shown in Fig. 1, respectively. f is the feedback factor. To simplify the analysis, device output resistances are assumed to be infinite. It should be noted that the effect of finite device resistance is to move the amplifier poles slightly to the left, which will slightly increase the bandwidth of the amplifier [7]. The node equations of this circuit are as follows:

$$\begin{cases} g_{m1}v1+(sC_1+g_{m2})v2+sC_a(v2-vo)=0 \\ sC_2\,v_3-g_{m2}\,v2-g_{m3}\,v4=0 \\ (sC_3+g_{m3}+sC_s)v4-sC_s\,vo=0 \\ (sC_L+sC_a+sC_s)vo-sC_a v2+(g_{m4}+g_{m5})v3-sC_s v4=0 \\ v1=vin-f\,vo \end{cases} \quad (1)$$

The transfer function will be as follows:

$$\frac{vo}{vin}=\frac{g_{m1}\,(s^2C_a\,C_2-g_{m2}\,g_m)(g_{m3}+sC_3+sC_s)}{s^4\,d4+s^3\,d3+s^2\,d2+s\,d1+d0} \quad (2)$$

where

$$g_m=g_{m4}+g_{m5} \quad (3)$$

$$d4=C_a^2C_2(C_3+C_s)+C_s^2C_2(C_1+C_a) -C_2(C_L+C_a+C_s)(C_1+C_a)(C_3+C_s) \quad (4)$$

$$d3=C_aC_2f\,g_{m1}(C_3+C_s)+C_a^2C_2g_{m3}+C_2C_s^2g_{m2} -g_{m2}C_2(C_L+C_a+C_s)(C_s+C_3) -g_{m3}C_2(C_L+C_a+C_s)(C_1+C_a) \quad (5)$$

$$d2=f\,g_{m1}g_{m3}C_aC_2-g_{m2}g_mC_a(C_3+C_s) -g_{m3}g_mC_s(C_1+C_a)-g_{m2}g_{m3}C_2(C_L+C_a+C_s) \quad (6)$$

$$d1=-f\,g_{m1}g_{m2}g_m(C_3+C_s)-g_{m2}g_{m3}g_mC_a -g_{m2}g_{m3}g_mC_s \quad (7)$$

$$d0=-f\,g_{m1}\,g_{m2}\,g_{m3}\,g_m. \quad (8)$$

In order to verify the usefulness of the proposed compensation technique, the settling time of Ahuja style, improved Ahuja style, and the proposed compensation techniques are shown as a function of the total compensation capacitance in Fig. 3. In these simulations the small signal parameters shown in Table (1) have been used. The proposed compensation technique can give a smaller settling time compared to the other alternatives.

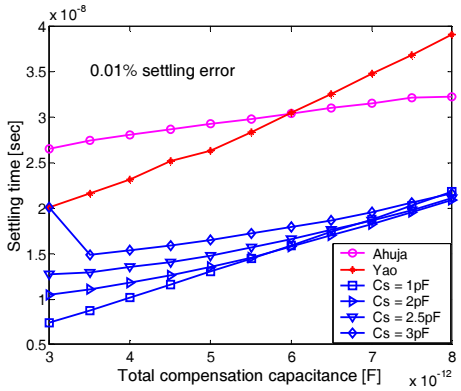

Fig. 3: Settling time with different compensation techniques.

Table (1): Small-signal parameters.

Parameter	Value	Parameter	Value
g_{m1}	4 mA/V	C_1 [pF]	0.206
g_{m2}	4.7 mA/V	C_2 [pF]	0.627
g_{m3}	4.2 mA/V	C_3 [pF]	0.267
g_{m4}	5.7 mA/V	C_L [pF]	4
g_{m5}	7.4 mA/V	f	0.8

3. DESIGN PROCEDURE

In order to investigate the settling behavior of the proposed compensation technique a standard fourth order system with the following transfer function is considered

$$H(s)=\frac{k(z_p^2-s^2)(s+c)}{(s+a)(s+b)(s^2+2\zeta\omega_n s+\omega_n^2)} =\frac{k(\gamma^2\zeta^2\omega_n^2-s^2)(s+z\zeta\omega_n)}{(s+\alpha\zeta\omega_n)(s+\beta\zeta\omega_n)(s^2+2\zeta\omega_n s+\omega_n^2)} \quad (9)$$

where $a=\alpha\zeta\omega_n$, $b=\beta\zeta\omega_n$, $c=z\zeta\omega_n$ and $z_p=\gamma\zeta\omega_n$.

There are six system parameters, α, β, γ, ω_n, ζ and z in the transfer function. ω_n and ζ are called natural frequency and damping factor, respectively. Fig. 4 shows the description of these six system parameters by the location of poles and zeros of the proposed compensation technique in a practical implementation.

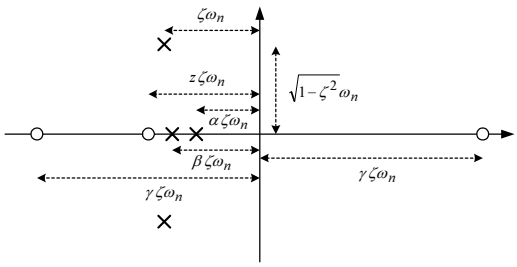

Fig. 4: Closed-loop pole and zero locations.

In switched-capacitor circuits, the step response determines the amplifier settling performance in the time domain. It can be shown that the step response of the above-mentioned fourth order system is as follows:

$$\begin{aligned} s(t) = A_{cl}\{1 - a1\times e^{-\alpha\zeta\omega_n t} - a2\times e^{-\beta\zeta\omega_n t} \\ + a3\times e^{-\zeta\omega_n t}\left(a4\times\cos(\omega_n t\sqrt{1-\zeta^2})\right) \\ - a3\times e^{-\zeta\omega_n t}\left(a5\times\sin(\omega_n t\sqrt{1-\zeta^2})\right)\} \end{aligned} \quad (10)$$

Where A_{cl} is the closed-loop gain and

$$a1 = \frac{\beta(z-\alpha)}{z(\beta-\alpha)(1-2\alpha\zeta^2+\alpha^2\zeta^2)} \quad (11)$$

$$a2 = \frac{\alpha(z-\beta)}{z(\alpha-\beta)(1-2\beta\zeta^2+\beta^2\zeta^2)} \quad (12)$$

$$a3 = \frac{\alpha\beta\zeta}{z(1-2\alpha\zeta^2+\alpha^2\zeta^2)(1-2\beta\zeta^2+\beta^2\zeta^2)} \quad (13)$$

$$\begin{aligned} a4 = -z\zeta\left((\alpha-1)(\beta-1)\zeta^2 - 1 + \zeta^2\right) \\ + (\alpha\zeta^2-1)(\alpha+\beta-2)\zeta \end{aligned} \quad (14)$$

$$\begin{aligned} a5 = \left\{(z\zeta^2-1)\left((\alpha-1)(\beta-1)\zeta^2 - 1 + \zeta^2\right)\right. \\ \left. + z\zeta^2(1-\zeta^2)(\alpha+\beta-2)\right\}\frac{1}{\sqrt{1-\zeta^2}}. \end{aligned} \quad (15)$$

In the calculation of the step response it is assumed that γ goes to infinity since in the practical cases the right and left-plane z_p zero pair in the closed loop transfer function will be at much higher frequencies than the poles.

The settling error as defined $\varepsilon_s = \frac{s(\infty) - s(t_s)}{s(\infty)}$ is obtained by:

$$\begin{aligned} \varepsilon_s = a1\times e^{-\alpha\zeta\omega_n t_s} + a2\times e^{-\beta\zeta\omega_n t_s} \\ - a3\times e^{-\zeta\omega_n t_s}\left(a4\times\cos(\omega_n t_s\sqrt{1-\zeta^2})\right) \\ + a3\times e^{-\zeta\omega_n t_s}\left(a5\times\sin(\omega_n t_s\sqrt{1-\zeta^2})\right). \end{aligned} \quad (16)$$

This equation is very complex to intuitively explain how to choose the system parameters to optimize the settling error. Therefore, numerical calculations are used. Fig. 5 shows the settling error of the proposed compensation technique for different values of the system parameters. The obtained system parameters for –120 dB settling error are $\alpha = 0.95$, $\zeta = 0.9$, $z = 0.9$, $\beta = 0.95$ and $\omega_n t_s = 17$.

The obtained system parameters for a specific settling error in a defined time can be used to determine the device parameters with the following equations:

$$(\alpha+\beta+2)\omega_n\zeta = \frac{d3}{d4} \quad (17)$$

$$\left(2(\alpha+\beta)\zeta^2 + \alpha\beta\zeta^2 + 1\right)\omega_n^2 = \frac{d2}{d4} \quad (18)$$

$$\left((\alpha+\beta)\zeta + 2\zeta^3\alpha\beta\right)\omega_n^3 = \frac{d1}{d4} \quad (19)$$

$$\alpha\beta\zeta^2\omega_n^4 = \frac{d0}{d4} \quad (20)$$

$$z\zeta\omega_n = \frac{g_{m3}}{C_s + C_3}. \quad (21)$$

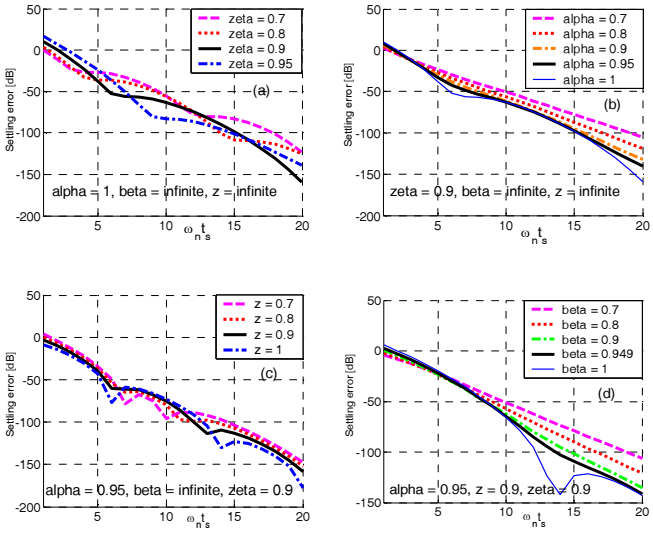

Fig. 5: Settling errors as a function of $\omega_n t_s$ for different values of (a) ζ, (b) α, (c) z, and (d) β.

In these equations, the system parameters, α, β, z, ζ, and ω_n are known. The load and compensation capacitances, C_L, C_a, and C_s are determined due to circuit noise considerations. The parasitic capacitances, C_1, C_2, and C_3 are related to the device sizes. Also all of device transconductances can be expressed by transistor sizes. So, these equations can be solved to determine the device sizes using numerical calculations. However, these equations are very complex to solve. In order to achieve a coarse design of the proposed opamp, some approximations are considered to simplify the solution of the above-mentioned equations and also give an insight to them. In equations (4-7) the parasitic capacitances, C_1, C_2, and C_3 are assumed to be much less than the other capacitances. In this case, equations (17-21) reduce to the following relations:

$$\begin{aligned} (\alpha+\beta+2)\omega_n\zeta = -\frac{f\,g_{m1}}{C_L} + \frac{g_{m2}(C_L+C_a)}{C_a C_L} \\ + \frac{g_{m3}(C_L+C_s)}{C_s C_L} \end{aligned} \quad (22)$$

$$\begin{aligned} \left(2(\alpha+\beta)\zeta^2 + \alpha\beta\zeta^2 + 1\right)\omega_n^2 = -\frac{f\,g_{m1}\,g_{m3}}{C_s C_L} \\ + \frac{(g_{m2}+g_{m3})g_m}{C_2 C_L} + \frac{g_{m2}\,g_{m3}(C_L+C_a+C_s)}{C_a C_s C_L} \end{aligned} \quad (23)$$

$$\left((\alpha+\beta)\zeta+2\zeta^3\alpha\beta\right)\omega_n^3=\frac{f\,g_{m1}g_{m2}g_m}{C_2C_aC_L}+\frac{g_{m2}g_{m3}g_m(C_a+C_s)}{C_2C_aC_sC_L} \quad (24)$$

$$\alpha\beta\zeta^2\omega_n^4=\frac{f\,g_{m1}g_{m2}g_{m3}g_m}{C_2C_aC_sC_L} \quad (25)$$

$$z\zeta\omega_n=\frac{g_{m3}}{C_s}. \quad (26)$$

In these equations, the transconductance of transistors M_1, M_2, M_3, and $M_{4,5}$ and the parasitic capacitance of node N_2, C_2 are unknown and can be obtained by solving them. Then one can run circuit level simulations to fine the obtained gate dimensions from system level calculations.

4. SIMULATION RESULTS

In order to demonstrate the usefulness of the proposed compensation technique, three different design examples with Ahuja style, improved Ahuja style, and the proposed compensation techniques were considered in the circuit level. At first, the system parameters of these design examples were obtained using their settling error equations with numerical calculations. Then, their circuits were simulated in a 0.25-µm CMOS technology with HSPICE. In these simulations, the OTAs were designed for a fully differential switched-capacitor integrator where sampling, integrating and load capacitances are 2.5pF, 10pF and 2pF, respectively. The bootstrapped switches proposed in [8] have been used in these designs. In Fig. 6 the settling behavior of the proposed OTA with three different compensation methods are shown. Simulation results are given in Table (2).

5. CONCLUSIONS

In this paper a new compensation technique for two-stage CMOS OTAs has been proposed. It employs merged cascode compensation technique, which results in fast settling compared to conventional miller, Ahuja style, and improved Ahuja style compensation techniques at the cost of more complex design procedure. A design procedure is also considered for the proposed OTA.

6. ACKNOWLEDGEMENT

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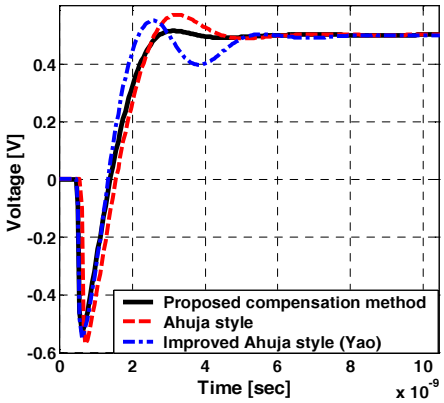

Fig. 6: Settling simulation results.

Table (2): Simulation results.

Parameter	Ahuja	Improved Ahuja	Proposed method
Power supply voltage	1.5-V	1.5-V	1.5-V
DC gain [dB]	80.3	79	80
Unity gain bandwidth [MHz]	137	151	167
Phase margin [degree]	75.5	89	73.5
Compensation cap.	3 pF	3 pF	3 pF
Load capacitance	4 pF	4 pF	4 pF
Settling time (0.01%)	10.1 ns	12.4 ns	7.1 ns
Output swing [V_{pp}]	1.13	1.13	1.13
Input referred thermal noise [V^2/Hz]	1.6×10^{-16}	1.5×10^{-16}	1.2×10^{-16}
Power consumption	8.9 mW	8.9 mW	8.9 mW

7. REFERENCES

[1] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS opamp for SC circuits with 90-dB DC gain," *IEEE Journal Solid-State Circuits*, vol. 25, no. 6, 1379-1384, Dec. 1990.

[2] K. Gulati and H.-S. Lee, "A high-swing CMOS telescopic operational amplifier," *IEEE Journal Solid-State Circuits*, vol. 33, no. 12, pp. 2010-2019, Dec. 1998.

[3] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE Journal Solid-State Circuits*, vol. 18, no. 6, pp. 629-633, Dec. 1983.

[4] M. Yavari and O. Shoaei, "Very low-voltage, low-power and fast-settling OTA for switched-capacitor applications," *in 14th IEEE International Conference on Microelectronics, ICM*, pp. 10-13, Dec. 2002.

[5] B. Razavi, *Design of analog CMOS integrated circuits*, McGraw-Hill, 2000.

[6] L. Yao, M. Steyaert, and W. Sansen, "Fast-settling CMOS two-stage operational transconductance amplifiers and their systematic design," *IEEE Symposium on Circuits and Systems*, ISCAS, vol. 2, pp 839-842, May 2002.

[7] A. Feldman, *High-speed, low-power sigma-delta modulators for RF baseband channel applications*, Ph.D. Dissertation, University of California at Berkeley, 1997.

[8] M. Dessouky and A. Kaiser, "Very low-voltage digital audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE Journal Solid-State Circuits*, vol. 36, no. 3, pp. 349-355, March 2001.