# Accurate and Simple Modeling of Amplifier DC Gain Nonlinearity in Switched-Capacitor Circuits†

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***Abstract*: This paper presents an accurate and simple model for dc gain nonlinearity of operational amplifiers used in the switched-capacitor circuits such as the sigma-delta modulators. The proposed model can simply be used in the time-domain system level simulation of sigma-delta modulators to evaluate the effect of amplifier's dc gain nonlinearity on the overall linearity of the modulator as well as in the other switched-capacitor circuits as explored in the paper.**

## I. INTRODUCTION

One of the most important factors that may limit the performance of switched-capacitor circuits is the finite dc gain in the operational amplifier. Owing to this, the amplifier's inverting input terminal in a switched-capacitor circuit does not provide a perfect virtual ground, thereby causing errors in the charge transfer between the capacitors.

Although the amplifier's finite dc gain introduces gain-error in switched-capacitor circuits, however, a more serious effect of the finite amplifier dc gain is that of nonlinearity introduced by variations in the amplifier's open loop gain. The dc gain of a CMOS amplifier varies with the amplifier's output voltage due to the dependency of the output resistance of an MOS transistor on its drain-to-source voltage [1]. The nonlinear dc gain results in harmonic distortion in the switched-capacitor circuits.

Although there have been reported a number of system level models for switched-capacitor oversampling A/D converters to consider the analog circuit imperfections such as the amplifier's finite dc gain and output swing, however, many of them either are not considering the accurate modeling of amplifier's dc gain nonlinearity [2, 3] or using a complicated modeling to account into the dc gain nonlinearity at the behavioral simulations [4-6].

This paper presents a simple and accurate model for dc gain nonlinearity in an operational amplifier. Based on this model, behavioral models for switched-capacitor gain-stages and integrators which are widely used in pipelined and sigma-delta A/D converters, respectively, are driven. Finally, the system and circuit level simulation results are provided to show the accuracy of the proposed behavioral models.

## II. AMPLIFIER DC GAIN NONLINEARITY

The dc gain nonlinearity of an MOS amplifier can be modeled by accurate representing the drain-source resistance's variation of an MOS transistor with its drain-source voltage. In [7] an accurate relation has been derived which shows the dependency of drain-source resistance of an MOS transistor upon its drain-source voltage. However, this relation results in complicated dc gain variation of an amplifier upon its output swing and hence does not give any simple modeling. Therefore, a simple yet accurate modeling for dc gain nonlinearity of an MOS operational amplifier is proposed here which is given by

$$A_{dc}(v_o) = A_0\left(1 - \delta\,\frac{|v_o - v_{cmo}|^{\rho}}{|v_{o,max}|^{\rho}}\right) \tag{1}$$

where $A_0$ corresponds to the dc gain at the mid-level output, i.e. $v_{cmo}$, $\delta$ is the dc gain variation over the amplifier output swing which spans from $-v_{o,max}$ to $v_{o,max}$, and $\rho$ is a fitting parameter which can be selected between 2 and 4. $v_{o,max}$ is the maximum output swing where the output transistors remain in saturation yet. It should be noted that the relation expressed in (1) gives valid results until that all of the transistors in the amplifier remain in saturation when the output voltage changes.

It should be noted that when $\rho$= 2, the proposed dc gain nonlinearity model in (1) corresponds to a *tanh* relation of the amplifier's input-output characteristics which has been used in the previously reported works [6, 8]. Because, by representing the amplifier's input-output relation as

$$v_{out} = a \times \tanh(b \times v_{in}) \tag{2}$$

the dc gain nonlinearity is obtained as follows

$$\begin{aligned} A_{dc}(v_o) = \frac{dv_o}{dv_{in}} &= a \times b\left(1 - (\tanh(b \times v_{in}))^2\right) \\ &= a \times b\left(1 - \frac{v_{out}^2}{a^2}\right) = b\left(a - \frac{v_{out}^2}{a}\right) \end{aligned} \tag{3}$$

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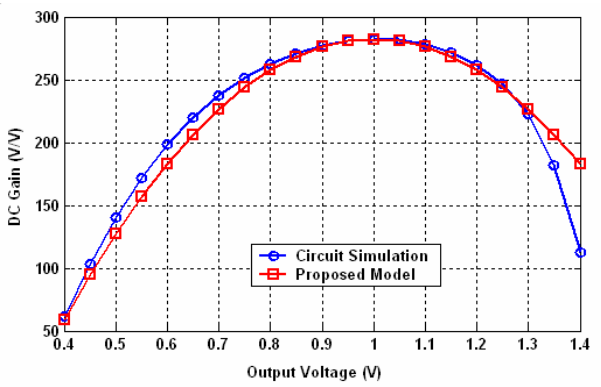


**Fig. 1:** Amplifier nonlinear dc gain versus its output swing.

Figure 1 shows the dc gain nonlinearity of a folded-cascode CMOS amplifier with pMOS input differential pair. This amplifier was designed and simulated in HSPICE with a 0.18µm CMOS technology. In this figure, the proposed amplifier dc gain nonlinearity model in (1) with parameters $A_0$ = 49 dB, $v_{o,max} = 0.5\,\mathrm{V}$, $v_{cmo} = 1\mathrm{V}$, $\delta = 0.55$ and $\rho = 2$ is also shown. As is seen the proposed model has the sufficient accuracy although it is very simple.

## III. DC Gain Nonlinearity in SC Circuits

### A. Switched-Capacitor Gain-Stage

The transfer function of the switched-capacitor gain-stage shown in Fig. 2 with a finite amplifier dc gain of $A$ is given by

$$H_g(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_S + C_F}{C_F} \frac{z^{-1/2}}{1 + (C_S + C_F)/(C_F A)} \tag{4}$$

As is seen from (4), the amplifier's finite dc gain results only in a gain error without any harmonic distortion. However, by considering the amplifier's dc gain variation as proposed in (1), the actual transfer function of a switched-capacitor gain-stage can be modeled as shown in Fig. 3 where $f(x)$ is given by

$$f(x) = A_0 \left( 1 - \delta \frac{|x - v_{cmo}|^{\rho}}{|v_{o,max}|^{\rho}} \right) \tag{5}$$

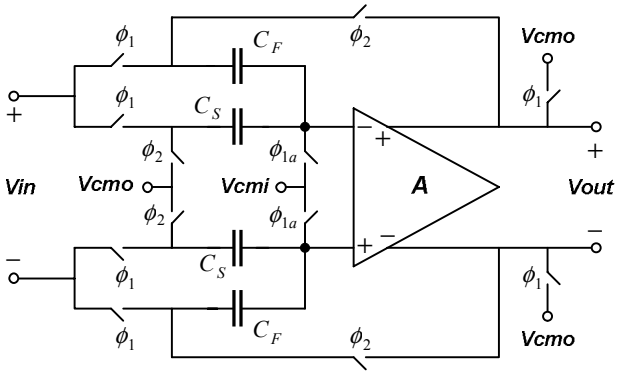


**Fig. 2:** A switched-capacitor gain-stage.

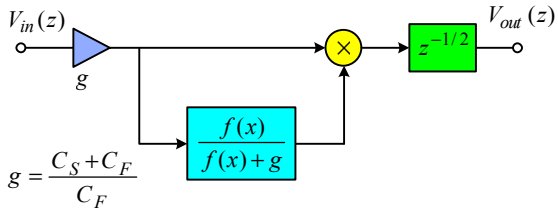

**Fig. 3:** Modeling the dc gain nonlinearity in a SC gain-stage.

It is worth mentioning that in deriving the model shown in Fig. 3, it was assumed that the amplifier's output voltage of the switched-capacitor gain-stage is directly depends on its input voltage without any nonlinearity. This is a first-order approximation since without assuming that, the dependence of the dc gain on the instantaneous output voltage does not result in any causal system level modeling.

The model proposed in Fig. 3 clearly shows that any nonlinearity in the amplifier's dc gain results in harmonic distortion in the switched-capacitor gain-stage as it is expected.

### B. Switched-Capacitor Integrator

The transfer function of the one-sample delaying integrator shown in Fig. 4 with a finite amplifier's dc gain is given by

$$H_i(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_S}{C_I} \frac{(1-\varepsilon_1)z^{-1}}{1-(1-\varepsilon_2)z^{-1}} \tag{6}$$

where $\varepsilon_1$ and $\varepsilon_2$ represent the integrator gain error and leakage, respectively, and are as follows

$$\varepsilon_1 = \frac{C_S + C_I}{(A+1)C_I + C_S}, \quad \varepsilon_2 = \frac{C_S}{(A+1)C_I + C_S} \tag{7}$$

As is seen a finite dc gain in an integrator manifests itself as both an integrator leakage and gain error. The finite dc gain in the integrators affects the noise transfer function of the ΣΔ modulator and increases the inband quantization noise. The resulting model in (6) and (7) can easily be used in the system level simulations to account into the effect of amplifier's finite dc gain.

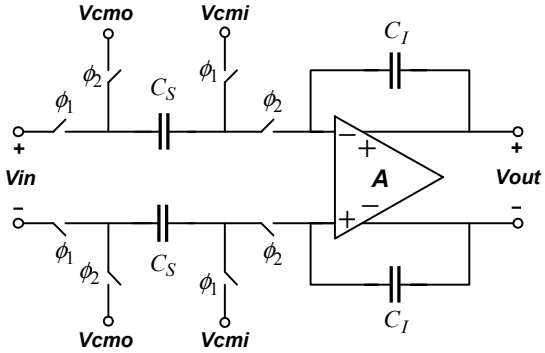


**Fig. 4:** A switched-capacitor one-sample delaying integrator.

Although the finite dc gain in the amplifier may result in integrator leakage and gain error and, hence, can affect the noise transfer function of the modulator, however, a more serious effect of the finite amplifier dc gain is that of nonlinearity introduced by variations in the amplifier's open loop gain. The effect of nonlinear dc gain in a switched-capacitor integrator can be accounted into by using the relation (1) in (6) and (7). However, the resulting model needs the instantaneous estimation of the output voltage of the integrator and that is very difficult because in this case $\varepsilon_1$ and $\varepsilon_2$ are also functions of the instantaneous output voltage that itself depends on $\varepsilon_1$ and $\varepsilon_2$ at the same time. Hence, there is a delay free loop. Therefore, a first-order estimation of $\varepsilon_1$, $\varepsilon_2$ and output voltage at sampling instance $n$ is considered by excluding the dependency of $\varepsilon_1$ and $\varepsilon_2$ on the output voltage that results in dc gain nonlinearity relations for delaying and delay free integrators, respectively, given by

$$A_{dc}\left(v_o[n]\right) = A_0\left\{1 - \frac{\delta}{|v_{o,max}|^{\rho}} \times \left| \frac{1+A_0}{a+1+A_0}\, v_o[n-1] - v_{cmo} + \frac{a A_0}{a+1+A_0}\, v_{in}[n-1] \right|^{\rho}\right\} \tag{8}$$

$$A_{dc}\left(v_o[n]\right) = A_0\left\{1 - \frac{\delta}{|v_{o,max}|^{\rho}} \times \left| \frac{1+A_0}{a+1+A_0}\, v_o[n-1] - v_{cmo} - \frac{a A_0}{a+1+A_0}\, v_{in}[n]\right|^{\rho}\right\} \tag{9}$$

The resulting dc gain nonlinearity model for both switched-capacitor one-sample delaying and delay free integrators are shown in Figs. 5 and 6, respectively, where $a$ is the integrator's ideal gain and $f(x)$ and $g(x)$, respectively, are given by

$$f(x) = \frac{A_0\left(1 - \delta \dfrac{|x - v_{cmo}|^{\rho}}{|v_{o,max}|^{\rho}}\right)}{A_0\left(1 - \delta \dfrac{|x - v_{cmo}|^{\rho}}{|v_{o,max}|^{\rho}}\right) + a + 1} \tag{10}$$

$$g(x) = \frac{A_0\left(1 - \delta \dfrac{|x - v_{cmo}|^{\rho}}{|v_{o,max}|^{\rho}}\right) + 1}{A_0\left(1 - \delta \dfrac{|x - v_{cmo}|^{\rho}}{|v_{o,max}|^{\rho}}\right) + a + 1} \tag{11}$$

The proposed models can simply be used at the behavioral level simulations of sigma-delta modulators using the softwares such as MATLAB and SIMULINK.

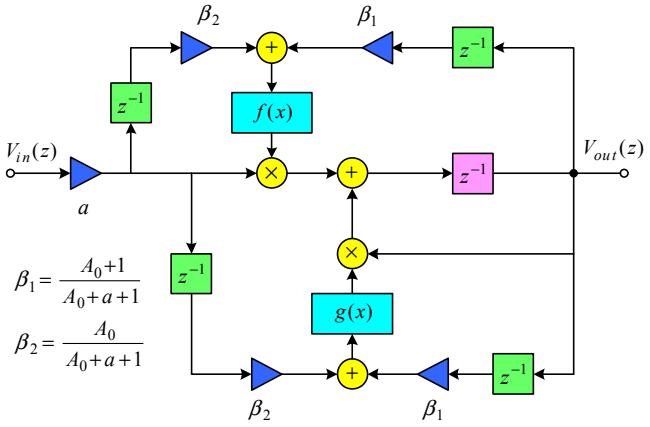


**Fig. 5:** Modeling the dc gain nonlinearity in a delaying integrator.

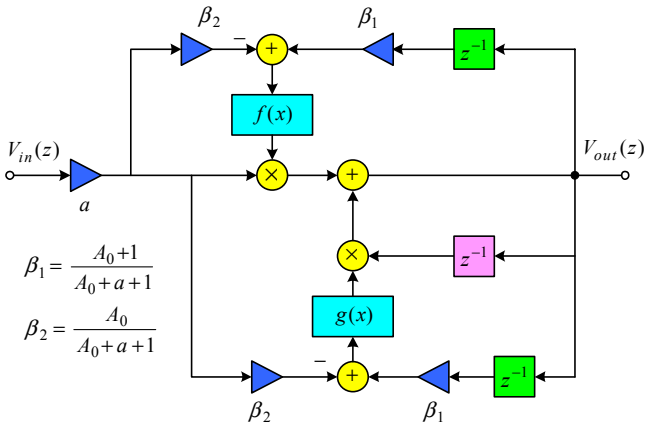


**Fig. 6:** Modeling the dc gain nonlinearity in a delay free integrator.

## IV. Simulation Results

In this section, circuit level simulations are provided to show the accuracy and usefulness of the proposed models for dc gain nonlinearity of switched-capacitor gain-stages and integrators. All of the circuits' simulations were performed in HSPICE using a 0.18µm CMOS technology. In these simulations the same folded-cascode amplifier where its dc gain dependence on its output voltage swing has been shown in Fig. 1, was used. Also, in the system level simulations, to account into the dc gain nonlinearity of the amplifier in the proposed models, the same parameters used in plotting the Fig. 1 were employed. Besides, in the circuit level simulations only the actual amplifier were used and the other circuits such as the switches employed ideal elements.

Fig. 7 shows the output spectrum of the switched-capacitor gain-stage with a gain of 2 and amplifier's dc gain characteristics proposed in Fig. 3 whereas Fig. 8 shows the resulted output spectrum from the circuit level simulations. As is seen from these figures, the error in estimations of both SNDR and SFDR is very negligible.

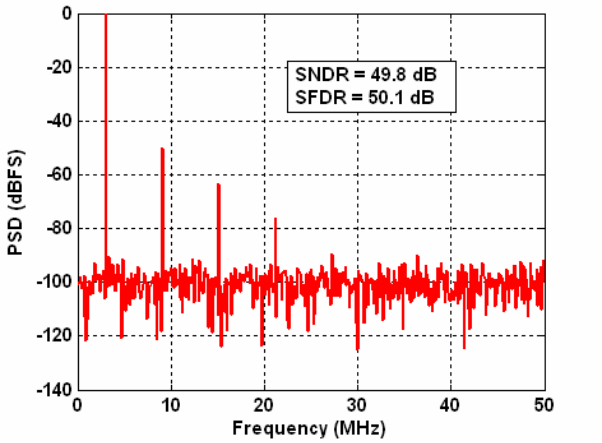


**Fig. 7:** Output spectrum of a SC gain-stage using the proposed model.

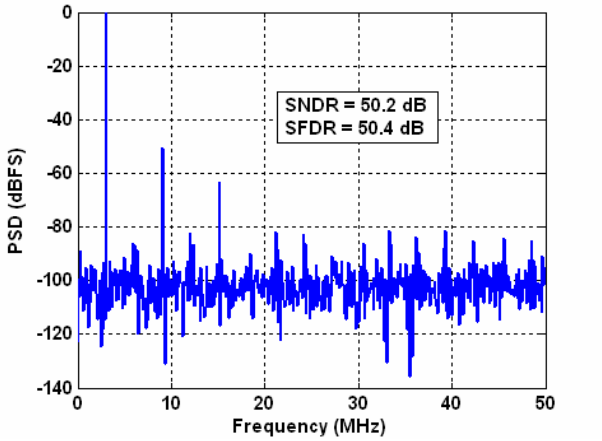


**Fig. 8:** Output spectrum of a SC gain-stage using the circuit level simulation.

In Fig. 9 the output spectrum of the conventional second-order single-bit sigma-delta modulator using the proposed models to estimate the effect of amplifier's dc gain nonlinearity is shown. Figure 10 shows the output spectrum of the same second-order sigma-delta modulator obtained from the circuit level simulations. As is seen, the proposed model results in only about 2 dB less estimation in both SNDR and SFDR.

## V. Conclusions

In this paper, a simple yet accurate model for dc gain nonlinearity of MOS amplifiers used in switched-capacitor circuits was proposed and its effect in both SC gain-stages and integrators was modeled. The proposed model can efficiently be used in the system level simulations of pipelined and sigma-delta A/D converters in order to account into the effect of dc gain nonlinearity of amplifiers on the overall performance without performing the time consuming circuit level simulations.

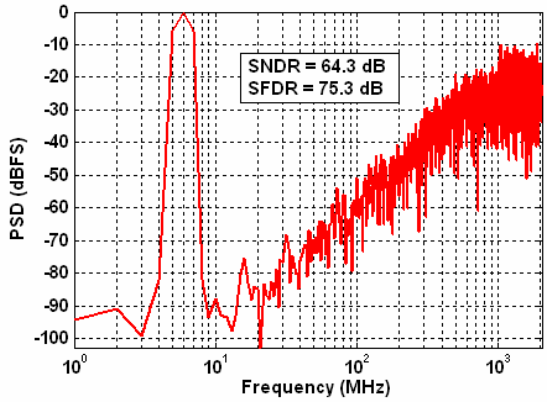


**Fig. 9:** Output spectrum of a second-order ΣΔ modulator using the proposed model.

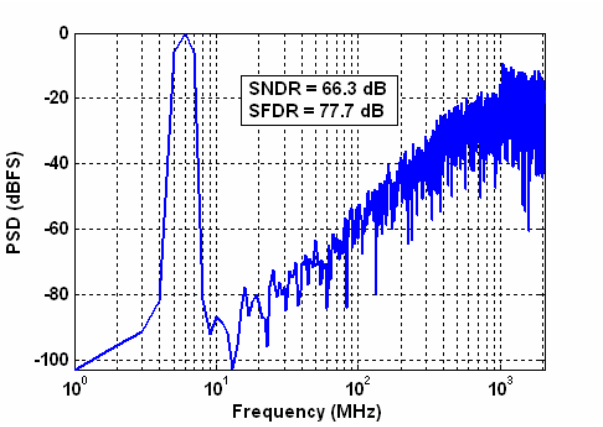


**Fig. 10:** Output spectrum of a second-order ΣΔ modulator using the circuit level simulation.

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