Systematic and Optimal Design of CMOS Two-Stage Opamps with Hybrid Cascode Compensation

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Abstract

This paper presents a systematic and optimal design of hybrid cascode compensation method which is used in fully differential two-stage CMOS operational transconductance amplifiers (OTAs). The closed loop analysis results are given to obtain a design procedure. A simple design procedure for the minimum settling time of the hybrid cascode compensation technique for a two-stage class A/AB amplifier is proposed. Optimal design issues of power dissipation are considered to achieve the lowest power consumption for the required settling time. Finally, a design example is presented to show both the usefulness of the hybrid cascode compensation and the proposed design procedure. The proposed design technique can help circuit designers as well as it can be used in computer aided circuit design tools.

1. Introduction

Several frequency compensation techniques such as Miller and cascode compensations are used to design the stable two-stage opamps [1, 2]. The main drawbacks of Miller compensation scheme are the low speed and low power supply rejection ratio (PSRR) compared to the cascode compensation. Cascode compensation scheme achieves higher speed and higher PSRR compared to Miller compensation at the cost of complex design and analysis procedure [2, 3].

A novel cascode compensation scheme called ***hybrid cascode compensation*** has been introduced in [4, 5] by the authors. In this method, two distinct capacitors are used between two low-impedance nodes of the first stage and the output node. In turn, this compensation technique merges Ahuja [2] and improved Ahuja style [6] compensation methods. This scheme of compensation yields a higher amplifier bandwidth compared to the standard Miller and conventional cascode compensation techniques at the cost of more complex design procedure for the settling behavior of the amplifier. This technique also offers all advantages of the cascode compensation technique such as high PSRR, etc.

In [4, 5] a closed loop analysis of the hybrid cascode compensation has been introduced and also a closed loop design procedure has been proposed. In order to get more insight in the design of this compensation scheme and also show its usefulness further, its open loop signal transfer function has been obtained in [7] to accurately estimate its poles and zeros. However, in [4, 5] a fourth order system has been analyzed to obtain a design procedure making the design more complicated and need solving a set of equations by numerical equations solving tools. As shown in [7] considering several good approximations result in the system order to be reduced to three making the closed loop design more relaxed as will be presented here. This paper uses the open loop analysis results of [7] to achieve a simple systematic design procedure for two-stage opamps with hybrid cascode compensation making their design very straightforward. Optimal design issues of power dissipation are also considered in the proposed design procedure here.

The paper is organized as follows. Section 2 presents the closed loop analysis of a two-stage opamp employing the hybrid cascode compensation method. In Sect. 3 an optimal design procedure is presented to achieve a minimum settling time considering the power optimization. Section 4 gives the simulation results in the context of a design example. Conclusions are given in section 5.

2. Closed Loop Analysis

Figure 1 shows a two-stage class A/AB OTA composed of a folded-cascode as the first stage and the class AB amplifier with active current mirrors as the second stage that employs the hybrid cascode compensation technique [4, 5]. It is worth mentioning that the compensation method can easily be applied to the other two-stage OTAs. As shown in Fig. 1 two separate capacitors, C_a and C_s, have been used for compensation of the opamp where C_a is used in a signal path and C_s in a non-signal path. The second stage is a class AB amplifier with active current mirrors similar to [8].

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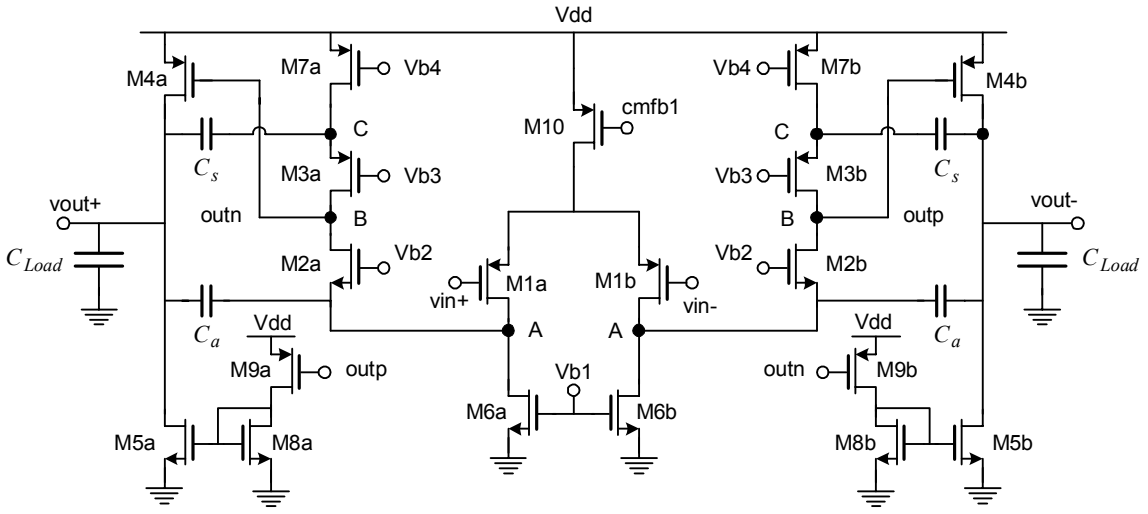

Fig. 1: A two-stage class A/AB OTA with hybrid cascode compensation.

It can readily be shown that using the similar approach presented in [7] to calculate the open loop loops and zeros of a two-stage class A amplifier with hybrid cascode compensation the closed loop signal transfer function of the opamp shown in Fig. 1 with considering $g_{m2} = g_{m3}$ and $C_a = C_s$ is obtained as follows:

$$A_v(s) = \frac{v_{out}}{v_{in}} = \frac{g_{m1}\left(g_{m2}\,(g_{m4}+ g_{m5}) - s^2 C_a\, C_B\right)}{s^3\, d_3 + s^2\, d_2 + s\, d_1 + d_0} \qquad (1)$$

where

$$d_3 \approx C_B\, C_a\, C_L$$

$$d_2 \approx C_B\, g_{m2}(C_a + C_s + C_L) - f\, g_{m1} C_B\, C_a$$

$$d_1 \approx (g_{m4}+ g_{m5})\,(g_{m2}\, C_a + g_{m3}\, C_s)$$

$$d_0 \approx f\, g_{m1}\, g_{m2}\,(g_{m4} + g_{m5})$$

$$C_B = C_{db2} + C_{db3} + C_{gs4} + C_{gd2} + C_{gd3} + C_{gs9}$$

$$C_L = C_{Load} + C_{db4} + C_{db5}$$

and f is the feedback factor in a closed loop configuration. In these calculations, it was assumed that the parasitic capacitances of the nodes A, B, and C are much smaller than the compensation capacitors C_a, C_s and the load capacitance C_L. It was also assumed that the transconductance of transistors, g_{mi}, is much greater than the conductances seen at the nodes A, B, C, and output and the mirror pole and zero are greater than the other non-dominant poles and zeros. This can be achieved by properly choosing the bias current of the active current mirrors. It was also assumed that the transconductance of transistors M8 and M9 to be equal.

3. Design Procedure

3.1 Settling of a Standard 3rd Order System

As shown in the previous section and also in [7], the $g_{m2} = g_{m3}$ and $C_a = C_s$ assumption reduces the order of the open loop and closed loop system transfer functions to three. So, in order to investigate the settling behavior of the hybrid cascode compensation technique, a standard third order system with the following transfer function is considered:

$$H(s) = \frac{k(\gamma^2\zeta^2\omega_n^2 - s^2)}{(s+\alpha\zeta\omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \qquad (2)$$

As it is seen, there are four system parameters, α, γ, ω_n, and ζ in the transfer function. ω_n and ζ are called the natural frequency and damping factor, respectively.

The settling error in definite time period of t_{ss} as defined $\varepsilon_s = \frac{s(\infty) - s(t_{ss})}{s(\infty)}$ is obtained by:

$$\varepsilon_s = \frac{1}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)} \times e^{-\alpha\zeta\omega_n t_{ss}}$$
$$+ \frac{\alpha\zeta\, e^{-\zeta\omega_n t_{ss}}}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)}\left(-2\zeta+\alpha\zeta\right)\cos(\omega_n t_{ss}\sqrt{1-\zeta^2}) \qquad (3)$$
$$+ \frac{\alpha\zeta\, e^{-\zeta\omega_n t_{ss}}}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)} \frac{(1-2\zeta^2+\alpha\zeta^2)}{\sqrt{1-\zeta^2}} \sin(\omega_n t_{ss}\sqrt{1-\zeta^2})$$

where $s(t)$ is the step response. In the calculation of the step response, it was assumed that γ goes to infinity since in the practical cases the right and left-plane zero pair in the closed loop transfer function are at much higher

frequencies than the other poles and zeros. However, this equation is very complex to intuitively explain how to choose the system parameters to optimize the settling behavior. Therefore, numerical calculations are used. Figure 2 shows the settling error for different values of the system parameters. For example, the obtained system parameters for a –80 dB settling error are $\alpha = 1$, $\zeta = 0.9$, and $\omega_n t_{ss} = 11$.

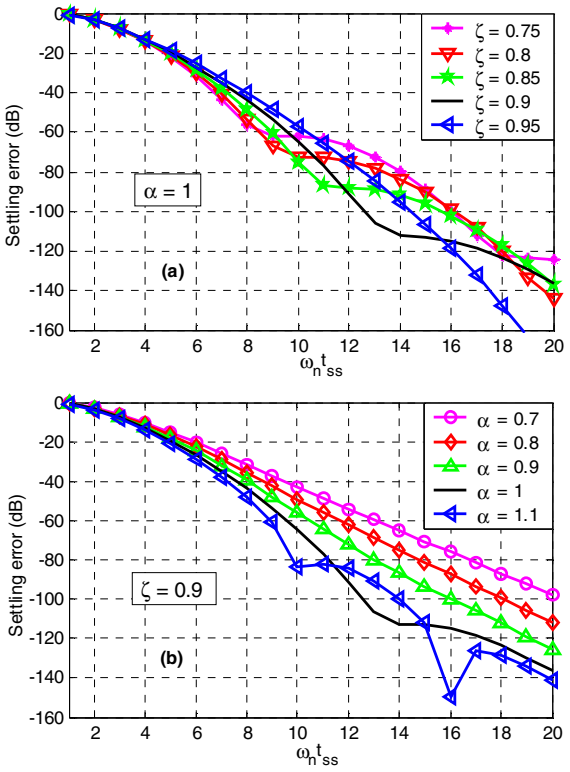

Fig. 2: Settling error as a function of $\omega_n t_{ss}$ for different values of (a) ζ, and (b) α.

3.2 Small Signal Settling

Using the obtained system parameters for a specific settling error in a defined time and the opamp closed loop transfer function given in (1), the device parameters can be determined with the following equations:

$$(2+\alpha)\,\zeta\,\omega_n = \frac{g_{m2}(C_L + C_a + C_s) - f\,g_{m1}C_a}{C_a C_L} \tag{4}$$

$$\left(1+2\alpha\zeta^2\right)\omega_n^2 = \frac{(g_{m2}+g_{m3})(g_{m4}+g_{m5})}{C_B C_L} \tag{5}$$

$$\alpha\zeta\,\omega_n^3 = \frac{f\,g_{m1}\,g_{m2}\,(g_{m4}+g_{m5})}{C_B\,C_a\,C_L} \tag{6}$$

In these equations, two of system parameters, α and ζ, are known. The value of ω_n is not known. However the value of $\omega_n t_{ss}$ is known. The optimal value of linear settling time, t_{ss}, is obtained in the next subsections to determine the ω_n efficiently.

3.3 Calculation of the Compensation and Load Capacitors

The load and compensation capacitors, C_L, C_a, and C_s are determined due to the circuit noise considerations. It can be shown using the similar approach introduced in [9], the total output thermal noise power of the opamp shown in Fig. 1 with the hybrid cascode compensation in a closed loop configuration assuming $g_{m2} = g_{m3}$ and $C_a = C_s$ with a feedback factor of f is as follows:

$$S_{N,out} = \frac{2kT}{3f(C_a+C_s)}\left(1+\frac{g_{m6}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right) \times\left(\frac{(2+\alpha)(1+2\alpha\zeta^2)}{1+2\alpha\zeta^2+\alpha^2\zeta^2}\right) \tag{7}$$

As it is seen from the above relation, the sum of the compensation capacitors, i.e. C_a and C_s, is obtained in such a way to achieve the required noise budget. The load capacitor is determined by the other capacitances of the switched-capacitor circuit that employs the opamp and also its circuit structure. It is worth mentioning that the value of the capacitances of switched-capacitor circuits is determined by the kT/C noise of the switches, matching of the elements, etc.

3.4 Optimization of the Bias Currents

The total settling time of an opamp consists of two distinct regions [1]. In the first region, the opamp slews since when the input signal is large, one of the input transistors may turn off. The second region of settling is the linear settling where in this region the small signal parameters of the opamp can be used to describe its settling behavior as employed in the previous section. The large signal settling behavior of an opamp is described by a quantity called the slew rate and its relation for the circuit shown in Fig. 1 is as follows:

$$SR = \frac{2I_{DS1}}{C_a+C_s} \tag{8}$$

where the bias current of both input stage and cascode transistors are assumed equal. To optimize the bias currents of the opamp and hence to reduce its power dissipation, the current of the input transistors, M1, is chosen equal with the values obtained from the slewing relation [10], i.e.:

$$I_{DS1} = \frac{1}{2}(C_a+C_s)SR = \frac{1}{2}(C_a+C_s)\frac{V_{FS}}{t_{ls}} = \frac{1}{2}g_{m1}V_{eff1} \tag{9}$$

$$t_s = t_{ls} + t_{ss} \tag{10}$$

where V_{FS} is the differential output signal step and t_{ls} and t_{ss} are the large and small signal settling times, respectively.

The transconductance of the input transistors can be obtained using the equations (4-6) as follows:

$$g_{m1} = \frac{2C_a}{f} \frac{\alpha\zeta\omega_n t_{ss}}{1+2\alpha\zeta^2} \frac{1}{t_{ss}} \quad (11)$$

So, the optimal bias current of the input transistors and also the optimal linear settling time are obtained as follows:

$$I_{DS1,\,opt} = \frac{1}{2t_s}(C_a+C_s)\left(V_{FS} + \frac{1}{f}\frac{\alpha\zeta\omega_n t_{ss}}{1+2\alpha\zeta^2} V_{eff1}\right) \quad (12)$$

$$t_{ss} = \frac{\alpha\zeta\omega_n t_{ss} V_{eff1}}{f V_{FS}(1+2\alpha\zeta^2) + \alpha\zeta\omega_n t_{ss} V_{eff1}}\, t_s \quad (13)$$

The optimal bias current of the output transistors is determined using the following relation:

$$I_{DS4,\,opt} = \frac{1}{2} g_{m4} V_{eff4} \quad (14)$$

where the value of V_{eff4} is obtained from the required output signal swing. g_{m4} is determined by solving the small signal equations of (4-6). The value of $\omega_n t_{ss}$ is obtained from Fig. 2 for a specific settling error and the value of t_{ss} is derived from relation (13). So, the optimal value of ω_n is also obtained.

3.5 Solving the Small Signal Equations

The small signal equations of (4-6) can be solved to determine the transconductance of the critical devices, i.e. M1, M2, M3, M4, and M5. However, since the value of C_B is unknown before the circuit is designed, so to solve these equations a suitable value for C_B is considered firstly. Considering C_B is known, the device transconductances will be obtained by solving the equations (4-6) as follows:

$$g_{m1} = \frac{2C_a}{f} \frac{\alpha\zeta\omega_n}{1+2\alpha\zeta^2} \quad (15)$$

$$g_{m2} = C_a\zeta\omega_n \frac{C_L(2+\alpha)(1+2\alpha\zeta^2)+2C_a\alpha}{(1+2\alpha\zeta^2)(C_a+C_s+C_L)} \quad (16)$$

$$(g_{m4}+g_{m5}) = \frac{(C_a+C_s+C_L)}{2} \times \frac{C_B C_L \omega_n (1+2\alpha\zeta^2)^2}{(2+\alpha)(1+2\alpha\zeta^2)\zeta C_a C_L + 2C_a^2\alpha\zeta} \quad (17)$$

After obtaining the transconductance value of the critical transistors and the value of bias currents, the transistors dimensions are determined. Then, circuit level simulators can be used to derive the opamp's specifications. At the circuit level simulations, the value of C_B is determined. The transconductance of critical transistors are derived accurately using the above-mentioned relations again. This procedure can be repeated for a few times to accurately include the effect of C_B in the relations (15-17). At the last step of design a few circuit level iterations are also performed to refine the transistors' dimensions.

The design procedure proposed in this paper is summarized as follows:

1. Derive the system parameters for a required settling accuracy from Fig. 2.
2. Estimate the value of the compensation capacitors from the relation (7) to achieve the required output noise voltage. Assume a suitable initial value for the first stage output node parasitic capacitance, C_B. The value of C_L is obtained from the circuit structure that employs the opamp.
3. Calculate the bias currents and linear settling time from the relations (12-14) for the required output signal swing.
4. Calculate the transconductance value of the critical transistors, i.e. M1, M2, M3, M4, and M5, from the relations (15-17).
5. Size all of the transistors and run circuit level simulations to obtain the required specifications and also the value of the first stage output node parasitic capacitance, C_B. If the value of C_B is different from its initial value, repeat the design procedure from step 4. Calculate the output noise power using the circuit level simulator and adjust the compensation capacitors and go to step 3 if the output noise power is less or greater than the required value.
6. Check the other circuit requirements and perform a few iterations at the circuit level simulations to refine the transistors' dimensions if the required design specifications are not satisfied.

4. Design Example

4.1 Design Parameters and Calculations

To verify the usefulness of the proposed design procedure for the hybrid cascode compensation an OTA with the structure shown in Fig. 1 was designed and simulated using a 0.18-µm BSIM3v3 level 49 mixed-signal CMOS models with HSPICE. The design is targeted for realization of a fully differential switched-capacitor

integrator to be used in a sigma-delta modulator with the specifications shown in Table 1.

The value of the sampling capacitor is determined by the kT/C noise budget. Its value is considered to be 5-pF resulting in the SNR due to the kT/C noise of the switches to be more than 94-dB. The value of integrating capacitor is considered as 10-pF to achieve a gain of 0.5.

Table 1: Design parameters

Parameter	Value
Settling accuracy	15-bit
Sampling frequency	40-MHz
Maximum output signal swing	1.5-$V_{PP,\ differential}$
SNDR	90-dB
Gain (C_1/C_2)	0.5
DC gain	70-dB
Oversampling ratio	8
Maximum differential output signal step (V_{FS})	0.5-V
Power supply voltage (V_{DD})	1.5-V
Technology	0.18-µm CMOS

To get 15-bit accuracy, i.e. 0.002% or -94-dB settling error, the system parameters are obtained using Fig. 2 as $\alpha = 1$, $\zeta = 0.9$, and $\omega_n t_{ss} = 12.5$. The compensation capacitors is chosen 1.5-pF resulting in the SNR due to the opamp's thermal noise to be more than 95-dB. The value of the load capacitance, C_L, is obtained 8-pF considering the integrator loading, parasitic and bottom plate capacitances.

To satisfy the required output signal swing with sufficient linearity the effective overdrive voltage of M4 and M5 is considered 0.2V. The effective voltage of the input transistors was also considered 0.2V to achieve the required linearity. The value of C_B is estimated to be 0.3-pF, firstly. Table 2 shows the derived system parameters using the proposed design equations and also their simulated values in the final design.

Table 2: Calculated and simulated device sizes

Parameter	Calculated Value		Simulated Value	
	(W/L)	g_m (mA/V)	(W/L)	g_m (mA/V)
M1a, M1b	171	2.73	32/0.18	2.73
M2a, M2b	216	5.32	40/0.18	4.51
M3a, M3b	647	5.32	120/0.18	4.11
M4a, M4b	72	1.17	33/0.18	3.13
M5a, M5b	24	1.17	12/0.18	3.65
M6a, M6b	50	3.64	15/0.3	3.70
M7a, M7b	76	1.82	20/0.25	1.51
M8a, M8b	8	0.39	4/0.18	1.14
M9a, M9b	24	0.39	11/0.18	1.05
M10	341	5.46	60/0.18	5.19

The bias current of the input and output stages were obtained 0.27mA and 0.12mA, respectively. At the circuit level simulations only the bias current of the output stage was increased (about 3 times) mainly in order to move the mirror pole and zero of active current mirrors to a higher frequency. The other circuit parameters have not been changed considerably. The bias current of active current mirrors was set to one third of the output transistors.

4.2 Simulation Results

The designed opamp was simulated with HSPICE with the device parameters shown in Table 2. The common mode input voltage was 0.2V. The body terminal of all NMOS and PMOS transistors were connected to the V_{SS} and V_{DD}, respectively. Table 3 shows the simulated and calculated open loop poles and zeros of the hybrid cascode compensation. In these calculations, the circuit parameters extracted from HSPICE simulations and shown in Table 4 were used in the relations presented in [7]. These simulations further indicate that the assumptions used to reduce the system order to three have the sufficient accuracy. Figures 3 and 4 show the open loop frequency response and settling performance of all three cascode compensation schemes, respectively. A summary of the simulation results is shown in Table 5.

Table 3: Simulated and calculated poles and zeros values

Parameter	Simulation	Calculation
f_{p1} (kHz)	21.73	19.96
f_{p2} (MHz)	536.1	456.3
$f_{p3,\ 4}$ (MHz)	827.1	835.6
f_{z1} (MHz)	498.6	436.1
$f_{z2,\ 3}$ (MHz)	1275.4	1395.6

Table 4: Device sizes and circuit parameters

Parameter	Value
R_A	2.85 kΩ
R_B	88.67 kΩ
R_C	2.77 kΩ
R_L	4.42 kΩ
C_A	0.132pF
C_B	0.265pF
C_C	0.282pF
C_L	8pF
C_a, C_s	1.5pF

In these simulations, equal values for the transistors' dimensions and bias currents have been used except the input transistor sizes of the conventional cascode compensation have been designed to get the same phase margin for both hybrid and conventional cascode compensation circuits and also the input and non-signal path cascode transistors of the improved cascode compensation have been sized to achieve a better settling performance.

Simulation results show that the hybrid cascode compensation scheme achieves a unity-gain bandwidth greater than that of the conventional cascode

compensation which results in smaller settling time as shown in Fig. 4. Simulation results of the improved cascode compensation show that its zero is so close to the unity-gain bandwidth which results in a large phase margin and so degraded settling behavior. To improve its settling performance the dimensions of its input and non-signal path cascode transistors, M1 and M3, have been sized about 0.65 and two times of those of the hybrid cascode compensation method, respectively. The hybrid cascode compensation also achieves about 1-dB DC gain greater than the conventional and improved cascode compensations. The slew rate and input referred thermal noise of all three cascode compensation schemes are approximately the same.

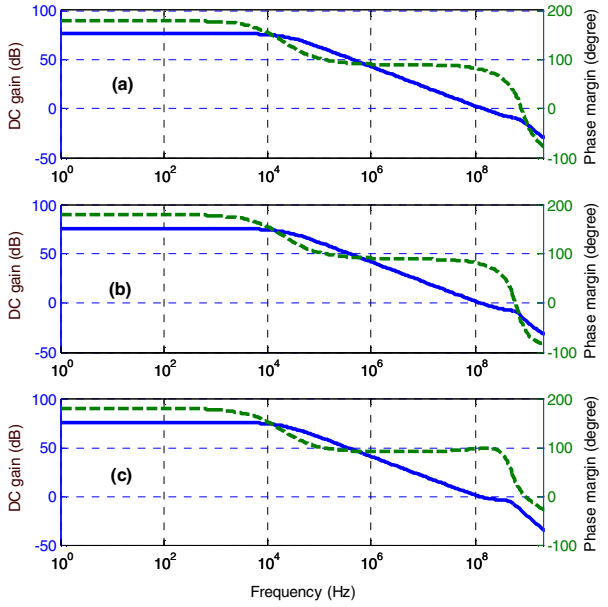

Fig. 3: Frequency response simulation results: (a) hybrid, (b) conventional and (c) improved cascode compensation methods.

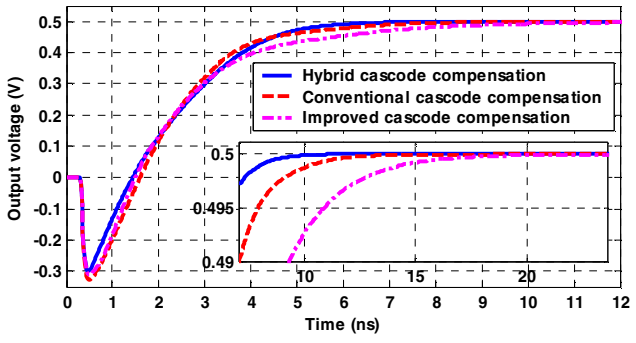

Fig. 4: Settling simulation results.

Table 5: Simulation results summary

Parameter	Hybrid Cascode	Conventional Cascode	Improved Cascode
Unity-gain bandwidth	145.1 MHz	126.7 MHz	120.1 MHz
Phase margin	78.9 °	79.0 °	97.5 °
DC gain	76.2 dB	75.1 dB	75.0 dB
0.002% settling time	11.2 ns	15.7 ns	23.1 ns
Power dissipation	3.64 mW	3.64 mW	3.64 mW

5. Conclusions

In this paper, a systematic design procedure for the hybrid cascode compensation method was presented. The only drawback of the hybrid cascode compensation was its complex design procedure for a required settling accuracy. In order to reduce its design time and also achieve an efficient power optimized design, the transconductance of the critical transistors and the bias currents are selected optimally. The proposed design method can also be extended for other cascode compensation methods efficiently.

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