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A Histogram-Based Digital Background Calibration Technique for Pipelined A/D Converters

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***Abstract*—This paper presents a digital background calibration technique for pipelined analog-to-digital converters (ADCs) to correct the gain error due to the capacitors mismatch and finite dc gain and nonlinearity error owing to the residue amplifiers. The proposed calibration scheme corrects these errors by using the histogram-based method. To calculate the linear and nonlinear coefficients, the threshold level of sub-ADC is changed and based on specifications of residue characteristic and output histogram, the first and third order coefficients are extracted. This method does not require any calibration signal or additional analog hardware and relaxes the performance requirements of the analog building circuits. Circuit level simulation results of a 12-bit 100 MS/s pipelined ADC in a 65 nm CMOS technology show that the proposed calibration scheme improves signal-to-noise and distortion (SNDR) and spurious free dynamic range (SFDR) from 30.4 dB and 31.8 dB to 69.3 dB and 81.2 dB, respectively.**

Keywords*—Capacitors mismatch, histogram-based digital background calibration, gain error, gain nonlinearity, pipelined analog-to-digital converters (ADCs).

I. Introduction

The scaling of CMOS technology affects the performance of analog circuits resulting in reduced voltage gain and output swing in op-amps which are employed in residue gain stage of pipelined analog-to-digital converters (ADCs) [1]. So, various digital calibration methods have been extensively utilized in order to lie down the characteristics of the required analog circuits [2-22]. Moreover, the non-idealities of the analog construction blocks are corrected to enhance the efficiency of high resolution pipelined ADCs.

Digital background calibration methods can be categorized into foreground and background schemes. A foreground calibration technique interrupts the data conversion operation while digital background techniques work in the background without any interruption in the ADC normal operation. Therefore, digital background calibration methods are suitable for many applications. The digital background calibration techniques consist of two estimation and correction phases and the estimation phase is the most important part in the calibration process.

In equalization-based methods like [3, 5], the errors are extracted by converting the calibration signal and the skipped input samples are estimated by using a prediction filter. In [4], a pseudorandom noise (PN) sequence is employed in correlation-based techniques to modulate the analog errors. Next, the modulated information is extracted in digital domain to reach the essential performance. In these techniques, after a long time of convergence, the input signal exposes like an uncorrelated noise with amplitude larger than the PN sequence. These ways are faster than others, but they require extra analog circuits to construct high accuracy calibration signals. Histogram-based calibration methods rectify the errors by calculating the output code density of the ADC [7, 12, 13, 15]. This method extremely relies on the input signal statistics. In [12], two-residual and histogram-based technique are used for correcting the linear errors. In [4], the error terms is estimated by measuring the width of histogram block. In [13], after measuring the output code of decision points, they are adjusted by mapping the output histogram to estimate and refine the first and third order errors in pipelined ADCs. In [12], the output histogram is considered and moved by injecting a PN signal and then it is compare with first mode to extract the error coefficients. In [2], the histogram of output is measured and it used to estimate the gap around decision points for correcting the linear error. In [7], a sliding histogram is moving on and sweeps all the output codes for error estimation.

This paper proposes a histogram-based digital background calibration which corrects both linear and nonlinear errors by using changing-threshold technique and characteristics of the residue curve. This is a quite digital method and insensitive to the comparator offset. In this calibration scheme, the structure of the digital approximation block is very simple.

The remains of the paper is arranged as follows. Section II presents the effect of inter-stage gain and nonlinearity errors. The proposed calibration methods is explained in Section III. The results of simulations are shown in Section IV, and at last, the conclusion is reported in Section V.

II. Pipelined ADC Architecture and Error Modeling

The overall block diagram of pipelined ADCs consists of numerous low-resolution stages for producing the digital output, D_{out}, where the last stage is generally a flash ADC. There are a sub-ADC and a multiplying digital-to-analog converter (MDAC) in each stage that is the main block of these stages. The capacitor flip-around (CFA) and capacitor non-flip-around (CNFA) are two common structures to realize an MDAC [3, 5]. The CFA MDACs have faster settling but need more calibration coefficients in comparison with the CNFA structure. So, the CNFA structure is mostly utilized in digital background calibrated pipelined ADCs owing to the reduced coefficients in the calibration process [3, 5].

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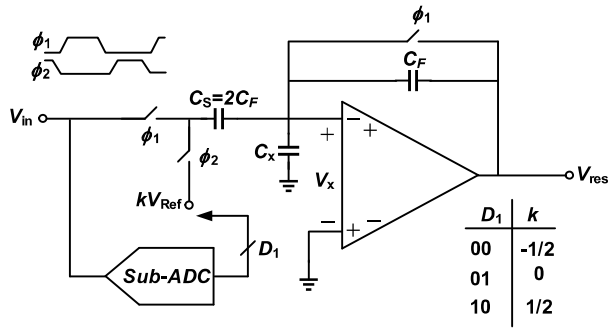

Fig. 1: 1.5-bit/stage non-flip-around MDAC.

A 1.5-bit/stage non-flip-around MDAC is represented in Fig. 1. In order to estimate the error coefficients, the behaviour of a non-flip-around MDAC is modelled here. According to Fig. 1, a third-order polynomial as below estimates the open-loop input-output static characteristics of a fully-differential amplifier in each stage.

$$V_{res} = \alpha_1 V_x + \alpha_3 V_x^3 \tag{1}$$

where α_1 and α_3 are the amplifier gain and gain nonlinearity factors, respectively. By placing it in a close-loop configuration, we can neglect higher order nonlinearity terms, the reverse of (1) can be estimated by another third-order polynomial as

$$V_x = \rho_1 V_{res} + \rho_3 V_{res}^3 \tag{2}$$

$$\rho_1 = 1/\alpha_1,\ \rho_3 = -\alpha_3/\alpha_1^4 \tag{3}$$

The input-output transfer function of the non-flip-around MDAC exhibited in Fig. 1 is obtained by

$$V_{in} = kV_{\mathrm{Ref}} + \gamma(1-\rho_1)V_{res} + \gamma\rho_3 V_{res}^3 \tag{4}$$

where

$$\gamma = \left(1 - \frac{C_X + C_F}{C_S}\right) \tag{5}$$

In order to simplify equation (4), it is denoted as

$$V_{in} - kV_{\mathrm{Re}f} = \eta_1 V_{out} + \eta_3 V_{out}^3 \tag{6}$$

where the amplifier gain and gain nonlinearity reverse coefficients are expressed as η_1 and η_3, respectively. In equation (6), the effects of amplifier linear and nonlinear errors, capacitor mismatch and parasitic capacitor in a 1.5-bit CNFA MDAC are considered. Equation (6) is the reverse function of an MDAC, so if η_1 and η_3 are extracted accurately, the MDAC non-idealities will be cancelled. The MDAC model based on the inverse of equation (6) is as follows

$$V_{res} = \beta_1\left(V_{in} - kV_{\mathrm{Re}f}\right) + \beta_3\left(V_{in} - kV_{\mathrm{Re}f}\right)^3 \tag{7}$$

where β_1 and β_3 are first and third order coefficients of MDAC, respectively. Fig. 2 shows a stage and its calibration model. A 1.5-bit/stage includes a 1.5-bit sub-ADC and MDAC block that consist of 1.5-bit sub-DAC and amplifier. Backend-ADC includes the rest of the stages and it is considered ideal because the calibration procedure begins from the last stage. Non-idealities are mostly related to the amplifier. Therefore, the error coefficients are estimated based on its input-output function. The inverse function is

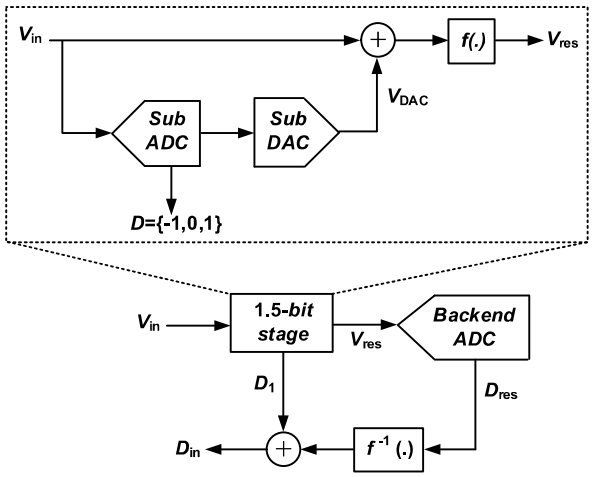

Fig. 2: A pipelined ADC stage and its calibration.

used for calibrating the errors. In the calibration process, the estimation of errors is the most important part and their compensation is easily possible by applying the inverse function.

III. Proposed Calibration Technique

As represented in Fig. 3, the residue characteristic is distributed to three sections based on the output code of the sub-ADC with first and third order errors. The slope of the lines is the same in all regions. This slope represents the first-order coefficient, which is ideally equal to 2.

The slope of each line is possible with two-point coordinates, so the gain error coefficient can be calculated in this way. But obtaining the coordinates of the points has several challenges as follows.

1) The values on the input axis are not fixed and only the decision points are known, but these points also change due to comparators offset effect. By using the back-end ADC, we can calculate the output peculiarities of decision points.
2) The accuracy of calibration coefficients is related to the back-end ADC resolution straightly. Besides, the position of decision points must be truly specified to achieve the correct value of output.

The last issue is solvable because the calibration procedure is begun from the last stage and comes into the first stage. So the output of the backend ADC is firstly corrected although there is a direct relationship between the residual output and the backend ADC accuracy. In order to alleviate these issues, the proposed solutions are illustrated in the following sub-sections.

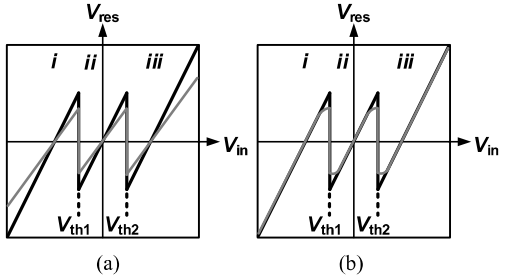

Fig. 3: Residue specification with (a) gain and (b) nonlinearity error.

A. Shift the Decision Points

In order to calculate the gain error coefficient, the decision points are moved to extract more information of the residue characteristic. In spite of common methods like [9], we want to have a symmetric residue characteristic. Fig. 4 presents the method for changing decision points with *S*. The input signal is compared with $\pm V_{Ref}/8$ and $\pm V_{Ref}/4$, respectively. By increasing the difference between the threshold voltages, the estimation accuracy is improved [10].

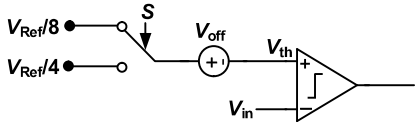

Fig. 4: Notion of the shift in the decision point.

B. Mapping Histogram Algorithm

This technique has been firstly presented in [11]. An ideal ADC included, a uniform histogram surrounded the decision points. However, in the presence of linear and nonlinear errors, the histogram is not uniform. With this technique, a short histogram is organized around the decision points and we can extract the minimum and maximum codes around the decision points. This technique can also remove noisy codes from the histogram by considering its density. Therefore, the codes that have the least number of repetitions are noisy codes. Noisy components have detrimental effect in the estimation of minimum and maximum codes in each region [2]. So, the detection and elimination of noisy codes is important for calibration accuracy.

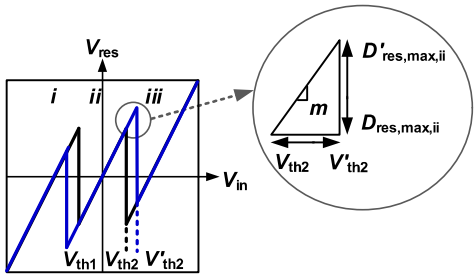

Fig. 5: Coefficient extraction technique.

C. Coefficients Extraction

As shown in Fig. 5, to obtain the first order coefficient, we use the vertical triangle relationships in the second region as

$$m = \frac{D'_{out,\max,ii} - D_{out,\max,ii}}{(V'_{th2} + V_{os2}) - (V_{th2} - V_{os2})} \tag{8}$$

$$\beta_1 = m = \frac{D'_{out,\max,ii} - D_{out,\max,ii}}{V'_{th2} - V_{th2}} \tag{9}$$

where $D_{out,max,ii}$ and $D'_{out,max,ii}$ are the maximum code in region 2 for V_{th1} and V_{th2}, respectively. Fig. 6 shows the regions according to equation (9). The linear coefficient is obtained without affecting by comparator offset since there is one only comparator. So according to equation (9), they

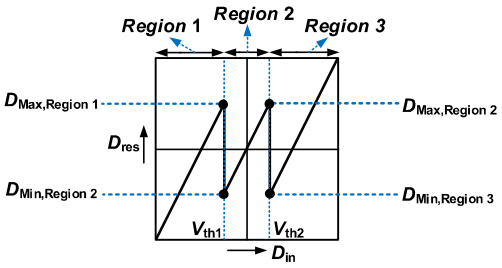

Fig. 6: Output peculiarities of decision points in each region.

cancel each other. Now we need to determine the mechanism for extracting the third-order coefficient.

As we know, the impact of the nonlinearity is ignorable when the input signal is small. When the voltage threshold is $V_{Ref}/8$, the input-output relationship is given by:

$$V_{out} = \beta_1 V_{in} \tag{10}$$

However, when the nonlinearity error is assumed, the input-output equation is as follows.

$$V'_{out} = \beta_1 V_{in} + \beta_3 V_{in}^3 \tag{11}$$

The digital equivalents for equations (10) and (11) are as:

$$D_{out,\max,ii} = \beta_1 (D_{in} - D_1) \tag{12}$$

$$D'_{out,\max,ii} = \beta_1 (D_{in} - D_1) + \beta_3 (D_{in} - D_1)^3 \tag{13}$$

By subtracting the relationship (12) and (13), the nonlinear coefficient is obtained as follows.

$$\Delta D = -\beta_3 (D_{in} - D_1)^3 \tag{14}$$

$$\beta_3 = -\frac{\Delta D}{(D_{in} - D_1)^3} = -\frac{\Delta D}{(D_{res,\max,ii} / \beta_1)^3} \tag{15}$$

Thus, the first and third order error coefficients are obtained.

D. Calibration Procedure

This method includes changing decision points and histogram-based method to calibrate pipelined ADCs. The calibration of each stage consists of two phases. Firstly, the decision points are changed, and then, by using the output histogram and residue characteristic, the linear and nonlinear coefficients are extracted. This technique does not disrupt the ADC normal action. The necessary digital hardware is decreased because the number of equations and calibration phases is minimum.

IV. Simulation Results

System and circuit level simulation results which are performed in MATLAB and Cadence softwares, respectively, are provided to measure the effectiveness of the proposed calibration method. In system level simulations, ten 1.5-bit stages and a 2-bit flash ADC as the last stage are considered to achieve a 12-bit 100 MS/s pipelined ADC. The calibration process is only performed in the first three stages and the 9-bit back-end ADC is assumed to be ideal. The calibration process starts from the third stage, and then, it is performed in the first stage. In these simulations, some

conditions are considered as follow. Comparator offset with $3\sigma = 25$ mV is assumed. DC gain of amplifier is 30 dB and $\beta_3 = -0.006$ V^{-2} is considered to realize the capacitive MDACs. The error coefficients are extracted from the circuit level simulations and then they are also utilized in system level simulations.

In the circuit level simulations, the amplifier presented in [3] has been utilized to realize the CNFA MDACs. This is a two-stage OTA with Miller compensation. The simulated OTA has about 30 dB open-loop gain, 2.06 GHz unity-gain frequency, and 69 degree phase margin. The dynamic latch comparator utilized in [18] with 25 mV offset and 100 ps regeneration time is also used here.

We use a full-scale sine wave as input and Fig. 7 and Fig. 8 show the spectrum of output simulated ADC in system level and circuit level simulations, respectively. Before the system level calibration, the spurious free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are about 33.8 dB and 33.2 dB, respectively. They are enhanced to 80.6 dB and 63.8 dB after employing the suggested calibration method. In circuit level simulations, the SFDR and SNDR values are enhanced from 31.8 dB and 30.2 dB to 81.2 dB and 69.3 dB, respectively. Fig. 9 represents the circuit level simulated SFDR and SNDR values according to the input signal frequency. The resolution of the suggested algorithm does not depend on the input wave frequency.

The offered calibration technique is contrasted with some methods in Table I. In brief, the hardware complexity is decreased in each phase of the offered calibration method due to the reduced calculation and one estimation block has been used instead of using separate blocks for each stages. This method also does not requirement any extra analog circuit so is more profited for CMOS procedure scaling.

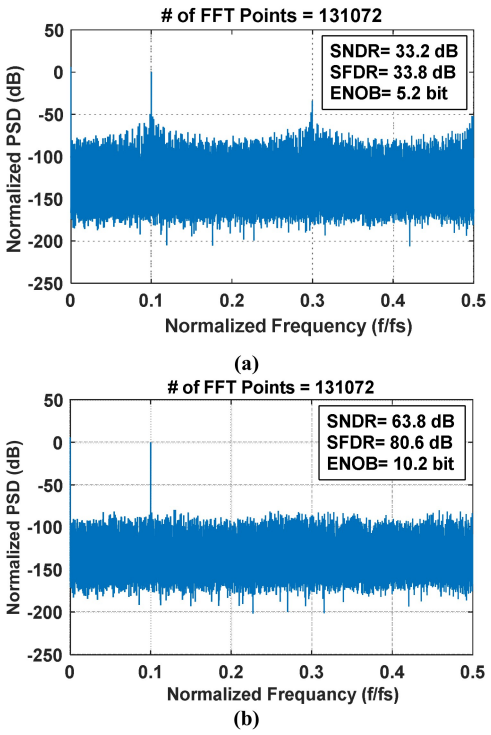

Fig. 7: System level simulations (a) before and (b) after the calibration.

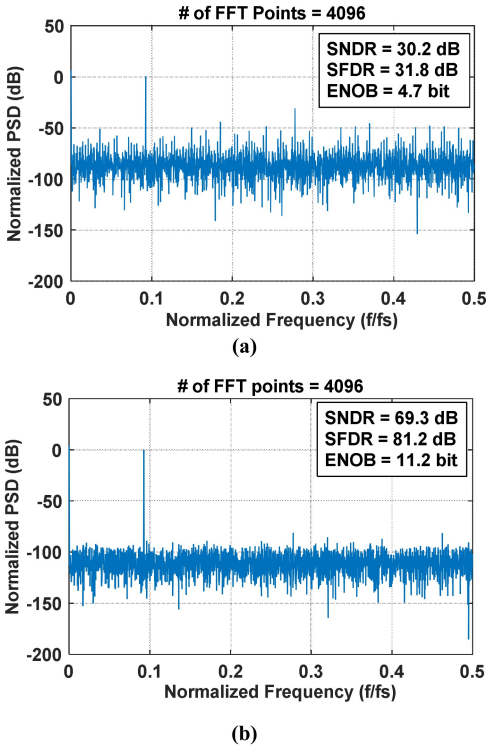

Fig. 8: Circuit level simulations (a) before and (b) after the calibration.

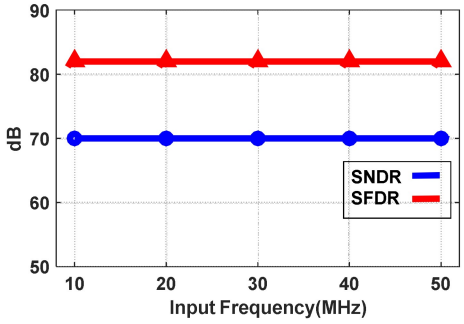

Fig. 9: SNDR and SFDR versus the input signal frequency.

TABLE I: COMPARISON WITH SEVERAL OTHER CALIBRATION TECHNIQUES.

Reference	[10]	[11]	[9]	[18]	This work
Additional analog circuit	none	none	none	none	none
Tracking capacity	α_1	$\alpha_1, \alpha_2, \alpha_3$	α_1, α_3	α_1, α_3	α_1, α_3
Additional digital hardware	moderate	moderate	moderate	moderate	low
Resolution (bits)	12	12	12	12	12
SNDR (dB) improvement	18.2	34.1	51	31	39
SFDR (dB) improvement	19.2	40.8	65	41	49
Supply voltage (V)	1	1	1	1	1

V. CONCLUSION

A digital background calibration method has been exhibited to amend the gain and gain nonlinearity errors in pipelined ADCs. In this method, the coefficients are estimated by using the residue histogram, changing decision points, and residue characteristic. The hardware complexity

is reduced due to using low calculations and some common blocks for extracting the calibration data. This method does not require any extra analog circuit and it is performed only in digital domain. According to the system and circuit level simulation results, the errors are appropriately suppressed and the ADC performance improves as well.

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