Realization of the 2nd-order NTF Enhancement in a Time-Encoded Continuous-Time Sigma-Delta Modulator Using Passive Elements

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***Abstract*—Embedding time encoding into the quantizers, has been proven to be as a promising technique to overcome the data converter's resolution problems in low-voltage CMOS circuits. In this paper, an NTF-enhanced time-based continuous-time sigma-delta modulator (TCSDM) with second-order noise-coupling is presented. The structure takes advantages from a combination of an asynchronous pulse width modulator (APWM) as a voltage-to-time converter (VTC) and a time-to-digital converter (TDC) as a sampler to realize the time quantization. By using a novel implementation of the noise-coupling technique, the modulator's noise-shaping order is improved by two. The concept is elaborated for an NTF-enhanced second-order TCSDM and behavioral simulation results are presented to verify the performance. To further confirm the effectiveness of the structure, the circuit-level implementation of the modulator is provided in TSMC 90nm CMOS technology. The simulation results show that the proposed modulator achieves a dynamic range of 84 dB over a 30 MHz bandwidth while consuming less than 25 mW from a 1 V supply voltage. With the proposed time-based noise-coupling structure, both the order and the bandwidth requirements of the loop filter can be relaxed, which in turn the analog complexity of the modulator is significantly reduced.**

Keywords— Asynchronous pulse width modulator; continuous-time sigma-delta modulators; noise-coupling; time-to-digital converter.

I. INTRODUCTION

An increasing demand to the wideband communication systems have led to a significant growth in a need of low cost, low-power analog-to-digital converters (ADCs). Continuous-time (CT) sigma-delta modulators are widely used to digitize moderate to high bandwidth signals due to their efficient power consumption and silicon area. However, the voltage headroom reduction in current CMOS technologies not only reduces the signal-to-noise ratio (SNR), but also deteriorates the effect of the nonlinear behavior of transistors, and thus, reduces the dynamic range (DR) of voltage mode circuits.

Due to finer time resolution of the advanced CMOS technology, the processing of the signal in the time domain becomes increasingly beneficial [1]. As a result, the time-based quantizers have emerged as promising quantization architecture for CT sigma-delta modulators. A major advantage of signal processing in the time domain (i.e., time-mode ADCs) is the digital-friendly nature of the system, which scales down with the technology.

In [2] a closed-loop time-based sigma-delta modulator with a voltage-controlled oscillator (VCO) quantizer is designed for wideband applications. In this structure the effect of the nonlinearity of the VCO and the harmonic tones are suppressed by the gain of the loop filter. Although the noise shaping order is increased by one order due to the VCO but since the gain of the VCO is small, the loop filter must provide most of the gain needed to suppress the quantization noise. In [3] a closed-loop CT sigma-delta modulator employing a synchronous ramp-based pulse-width modulator (PWM) as a VTC and a multi-bit TDC as a sampler is introduced. Besides having some significant achievements, this architecture suffers from some main problems mainly arising from the combination of the synchronous PWM and the TDC which causes the aliasing of the high frequency components to be present in the spectrum of the input PWM waveform. This way, the noise floor significantly increases which degrades the SNDR of the modulator. The time-encoded structures in [4,5] can also be categorized into wideband high performance PWM-based CT sigma-delta modulators. However, their sampling rates are in the order of multi-GHz which may make them unsuitable for low power applications.

The proposed structure is based on an asynchronous PWM (APWM) which takes advantage from the second order noise-coupling idea to enhance the shaping property of the modulator without affecting its signal transfer function (STF) and adding any integrator in the loop filter [6]. The novel implementation of the noise-coupling not only enhances the performance of the modulator but also it resolves the problems in realization of this concept in conventional CT sigma-delta modulators. In this structure, a multi-bit double-sampled TDC, based on dual-edge triggered D-flip flops (DEDFF) is utilized to digitize the output signal of the APWM. The TDC is followed by a digital block named as digital-to-time converter (DTC). The combination of TDC and DTC can emulates the multi-bit DAC operation by providing the time quantized feedback pulse without the need

of a multi-bit DAC. This brings a significant improvement in area and power in a practical circuit.

The rest of the paper is organized as follows. The concept of the time-encoding is described in Sect. 2. The basics of the noise-coupling is elaborated in Sect. 3. The proposed TCSDM with second-order NTF enhancement is introduced in Sect. 4. Section 5 and 6, are devoted to the implementation of the proposed modulator. Finally, Sect. 7 conclude the paper.

II. The Concept of Time-Encoding

A. Pulse-width modulation as a voltage-to-time conversion

The principle core of the time-based sigma-delta modulators is a voltage-to-time converter. The VTC can be realized using VCOs, pulse-width modulators (PWM) or voltage controlled delay units (VCDU). In the proposed structure we will use asynchronous pulse-width modulator (APWM). An APWM operates without a reference clock to avoid the quantization noise aliasing as exists in [3]. A self-oscillating behavior of the APWM resolves the need of an additional circuitry to create an external carrier, which results in a compact circuit. An APWM consists of an integrator, a hysteretic comparator and a negative feedback loop path. The output of the APWM is a continuous-time, discrete-amplitude signal without the quantization noise since the time is not quantized or sampled [7]. The oscillation frequency or a limit cycle denoted by f_c is the main design parameter that determines the spectral properties of the APWMs and the quality of the amplitude-time transformation.

Utilizing an APWM, the simplified block diagram showing the exchange of a conventional voltage-mode CT sigma-delta modulator to a time-based one is illustrated in Fig. 1. Regarding the challenges related to the multi-bit digital-to-analog converters (DACs), one of the main concepts behind the time-encoding quantizers is to get rid of using multi-bit DACs in the feedback path. To gain a better understanding from this feature of time-encoded quantizers, assume that the APWM has a carrier frequency of f_c and the sampling frequency is f_Q. It can be shown that the combination of an n-bit conventional quantizer with an n-bit DAC which is sampled at the rate of f_c can be replaced by an APWM which its output is oversampled by f_Q where $f_Q=2^n*f_c$ [5]. As a result of this concept, by choosing $f_Q>>f_c$ a modulator equipped with a time-based quantizer can resolve the need of an n-bit DAC without degrading the performance of the modulator.

Another superiority of the time-based sigma-delta modulators is that, the loop filter has to process the signals with the rate of f_c rather than f_Q where $f_c<<f_Q$. This way, the speed requirements of the Opamps of the loop filter is relaxed and thus the significant reduction of the total power is obtained.

On the other hand, the most of the APWM out of band energy is concentrated around the carrier frequency but in the case of the conventional single-bit sigma-delta modulators it is spread over all the frequencies. Hence, the improvement of the resolution in the time-based structures can be expected [5].

Although providing such a high sampling frequency as f_Q is a major challenge but this can be realized using an N-stage poly-phase sampling scheme [7]. This way, the rate of the sampling clock is reduced and reaches to f_Q/N.

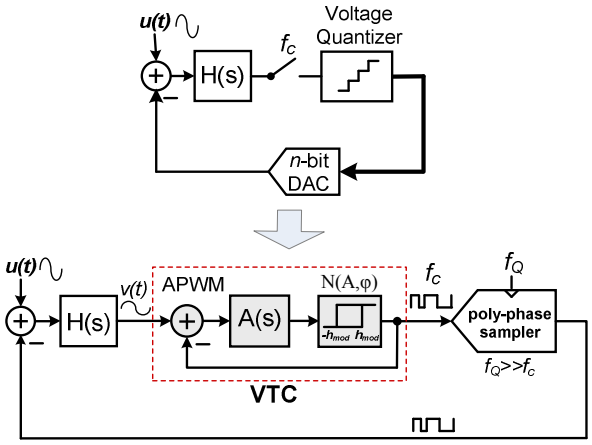

Fig. 1. An exchange of the voltage-mode CT sigma-delta modulator to the APWM-based time-mode structure..

III. NTF Enhancement by Noise-Coupling

The SNR of a sigma-delta modulator depicted in Fig. 1 is improved if the order of the loop filter, $H(s)$, is increased. But this improvement is achieved at the expense of lower satiability. An NTF enhancement through noise-coupling (NC) is a technique for increasing the noise-shaping performance of a sigma-delta modulator. In this technique, the STF does not change and the order of the loop filter remains the same. This way, the new NTF for a noise-coupling sigma-delta modulator denoted as NTF_{NC}, can be stated as [6].

$$NTF_{NC} = \left(1 - G(z)\right) NTF \tag{1}$$

where $G(z)$ is the transfer function a finite-impulse response (FIR) filter. The block diagram of the noise-coupling concept in conventional sigma-delta modulators is shown in Fig. 2.

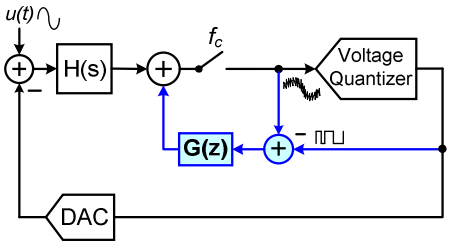

Fig. 2. Noise-coupling in conventional CT sigma-delta modulator.

Unlike the realization of the noise-coupling technique in discrete-time (DT) sigma-delta modulators, it is not so straight forward to take the advantage from this idea in CT sigma-delta modulators owing to the difficulty in implementing the analog subtractor. In [6], a discrete-time noise-coupling branch using a switched-capacitor circuit and a clocking scheme is utilized

to realize the noise-coupling in a CT sigma-delta modulator. Although it is shown that the noise-coupling is properly achieved but the introduced modulator is not a fully continuous-time since the noise-coupling branch utilizes a discrete-time active subtractor which makes it an unsuitable choice for wideband and low power applications.

Applying DT-to-CT conversion accompanied with some modification on the structure in Fig. 2, one can implement the first order enhancement using only passive filters which does not dissipate power . Although higher-order enhancement is also feasible but it requires positioning multiple zeros at DC to form the high-pass profile for the NTF, which cannot be implemented using passive filters only, and requires additional active filters and therefore increases the power dissipation. We will show that using APWM as a VTC, not only the first order NTF enhancement is feasible but also the second order noise-coupling is also realizable without a need of additional active filter. During the next section we are going to show this superiority of the proposed TCSDM.

A. Proposed NTF-Enhanced TCSDM

The conceptual block diagram of the proposed noise-coupling TCSDM with excess loop delay (ELD) compensation and noise-coupling branches is shown in Fig. 3a where $G(s)$ is the CT equivalence of $G(z)$. In Fig. 3a, the branch with a delay of e^{-sT_d} is applied for ELD compensation, where T_d mainly accounts for the total delay of the APWM and the sampler. Although the ELD has negative effect on the stability of the modulator, but it can be used to simplify the architecture and reduce the number of needed feedback branches.

Taking an advantage from the inherent summing node of the APWM, we can integrate all the feedforward and internal feedback branches of the structure at the input point of the APWM. This modification resolves the need of an extra subtractor or a summing amplifier. Using this feature, the modified version of the structure is illustrated in Fig. 3b. Here, the $G(s)$ will be approximated according to the transfer function of the FIR $G(z)$. The approximated $G(s)$ can be implemented using only passive elements.

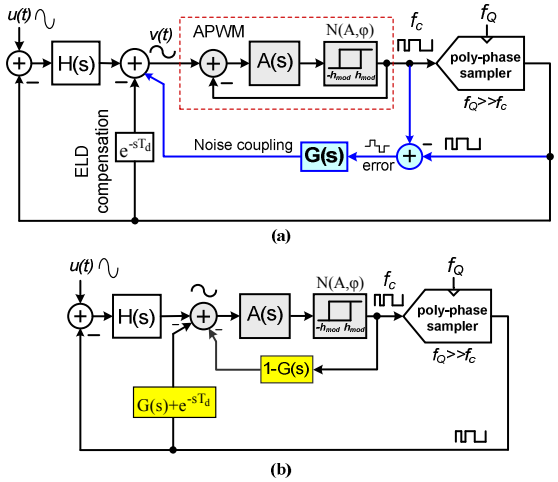

Fig. 3. (a) The conceptual illustration of the proposed NTF-enhanced modulator (b) its modifed version.

According to (1) assuming $G(z)=z^{-1}$ causes an NTF be enhanced by one order. As implied before, in the proposed TCSDM the rate in which the output of the loop filter is sampled is approximately equals to the switching frequency of the APWM, f_0, where $f_0 \approx f_c$. Hence, the CT counterpart of $G(z)=z^{-1}$ can be given as e^{-sT_0} where T_0, is the equivalent of the time delay associated with z^{-1}. According to the Taylor's series approximation of e^{-sT_0} it can be shown that for $f<<1/T_0$:

$$e^{-sT_0} \approx \frac{1}{1+sT_0} \tag{2}$$

which indicates that, The transfer function of the FIR $G(z)$ can be realized by a passive low-pass filter (LPF) in a CT counterpart. This approach is applicable if an LPF provides a constant delay to its input. Otherwise, it is not an effective alternative to the FIR $G(z)$. Fortunately, owing to the oversampling phenomenon in the sigma-delta modulators the approximation of $f<<1/T_0$ is usually valid. By using this approximation, the feedback branch of the APWM and also the ELD path of Fig. 3b for the case of the first order noise-coupling can be represented as:

$$1-G(s)_{NC1} = 1-\frac{1}{1+sT_0} = \frac{s}{s+\omega_{p1}} \quad ; \ \omega_{p1} = 1/T_0 \tag{3}$$

$$e^{-sT_d} + G(s)_{NC1} = 2\times\frac{\omega_{p1}}{s+\omega_{p1}} \quad ; \ T_d \approx T_0 \tag{4}$$

where the subscript NC_1 refers to the 1st order noise-coupling.

IV. Second Order NTF Enhancement

A. The Concept

In this section we want to study the feasibility of the generalization of the previously mentioned NTF enhancement technique to the higher orders. To do this, we will elaborate the possibility of the 2nd order noise-coupling realization. As indicated before, this order of the NTF enhancement may not be so attractive in conventional noise-coupling structures due to the need of additional amplifiers. But we will show the effectiveness of this idea in the proposed modulator.

Considering (1), the 2nd order NTF enhancement is achieved if a second order FIR $G(z)$ is realized as below:

$$G(z)_{NC2} = 2z^{-1} - z^{-2} \tag{5}$$

Applying the approximation calculated in the previous section, the CT equivalence of (5) can be given as:

$$G(s)_{NC2} = \frac{2}{1+sT_0} - \left(\frac{1}{1+sT_0}\right)^2 = \frac{1+2sT_0}{(1+sT_0)^2} \quad (6)$$

Similarly, the transfer function of the ELD branch and also the APWM feedback path of Fig. 3b can be calculated as:

$$e^{-sT_d} + G(s)_{NC2} = \frac{2+3sT_0}{(1+sT_0)^2} \approx \frac{3-\alpha}{1+s/\omega_{p2}} \quad ; \omega_{p2} = 1/T_0 \quad (7)$$

$$1 - G(s)_{NC2} = \frac{s^2}{(s+1/T_0)^2} = \frac{s^2}{(s+\omega_{p2})^2} \quad (8)$$

Where α (i.e., α<1) is a constant that is applied to further equalize the two functions within the desired bandwidth.

This indicates that, the feedback path of the APWM is a second order HPF consists of two zeros in the origin and two real and identical poles in the left side of the $j\omega$-axis. Realization of this second order HPF may be a major challenge which may give the uncertainty to the usefulness of the 2nd order NTF enhancement technique. But we will show an effective method to implement this transfer function without adding any additional hardware.

B. Realization of the second order HPF

Regarding (8), an active second order HPF should be designed to realize this second order HPF. The schematic of the second order active HPF is shown in Fig. 4a. The transfer function of this filter can be stated as:

$$\frac{V_{o1}(s)}{V_{i1}(s)} = -\frac{s^2}{(s+1/RC)^2} \quad (9)$$

As is clear, the transfer function in (9) can successfully be a representative for the one in (8) if we assume ω_{p2}=1/RC. But a major drawback of this filter is the existence of two amplifiers which increases both the design complexity and the power consumption. In order to avoid these two amplifiers we must modify the transfer function of (8), since it is impossible to realize it without using the amplifiers. For this, we can slightly split the poles of the second order HPF. In other words, if we replace the poles in $\omega_{p2}\pm\varepsilon$ (i.e., $\varepsilon<<\omega_{p2}$) rather than arranging both of them in ω_{p2}, we can obtain a degree of freedom to implement an alleviated second order HPF. An implementation of second order HPF with new positions of the poles is shown in Fig. 4b. The transfer function associated with this circuit is calculated as:

$$\frac{V_{o2}(s)}{V_{i2}(s)} = -\frac{s^2}{s^2\left(\frac{R_2}{R_2}\right) + s\left(\frac{1}{R_3C_2} + \frac{1}{R_3C_1} + \frac{R_2}{R_1R_3C_1}\right) + \frac{1}{R_1R_3C_1C_2}} \quad (10)$$

As is clear, the transfer function has two zeros in the origin and two different poles which can be matched with $\omega_{p2}+\varepsilon$ and $\omega_{p2}-\varepsilon$ with proper selection of the value of the elements.

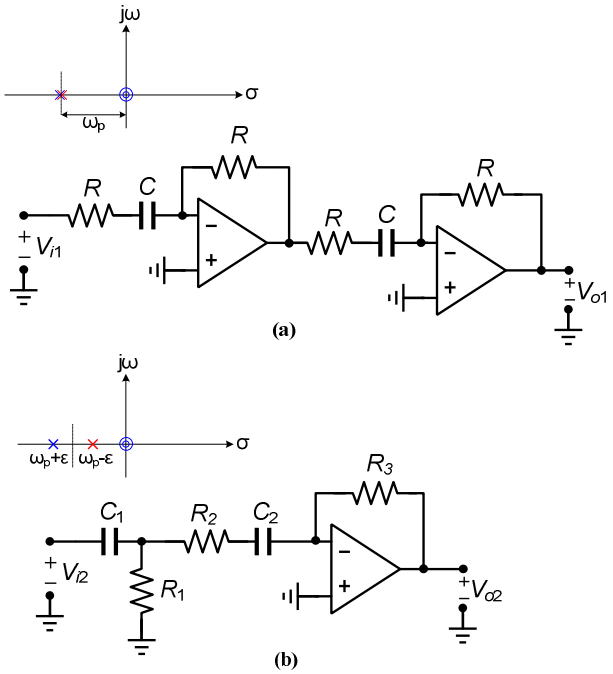

Fig. 4. (a) Second-order active HPF (b) the proposed 2nd order HPF.

Although the new 2nd order HPF still needs an amplifier, but it should be noted that this amplifier can be removed since the inherent summing node of the APWM can serve as an amplifier for this filter. In other words, the superiority of the proposed 2nd order noise-coupling based on an APWM is that the inherent amplifier of the APWM not only serves as a summing node to the ELD compensation and feedforward branches, but also it can play the role of an amplifier to realize a second order HPF which exists in the feedback path of the APWM. This way the second order NTF enhancement concept is realized without a need to any additional hardware.

V. Block Diagram of the Proposed TCSDM

A. The proposed structure

To gain a detailed view from the complete structure of the proposed TCSDM, a second-order example of the modulator employing the 2nd order noise-coupling technique is illustrated in Fig. 5. Although the loop filter is of the order two but the noise shaping is of the order 4 due to the second order noise-coupling. The loop of the APWM oscillates properly if the Barkhausen criterion is satisfied and also if the input signal is slower enough compared to its output signal, $p(t)$. It means that high frequency components should be attenuated before the summing node at the input of the APWM. For this to be satisfied, a first-order passive LPF such as $k_f\omega_f/(s+\omega_f)$ is utilized in the main feedback path to filter out the high frequency components around the limit cycle frequency of

$p_q(t)$. This filter can also improve the clock jitter immunity of the modulator and helps to better compensate the ELD.

a combination of an ADC/DAC, thus resolving the need of a multi-bit DAC.

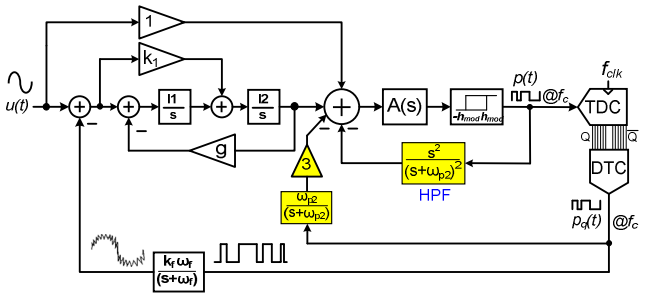

Fig. 5. A complete block diagram of the proposed second-order TCSDM with second order NTF enhancement.

B. TDC/DTC Structure

A TDC is mostly composed of digital components such as inverters and latches, and hence, it can be benefited from the high speed and low power consumption of digital circuits [1]. In an N-level TDC, the combination of a delay line and N latches divide the phase of the input clock into N-1 similar parts and outputs a quantized version of the input pulse widths. For the TDC to be able to detect all the edges of the APWM output signals, the TDC sampling frequency should be $f_{clk} \geq 4f_c$. But in the proposed TDC, all of the latches are based on dual edge triggered DFFs (DEDFFs). This way, a double-sampled TDC is realized and the minimum required sampling frequency is halved as $f_{clk} \geq 2f_c$. This, results in alleviating the design constraints and also leads to the reduction of the power consumption. The TDC outputs are recombined together to provide the single bit quantized feedback pulse using a DTC. The DTC is comprised of two N-input OR gates and two resettable DFFs asynchronously clocked by the output of two OR gates. Note that An N- stage double-sampled TDC/DTC clocked at f_{clk} can be conceived as a mere DFF with a virtual sampling clock of $f_Q=2N\times f_{clk}$ which emulates an operation of a multi-bit DAC. This way, a significant reduction in the complexity of the design of the TCSDM's feedback branch is achieved.

C. System-level simulation results

Behavioral simulations were performed in MATLAB/SIMULINK to verify the performance of the proposed TCSDM in more details. In all of the simulation steps, the TDC is a 6-stage delay-based structure with typical resolution of 80 psc for T_Q which is defined based on the characteristic of a 90 nm CMOS technology [3]. The signal bandwidth of the modulator is chosen as 30 MHz, the loop filter structure is a feedforward topology and f_c is 450 MHz while the f_{clk} is 1 GHz. The validity of the noise-coupling technique is also elaborated via comparing the dynamic range of the NTF-enhanced TCSDMs with the non-enhanced second-order one. These DR plots are depicted in Fig. 6. As

To realize the poly phase sampler, a combination of a TDC and DTC is utilized. The combination of TDC/DTC works as expected, the dynamic range of the NTF-enhanced second-order TCSDM is significantly improved.

To obtain a better dynamic range, one can make the resolution of the TDC finer. However, due to the technology limitations, it is not possible to decrease T_Q as much as desired. On the other hand, increasing the TDC stages can also be an improvement factor. However, the dynamic range enhancement with increasing the number of the TDC stages comes at the expense of the higher power consumption and larger silicon area. Although increasing the value of f_c may improve the dynamic range, but as mentioned before, for the stability problem, the ratio of $f_Q/2Nf_c$ should be at least higher than 2, implying the upper limit for the limit cycle frequency. In a brief, the simulation results show that one can achieve the desired dynamic range by making a good compromise between the design parameters.

As a comparison of the proposed TCSDM with conventional voltage-based sigma-delta modulators assuming the same clock as we used, the conventional modulator needs a loop filter of order L=4 with a 1.5-bit quantizer or an L=2 with a 6.5-bit quantizer to achieve the DR of the proposed structure. This brief comparison can clearly shows the superiority of the proposed TCSDM from the point of performance and hardware view.

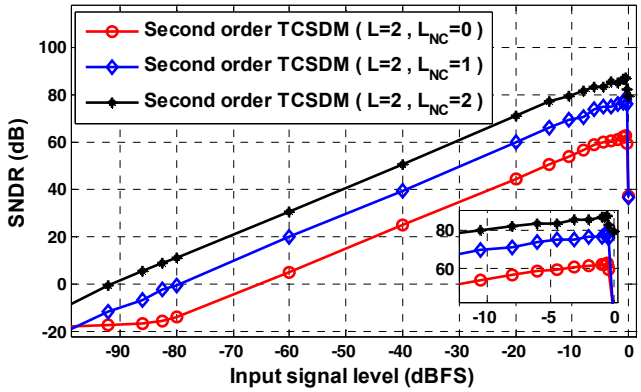

Fig. 6. System-level simulation of the SNDR versus the input signal amplitude.

VI. Circuit-Level Implementation

The implementation of the proposed TCSDM is shown in Fig. 7. The utilized technology is TSMC 90nm CMOS with 1V supply voltage. It incorporates a second-order feedforward active loop filter implemented using an opamp-RC integrator. Two-stage Miller-compensated topologies are selected for the OTAs to better satisfy the swing requirements of the stages.

The spectrum of the modulator with a 4.35 MHz, -2.6 dBFS input signal is also shown in Fig. 8. As expected, the spectrum and the dynamic range of the NTF-enhanced second-order TCSDM is improved and the expected slope of 80 dB/dec in the spectrum showing the effective 4th order noise shaping is achieved over the 30 MHz bandwidth.

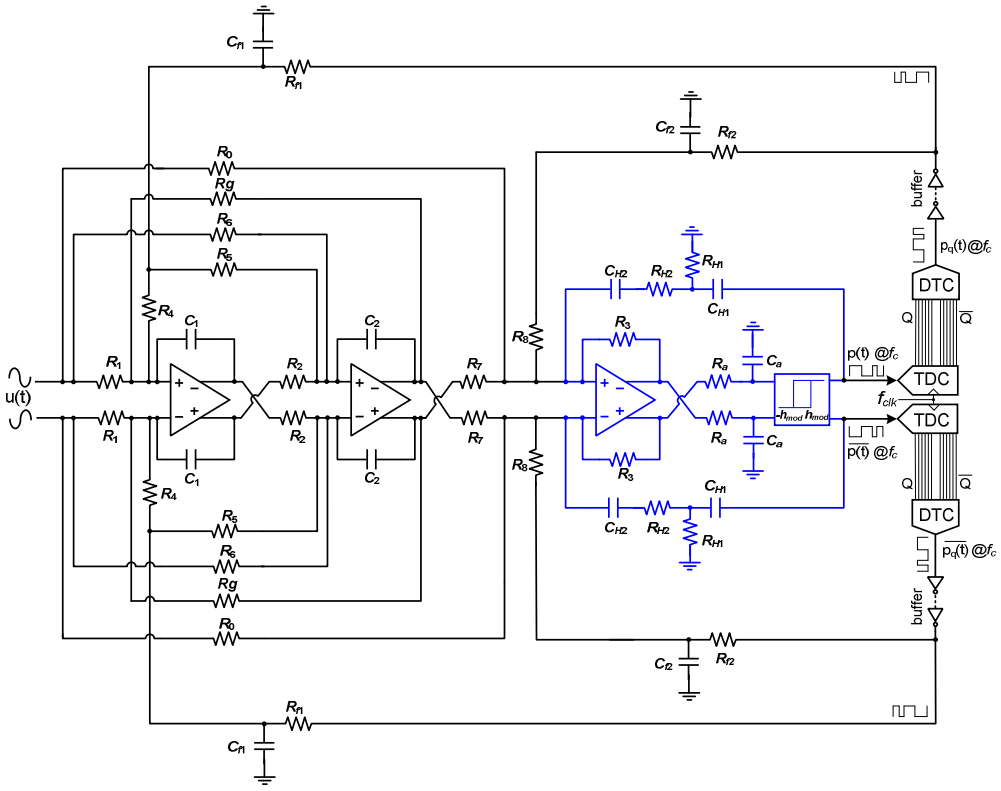

Fig. 7. Fully-differential implementation of the proposed TCSDM with L_{NC}=2.

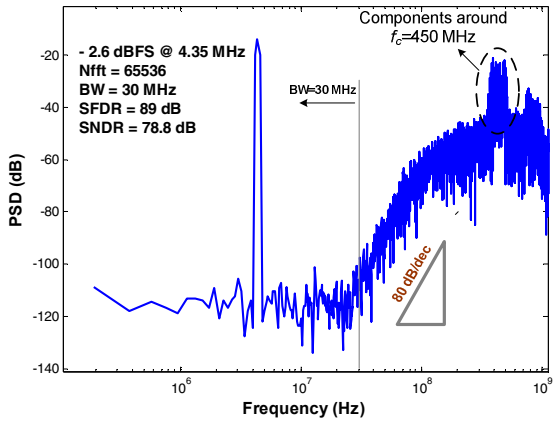

Fig. 8. Circuit-level simulation of the proposed TCSDM (TT@27°C).

VII. CONCLUSION

In this paper, an NTF-enhanced continuous-time sigma-delta modulator using a digital friendly time-based approach is presented. The proposed TCSDM leverages an asynchronous pulse width modulator (APWM) as a voltage-to-time conversion (VTC) and a time-to-digital converter (TDC) as a time quantizer in its architecture. A combination of the TDC with a digital-to-time converter (DTC) gives the possibility of avoiding multi-bit DAC. A novel realization of the second-order noise-coupling technique using passive elements is introduced to enhance the noise-shaping order of the modulator by two, without adding a significant hardware. Furthermore, by combining the TDC and DTC, the robustness of the proposed modulator against the clock jitter is improved due to the invariance of the feedback pulse widths. Simulation results performed both in system and circuit level, confirm the effectiveness of the proposed NTF-enhanced TCSDM.

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