Design of a Continuous-Time ΣΔ Modulator Using the Time Domain Quantization Approach

Mohsen Tamaddon and Mohammad Yavari
Integrated Circuits Design Laboratory, Department of Electrical Engineering,
Amirkabir University of Technology, Tehran, Iran
Emails: m.tamaddon@gmail.com, myavari@aut.ac.ir

Abstract— **Translation of the amplitude axis to the time axis can be a promising alternative to overcome the resolution problems in analog-to-digital conversion in low-voltage CMOS circuits. From this point of view, design of a continuous-time sigma-delta modulator (CTSDM) with time domain quantization is presented. The proposed structure utilizes an asynchronous pulse width modulator (APWM) in order to map the data from the amplitude to the time. A classic flash time-to-digital converter (TDC) is also employed to digitize the PWM signal. The TDC is designed based on dual-edge triggered D-filp-flops (DE-DFF) to enhance the time resolution. A simple digital-to-time converter (DTC) is combined with the TDC to feed the single bit DAC with a serial data stream. The modulator leverages a third order active loop filter to exhibit a -60dB/dec noise shaping behavior. The systematic simulation results show SFDR and SNDR more than 82 dB and 75 dB for 40 MHz BW and time resolution of 80 psec, respectively. A digital-friendly implementation of the modulator makes it suitable for low-voltage nanometer CMOS technologies.**

Keywords— Asynchronous pulse width modulator (APWM); sigma-delta; time-to-digital converter (TDC).

I. INTRODUCTION

The area and power-dissipation constraints are the major demands in modern mixed-mode circuit design. The ever-increasing growth in CMOS technologies leads to the optimal performance of digital systems. As a result, analog circuits are not only losing their capabilities, they must also cope with drastically decreasing voltage headroom and transistors intrinsic gain while meeting ever-demanding performance specifications [1].

Recent developments in mobile computing and wireless internet have led to exponential growth in demand for portable computers and smart phones that needs low cost, low-power wireless standards. Analog-to-digital converters (ADCs) are of inseparable parts of wireless communication systems. Design of high resolution ADCs suitable for broadband applications is always in the scope of the researcher's attention. However, the integration of efficient baseband circuits in modern CMOS technologies remains a challenge. Sigma-delta modulators have attracted a lot of attention as digital-friendly architectures for ADC since a substantial part of the signal processing is performed in the digital domain. Low-cost and low-power digital signal processing coupled with analog circuits with minimal matching requirements makes sigma-delta an ideal architecture for nanometric technologies. However, achieving wider bandwidths is a demanding task from the point of circuit design view due to of the oversampling nature in these kinds of converters. For this reason, discrete-time sigma-delta modulators (DTSDM) are hardly selected for broadband applications, since they need high speed analog amplifiers and switches. Continuous-time sigma-delta modulators (CTSDM) are widely used to digitize moderate to high bandwidth signals due to their efficient power consumption and silicon area [2]. It is important to note that the modulator with a continuous-time loop filter offers several advantages over DTSDMs at high signal bandwidth. However, the conventional mostly-analog structures suffer from the CMOS technology scaling problems. Declining in the voltage headroom not only increases the voltage error and reduces the signal-to-noise ratio (SNR), it also deteriorates the effect of the nonlinear behavior of MOS transistors, and thus, reduces the dynamic range of voltage mode circuits.

But, the intrinsic gate propagation delay time of digital circuits, is the primary advantage of technology scaling. The increasing switching speed of MOS transistors offers an excellent timing accuracy such that the time resolution of digital circuits has well overcome the problems of the voltage resolution in analog circuits. A new design strategy in which the information is represented by the duration time of pulses rather than analog nodal voltages or branch currents, offers a new solution to alleviate the challenges appeared in the amplitude domain. Unlike voltage-mode or current-mode circuits, time-mode circuits depict an analog signal with a time difference between two digital signals which is linearly proportional to the amplitude of the analog signal. This way, since the information is represented by the time difference, not only the performance of time-mode circuits scale well with technology, an intrinsic characteristic of time-mode circuits, also offer high-speed signal processing with low power consumption. Due to the tempting benefits of time-mode signal processing, ADCs in time-mode have received an increasing attention from both academia and industry recently.

Architecturally, time-mode ADCs can be classified into open-loop ADCs and closed-loop ADCs. Unlike the former structure, the latter employs the negative feedback to improve the performance. An open-loop time-mode ADC typically consists of a voltage-to-time converter (VTC),

such as VCOs, where the input voltage is sampled and converted to a pulse whose width is proportional to the amplitude of the sampled input and a TDC where the pulse width is digitized [3]. Open-loop time-mode ADCs can have short conversion time and lower power consumption. Its performance, however, is severely affected by the nonlinearity of the VTC, and the resolution and nonlinearity of the TDC [4]. As a result, these ADCs typically have a poor SNDR and alternative means are critically needed to compensate the linearity problems.

TDC-based closed-loop CTSDM is another type of time-mode ADCs, where a conventional quantizer is realized with a combination of VTC and a multi-bit TDC. In [5], a closed-loop CTSDM employing a synchronous ramp-based pulse-width modulator (PWM) as a VTC and a multi-bit flash TDC as a sampler is introduced. Besides having some invaluable achievements, this architecture suffers from some main problems mainly arising from the synchronous PWM. In frequency domain, the synchronous ramp-based PWM waveform's spectrum contains the signal frequency, reference frequency and its harmonics and progressively higher order intermodulation products of reference harmonics and signal frequency. The TDC quantizes the PWM waveform in time-domain. The feedback pulse generated by the TDC is essentially a sampled and held version of the PWM pulse with a sampling period of T_Q (the time resolution of TDC). This sampling process inevitably results in aliasing of the high frequency tones present in the spectrum of the input PWM waveform. Thus, the quantization noise floor is formed due to the TDC sampling. This way, the noise floor significantly increases which deteriorates the SNDR of the modulator.

In the proposed structure, an asynchronous PWM (APWM) is employed which maps the voltage to the time duration without a reference clock. As a result, the spectrum of the VTC will be better than that of in [5]. A multi-bit flash TDC which utilizes DE-DFFs in the register line is inserted to digitize the APWM output signal. Using DE-DFF can enhance the time resolution of the TDC since it works on both rising and falling edges. This way, the time resolution gets finer compared with a TDC based on a simple DFF, and as a result, the virtual sampling frequency of the TDC can be doubled. A DTC combined with the TDC can generate a serial bit stream which will be converted to the analog signal using a simple 1-bit DAC. A relaxed LPF is utilized at the output of the DAC to suppress the limit cycle oscillation frequency of the feedback pulse to alleviate the design constraints of the first integrator. To reduce the deviation of the APWM oscillation frequency, an extra feedback path around the comparator is employed.

This paper is organized as follows. Section II briefly discusses the conventional CTSDM and time-mode structure. Section III describes the details of the proposed architecture. Section IV summarizes the simulation results for the design example, and the conclusions are in Section V.

II. CONTINUOUS-TIME ΣΔ MODULATOR

The structure of the conventional multi-bit CTSDM and also its time-mode counterpart is depicted in Fig. 1. As it is illustrated in Fig. 1, the major difference between the voltage-mode CTSDM and time-mode one is their quantizers. While the voltage-mode CTSDM utilizes coarse ADCs to realize the quantizers, the time-mode structure leverages VTC in combination with TDC to realize the time quantizer in a more "digital-friendly" manner. As a result, the complexity of the CTSDM is significantly alleviated. As can be seen, both of the structures requires a high gain integrator to shape the quantization error.

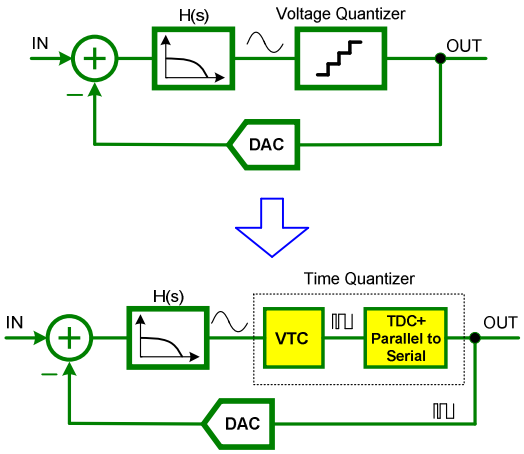

Figure 1. An exchange of voltage-mode CTSDM to the time-mode CTSDM.

III. CTSDM WITH TIME MODE APPROACH

The simplified block diagram of the proposed time-mode CTSDM is shown in Fig. 2. An APWM is employed to play the role of VTC with a better spectral profile in comparison with the synchronous ramp-based PWM. Excluding APWM, a multi-bit DE-DFF-based TDC and a simple feedback 1st order LPF is also employed which will be described in the following sections.

A. Asynchronous Pulse Width Modulator

APWMs which are similar to 1-bit sigma-delta modulators are closed-loop nonlinear systems that transform the information in the amplitude axis into the time axis. Unlike the synchronous PWM, due to the absence of the clock signal, the output of the APWM is a continues-time, discrete-amplitude (CT-DA) signal. This means that, since the time is not quantized or sampled, thus there is no quantization noise at the output [6]. As a result, neither SNDR nor SNR is calculated while SFDR is still valid due to the existence of the harmonics at the output of the APWM. In the APWM, the amplitude-time transformation is done using an inherent self oscillation denoted as a limit cycle. This oscillation frequency or a limit cycle (f_c) is the main design parameter that determines the spectral properties of the APWMs and the quality of the amplitude-time transformation.

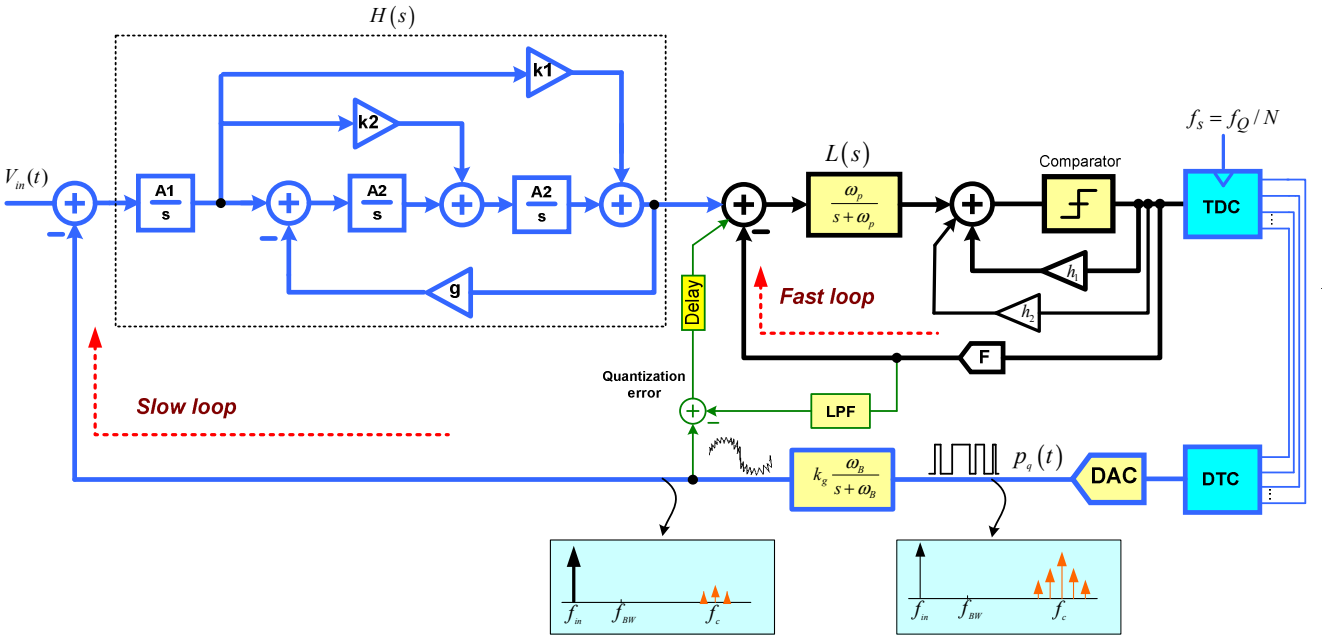

Figure 2. Simplified block diagram of the proposed time-based CTSDM.

The structure of an APWM is composed of a non-linear block and a low pass filter. It is common to use a comparator with hysteresis to realize a non-linear block. This kind of a comparator can be quasi linearly modeled with describing functions (DF) which is shown with $N(A,\varphi)$ in Fig. 3. Here, A is the amplitude of the input signal to the comparator, and φ is the input angular frequency. For a hysteresis comparator, the describing function is given by [7]:

$$N(A,\phi)=\frac{4D}{\pi A}e^{-j\sin^{-1}h/A} =\frac{4D}{\pi A}\sqrt{1-\left(\frac{h}{A}\right)^2}-j\frac{4Dh}{\pi A^2}\quad ;(A\geq h) \tag{1}$$

where h is the hysteresis limit and half of hysteresis width, and D is the level of the hysteresis window. Applying the Barkhausen oscillation criteria for a zero input APWM, the limit cycle and its amplitude will be obtained as below:

$$-1/N(A,\phi)=L(j\omega)\qquad @\omega=\omega_c \tag{2}$$

Increasing the degree of the filter gives a better performance for the APWM namely a better SFDR, at the expense of higher power consumption and also the poor stability. Hence, it is not usual to increase the degree of $L(s)$, up to higher than three. Due to the fact that, the noise-shaping behavior of the proposed CTSDM mostly depends on the $H(s)$ rather than $L(s)$, thus we prefer to use a simple first order $L(s)$ in the APWM loop. Although in this case, the SFDR of the APWM is not high, but since this APWM is inserted in the closed-loop architecture with a higher order $H(s)$, its nonlinearity effects can be significantly suppressed. Although applying Tsypkin's method [7] is more accurate than the describing function in calculating the limit cycle for lower order filters but due to the simplicity of the DF analysis and also in order to conveniently model the whole structure, the DF method is found to be more suitable for the analysis. This way, the Barkhausen criteria for a 1st order filter is as below:

$$L(j\omega)=\omega_p/(s+\omega_p)$$
$$\Rightarrow\omega_c=\frac{\omega_p\left(2+\sqrt{4-\pi^2h^2}\right)}{\pi h}\approx\frac{4\omega_p}{\pi h} \tag{3}$$

A major design concern in modulators based on the comparator with hysteresis is the dependency of the switching frequency on the input amplitude, which can deteriorate the loop gain and linearity performance significantly or even cause stability problems in a high-order design. As the limit cycle is a function of the hysteresis value (h_1), in the proposed structure we compensate the limit cycle deviations by applying an extra feedback branch (h_2) around the comparator. The compensation path gain can be obtained as follows:

$$\text{for: } V_{in}=V_m\sin(\omega t)$$
$$\overline{f_0}=f_c\left(1-0.5V_m^{\,2}\right)$$
$$\Rightarrow h_2=-0.5\,h_1V_m^{\,2} \tag{4}$$

where f_0 is the average instantaneous frequency, V_{in} is the sinusoidal input signal with the amplitude of V_m and f_c is the zero-input oscillation frequency or a limit cycle. This way, although f_0 fluctuates as a function of the input signal, but

its average value remains constant owing to the extra hysteresis compensation branch.

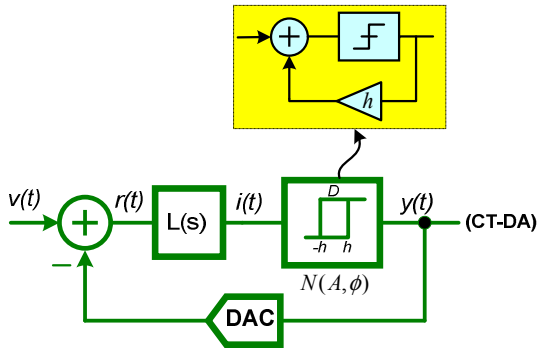

Figure 3. The structure of an APWM.

B. Time-to-Digital Converter

In order to overcome the shortcomings of the nanometric technologies and at the same time take the advantage of the precise timing edges available in these technologies, a TDC based approach for multi-bit quantization and feedback is investigated in this work. The schematic of a basic TDC and a DTC is shown in Fig. 4. The DTC logic works as a parallel to serial converter to feed a 1-bit DAC. The TDC outputs a pair of digital codes that corresponds to the time edges of its input pulse and it also generates a "time-quantized" feedback pulse. The quantization of the pulse is required to ensure that the feedback signal corresponds to the quantized code output of the TDC. The continuous-time loop filter shapes the TDC's quantization noise and PWM nonlinearity error. The time-quantized feedback pulse, denoted as $p_q(t)$, which is provided via a simple DTC, has to make transitions only at the time instances of clock transitions.

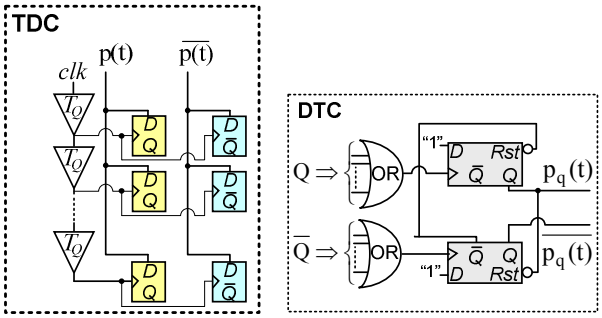

Figure 4. The schematic of a TDC and a DTC.

The input propagates through a cascade of digital buffers with the delays of T_Q, whose outputs are fed to the D input of an array of flip-flops. The output of the flip-flops provides a thermometric coded output that represents the time duration of the APWM output signal. It is apparent that the time resolution of this basic TDC is limited to the delay of one digital buffer (T_Q). In order to overcome this limitation, several solutions were proposed. The TDC architecture can be conceived as a mere DFF with a virtual sampling clock of $f_Q=N.f_s$. This means that although the TDC sampling clock is f_s but due to of the interleaving characteristic of the structure, the virtual sampling clock ($f_Q=1/T_Q$) is much higher than the applied sampling clock, f_s. This way, we can conclude that as the value of T_Q declines with the technology scaling, the virtual sampling clock of the TDC increases, and as a result, the resolution of the proposed CTSDM is enhanced.

C. Loop filter design

The power spectral density $E(f)$, of the time quantization error caused by the TDC is as below [6]:

$$E(f)=\frac{8}{3}f_0\,T_Q^{\,2} \tag{5}$$

The strength of the noise shaping of the proposed CTSDM is a function of the degree of the loop filter (L), the time resolution of the TDC (T_Q), the ratio of the limit cycle frequency and the input bandwidth (f_{BW}), which is named as over-cycling ratio ($OCR = f_c/f_{BW}$) and also the modulation depth of the APWM (M). It can be shown that the SNDR of the structure can be obtained from the Equation (6) [8]:

$$SNDR \triangleq \left(\frac{M}{T_Q}\right)^2 . \frac{OCR^{\,(2L-1)}}{f_{BW}^2} \tag{6}$$

A 3rd order loop filter $H(s)$ is selected for the structure to simultaneously meet the desired SNDR and the loop stability. The 3rd order noise transfer function (NTF) can shape the time quantization error of the TDC with the slope of -60 dB/dec. The filter design is commonly performed in discrete-time domain by realizing the desired $H(z)$ as $NTF=1/(1+H(z))$. The corresponding continuous-time transfer function (obtained by discrete-to-continuous-mapping, *d2cm*, function in MATLAB) assuming an NRZ-DAC is calculated as:

$$H(s)=\frac{A_1}{s}\frac{k_1s^2+A_3k_2s+A_1A_2}{s^2+gA_2A_3} \tag{7}$$

where the local feedback with the gain of g, is applied to spread the zeros of the NTF in the band of interest and provide a notch frequency to enhance the SNDR of the modulator.

As is shown in Fig. 2, a simple LPF is inserted in the outer loop path. This filter suppresses the high frequency components of its input such as the limit cycle and clock jitter noise. This way, a low frequency is provided to be subtracted by the input signal rather than a high frequency signal which may degrade the performance of the filter and also the APWM. As the input signal of the APWM is lower than the limit cycle, the degree of the validity of DF approximation in modeling of the modulator will be increased and vice-versa. From this point of view, a simple 1st order LPF can significantly enhance the performance of the modulator at the expense of a negligible reduction in the stability of the structure.

Similar to the noise-coupling techniques which is common in DTSDMs to increase the degree of the NTF [9], in the proposed structure, an identical method is utilized which results in the enhancement of the SNDR. The realization of this method is done using a subtraction of the filtered versions of DAC and APWM output signals. As we expect, the result of this subtraction is the quantization error of the TDC. The delayed version of this error is applied to the input of the quantizer. This way, an SNDR enhancement method identical to the noise-coupling technique is realized. The simulation results will show the amount of this enhancement.

IV. SIMULATION RESULTS

The proposed structure in Fig. 2 has been simulated and modeled in SIMULINK, showing a peak SNDR of 75 dB and an SDFR of 82 dB over 40 MHz bandwidth. In Fig. 5, the SNDR of the structure versus the input signal amplitude is shown. The FFT of output signal in the absence of all the compensation and enhancement techniques is shown in Fig. 6. Fig. 7 illustrates the spectrum after applying the compensation techniques. These techniques are: 1) $H(s)$ coefficient optimization, 2) limit cycle frequency deviation compensation by h_2 branch, 3) low pass filter in the feedback path to suppress the adverse effects of high frequency components, 4) using DE-DFF in the TDC to improve the time resolution, 5) spreading the NTF zeros and inserting a notch in the bandwidth, and 6) using a method identical to the noise coupling by applying the delayed version of the quantization error to the time quantizer.

V. CONCLUSION

In this paper, a wideband CTSDM is analyzed, designed and simulated. A time-mode approach is used to overcome the resolution problems in analog-to-digital conversion in low-voltage CMOS circuits. The proposed structure utilizes an asynchronous pulse width modulator (APWM) in order to transform the data from the amplitude to the time. A classic flash time-to-digital converter (TDC) was also employed to digitize the PWM signal. The TDC was designed based on a dual-edge triggered D-flip-flop (DE-DFF) to enhance the time resolution. The modulator leverages a third order active filter to exhibit a -60 dB/dec noise-shaping behavior. The systematic simulation results show SFDR and SNDR more than 82 dB and 75 dB for 40 MHz BW and time resolution of 80 psec, respectively.

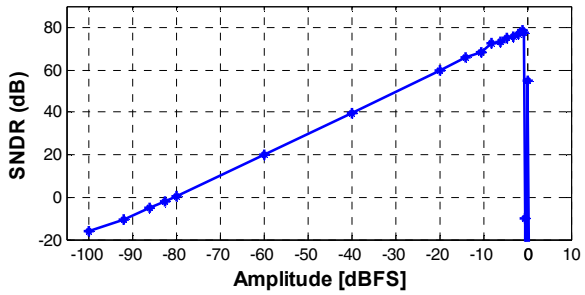

Figure 5. Simulated SNDR of the structure vs. the input signal amplitude.

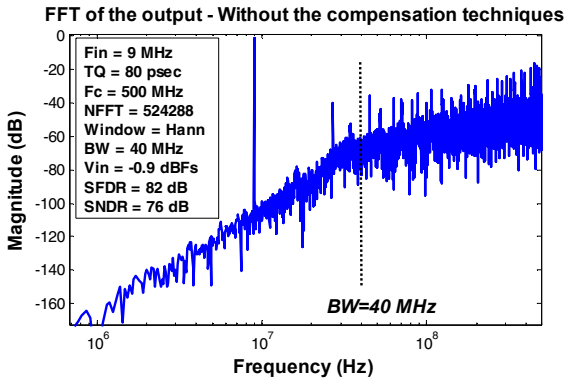

Figure 6. Output spectrum in the absence of all compensation techniques.

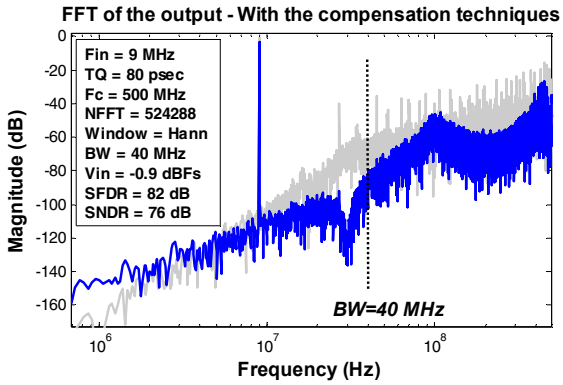

Figure 7. Output spectrum with the compensation techniques.

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