A High Speed and High Resolution, Parallel Pipeline A/D Converter in 0.6 –μm CMOS

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Abstract-This paper describes a 10-bit 150MS/s CMOS parallel pipeline ADC. The converter includes four parallel interleaved pipeline A/D converters with analog background calibration using adaptive signal processing, an extra channel, and mixed signal integrators that match the offsets and gains of time-interleaved ADC channels. With monolithic analog background calibration, the SNDR in all corner cases (SS, SF, FS, FF, and TT) and temperature between –40°C to 85°C is better than 57dB. The power consumption is 1200mw at a 3.0V supply voltage. This work is achieved in a 0.6 μm CMOS process.

I. Introduction

The increasing range of wide-band wireless Communication Standard, like the Universal Mobile Telecommunication System (UMTS), Wireless Local Loop (WLL), and Local Multipoint Distribution Services (LMDS), will evolve to high data rate applications within the next few years. The throughput rate of digital signal processing systems operating on analog inputs is often limited by the speed of the analog-to-digital (A/D) interface. So, for these applications we need the high resolution and very high sampling rate A/D converters.

To increase the speed of A/D converters beyond the technological limitations, more than one analog-to-digital converter (ADC) component, are interleaved in time as shown in Fig.1 [1], [2], [3], [5], [7], [8], [9]. Unfortunately the use of parallel ADCs has limited application because 1) the silicon area, and power consumption are increased dramatically, and 2) the performance of time-interleaved is degraded by the mismatches among the multiple channels. These mismatches include gain, offset, and timing mismatches that give rise to fixed-pattern effects, which are manifested as spurious harmonics in the frequency domain [2]. Previous monolithic time-interleaved ADC arrays used careful layout, foreground calibration, digital filters, or trimming to minimize the effects of these mismatches [3], [5], [10]. This paper describes a parallel pipeline ADC that uses the adaptive background calibration to match the gains and offsets of the channels [8], [9]. Background calibration is able to track variations over time and, it dose not interrupt the conversion process of ADC.

In section II, brief views of 1.5bit/stage pipeline ADCs are described. In section III, the parallel pipeline architecture and their problems are presented. The circuit description of this ADC is brought in section IV. Finally, section V contains the adaptive calibration method, and section VI, contains the simulation results.

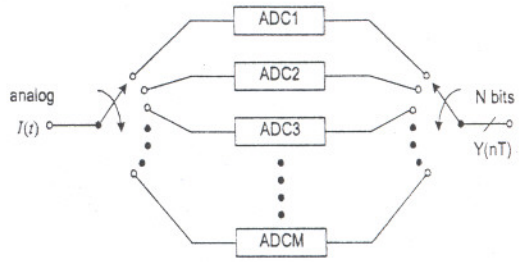


Fig.1: Time-interleaved ADCs.

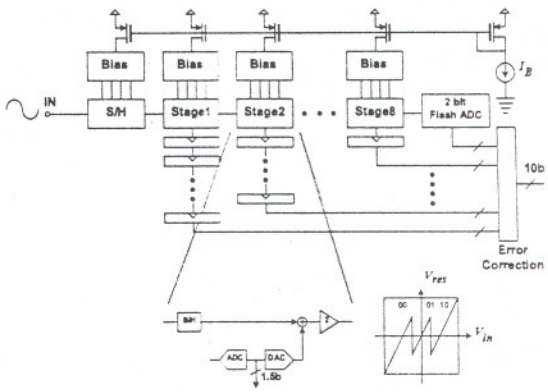


Fig.2: A pipeline ADC with 1.5bit/stage architecture.

II. Review Of Pipeline ADC

The functional block diagram of a 1.5bit/stage pipeline ADC is shown in Fig. 2. The characteristics of this ADC are described in [3] and [4]. The system consists of several cascaded gain stages, as shown in Fig.3. Each stage comprises of two comparators, a multiplexer, and a gain stage. Digital output codes of comparators drive a multiplexer to make a quantized analog estimate of the input. The multiplexer output is then subtracted from the input to make a residue, which is gained up by two and transferred to the next stage. The next stage manipulates on the residue of previous stage. In each stage, 1.5bit of input signal is quantized except the last one, which has three comparators, and 2bits are quantized. In implementation of pipeline multistage ADCs, digital error correction is usually employed with 0.5-bit or 1-bit redundancy between stages

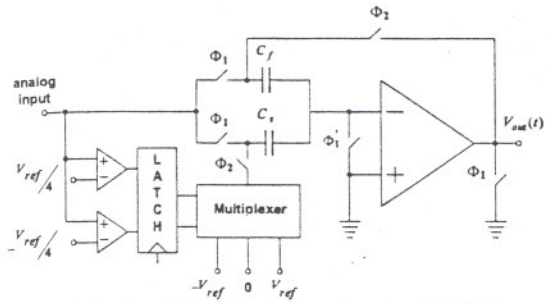


Fig.3: A single ended configuration of a stage of 1.5bit/stage pipeline ADC.

TABLE I: Summary of performance limitation and solutions.

Problem	Effects	Power	Solutions
Channel offset mismatch	Tones at: $k\frac{F_s}{M}$ $k=1$ to $(M-1)$	σ_o^2	offset cancelation or calibration (analog or digital)
Channel gain mismatch	Amplitude Modulation of input signal at: $k\frac{F_s}{M} \pm F_{in}$	$\frac{1}{2}A^2\sigma_g^2$	capacitor matching and share DAC levels
Sampling-time mismatch	Phase Modulation of input signal at: $k\frac{F_s}{M} \pm F_{in}$	$\frac{1}{2}A^2\omega_{in}^2\sigma_t^2$	use of Delay Locked Loop or Front-Rank sample and hold

except the last one [3], [4], [6]. This relaxes the offset requirements of the comparator to 2-bit level. If the comparators have offsets lower than $V_{REF}/4$, the system corrects the final digital output code.

III. Parallel Pipeline ADCs

This ADC uses multiple pipeline ADCs in parallel time-interleaved configuration in order to increase throughput. Fig.1 shows a block diagram of M time-interleaved ADCs. Each ADC operates at the sampling rate of F_s/M, where M is the number of parallel ADC channels. On the left side, an analog demultiplexer selects an ADC to quantize the input I(t). On the right side, the corresponding multiplexer selects the digital output of the ADCs. The overall system operates in sampling rate of F_s. Each channel contains, an input S/H followed by a cascade of pipeline stages. Performance of parallel pipeline ADCs is limited by two factors; first, by matching among the ADC channels. Three major sources of mismatch in time-interleaved ADCs are offset, gain, and sampling time mismatches among the channels. Second, the speed of each individual channel is limited by settling time of S/H and gain-stage in hold mode, which is determined, by op-amp settling time. In Table I, summary of performance limitation, mismatch error power, and solutions in the design of parallel pipeline ADCs are described [1], [2]. Here σ_o^2 is the channels offset variance; σ_g^2 is the channels gain variance; σ_t^2 is the sampling-time variance; A and ω_{in} are amplitude and frequency of the input signal, respectively.

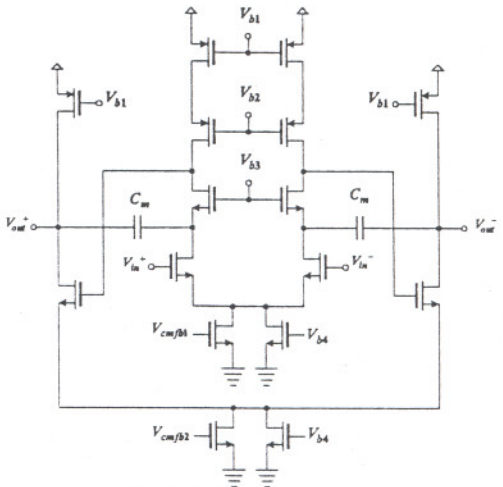


Fig.4: A two-stage op-amp.

IV. Circuit Description

In the main pipeline ADC, many basic building blocks are used. The speed of the ADC depends on the speed of these blocks. In the following section, their schematics, and properties are described.

A. High-Swing Amplifier

In pipeline ADCs, speed is limited by the settling time of the op-amp in its closed-loop configuration. So, op-amps with high GBW and high dc gain must be used. Most designers use one-stage op-amps with gain boosting or two-stage op-amps; Gain boosting technique uses four auxiliary op-amps that increase power consumption and silicon area. So, in this work a two-stage op-amp is used as shown in Fig.4. This configuration gives enough dc gain and GBW. This op-amp is very fast, has high swing and is a good choice for low voltages. In this configuration, two SC Common Mode Feedback (CMF) are used. First-stage of this op-amp does not need to accommodate a large voltage swing, so small transistor sizes can be used. This makes the parasitic capacitances smaller, which in turn makes the op-amp faster.

B. Latch Comparator

A 1.5bit/stage pipeline ADC employing digital correction does not require a low-offset comparator. The dynamic comparator shown in Fig.5 operates without sampling capacitors and has fairly low power consumption [3]. The input nodes are connected to the outputs of the previous stage. When latch='0', the comparator is in the reset mode and the outputs are low, when latch='1', the comparator compares input signal with the scaled reference voltage, to make a decision.

This comparator has a poor common mode rejection ratio (PSRR) with an offset that is dependent on the input common mode voltage.

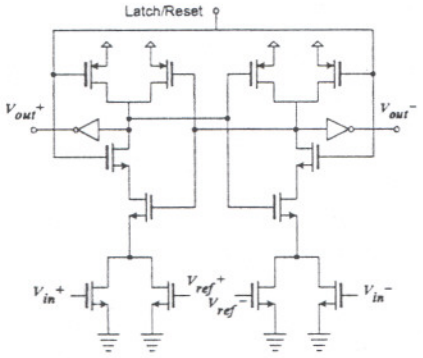
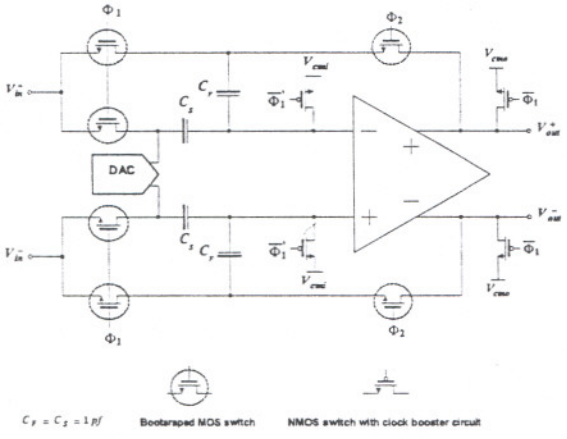
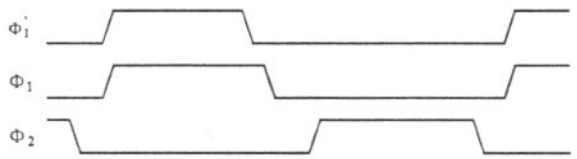


Fig.5: A dynamic latch comparator.



(a)



(b)

Fig.6: (a) The fully differential gain stage, And (b) the clock phases.

C. Gain Stage

The fully differential implementation of the gain stage is shown in Fig.6 (a). The bootstrapped switches are used for high swing switches (the input and the feedback loop switches). The clock booster circuit locally is used for each bottom-plate sampling, DAC, and output switches. This circuit decreases the on-resistance of a NMOS switch. The clock phases are shown in Fig.6 (b), Corresponding to sampling on phase Φ_1, bottom-plate sampling on phase Φ_1', and residue amplifying on phase Φ_2.

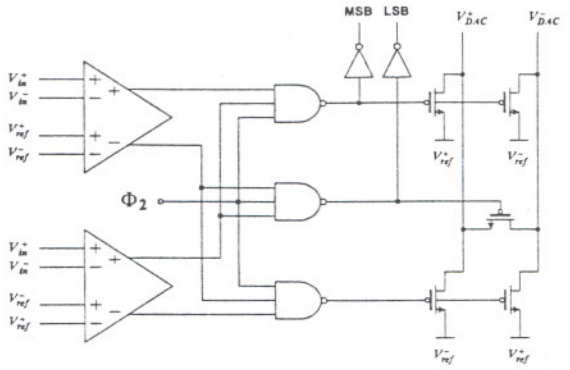


Fig.7: The Sub-ADC and DAC.

D. Sub-ADC And DAC

The fully differential sub-ADC and DAC circuit within each pipeline stage is shown in Fig.7. The threshold voltages of comparators are at $-V_{ref}/4$ and $V_{ref}/4$. The input signal is compared with the threshold voltages, and the comparator outputs are then decoded by some digital logic gate which selects one of the three values, $-V_{ref}$, 0, V_{ref} for the differential DAC output. The output is also gated by the clock phase Φ_2. The MSB and LSB bits are fed to latches. The NMOS switch with the clock booster circuit is used for each switch in this circuit. The schematic of the comparator is shown in Fig.5.

E. Bootstrapped MOS Switch

In low-voltage designs, transmission gates cannot be directly realized on a supply voltage below the sum of the two threshold voltages. In high-speed designs, the transmission gates aren't used, because the parallel NMOS and PMOS

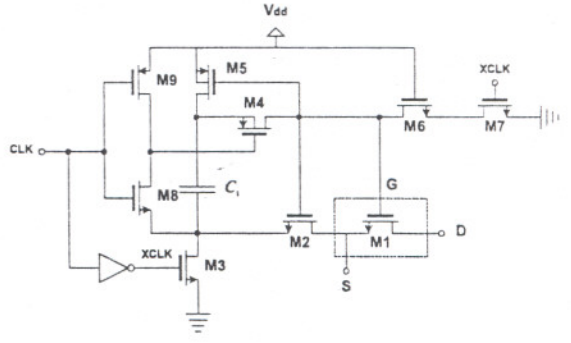


Fig.8: The bootstrapped MOS switch.

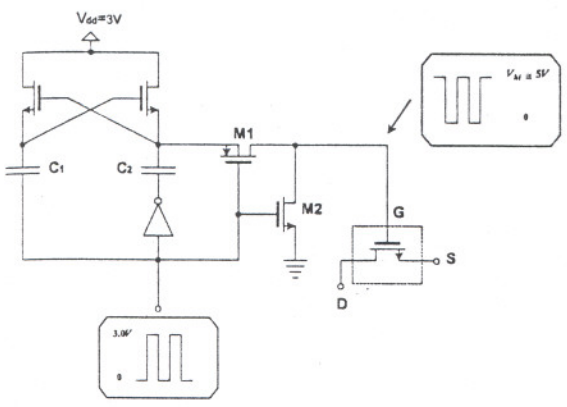


Fig.9: The charge pump circuit to boost the clock voltage.

transistors increase the parasitic capacitances. Moreover, the on-resistance has a nonlinear voltage dependent, which produces distortion when the switch tracks the input signal.

For reducing the on-resistance, distortion, and parasitic capacitances, the bootstrapped MOS switch was designed as shown in Fig.8 [4], [7]. In "off " phase, the capacitor C_1 is charged to supply voltage, and during the "on " phase, the capacitor C_1 is then connected across the gate and source terminals of the switching device M1. This capacitor will act as the battery across the gate and source during the "on " phase. Note that the body of the PMOS M4 is tied to its the source and latch up effect is suppressed by it. Device M6 reduces the V_{ds} and V_{gd} experienced by device M7 when XCLK=1. So, in this circuit no device experiences a relative terminal voltage greater than V_{dd}. This circuit presents the low and constant on-resistance switch, which reduces the distortion and gain error. This circuit can be used in low-voltage and high-speed designs.

F. The NMOS Switch With Clock Booster Circuit

In standard CMOS technologies, the threshold voltage of MOS transistor does not scale down with the supply voltage, and it lead to some problems, when the MOS transistor is used as switch at low-voltages. The threshold voltage with body-effect has become a large value, which the drive effective voltage reduces; hence the on-resistance of a MOS switch increases. It degrades the speed of SC circuits.

For reducing the switch on-resistance, width of the switch increases. However, this will also increase the parasitic capacitances associated with switch. Another way is to reduce the threshold voltage of the switches. However, this requires a few extra mask steps in the process, which are not available in typical CMOS process. The only option left is to increase the gate drive voltage to 5V. The approach chosen here is to simply use a dynamic charge pump circuit to locally boost the clock drive. This circuit is shown in Fig.9 [3].

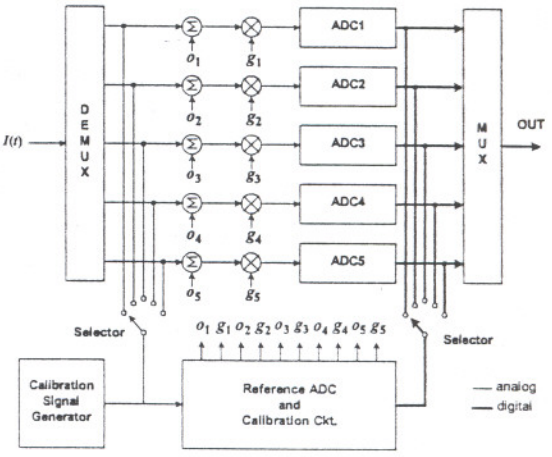


Fig.10: Adaptively calibrated ADC system.

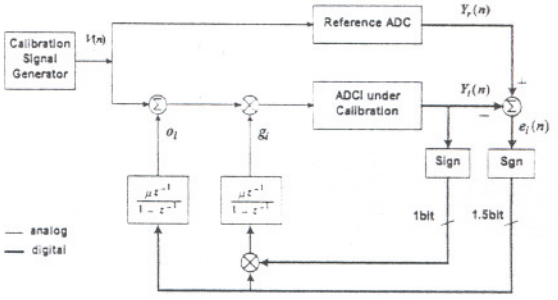


Fig.11: Mixed-signal adaptive calibration loop.

By applying a 3V clock signal, the capacitances C_1 and C_2 are self-charged to 3V through the cross-coupled NMOS transistors. When the clock is low, the voltage will be pumped on C_2 is greater than 3V, and the PMOS M1 will be on and transfers the voltage to the NMOS switch. Transistor M2 discharges the high voltage node to ground when the clock signal is high. The booster circuit converts a 3V clock signal to 5V. The switch is on when the clock is low and it is off when the clock is high.

To avoid latch up in the circuit, the body of the PMOS M1 is tied to its source, and the latch up effect is suppressed by it.

V. Calibration

Fig.10 shows a block diagram of a time-interleaved ADC system that uses adaptive calibration to overcome gain and offset mismatches [8]. Five high-speed pipeline ADCs are used in this work, of which, four ADCs are in sampling mode; while the other one is in calibration mode. The selected ADC and reference ADC (that is usually algorithmic) are fed with identical inputs from the calibration signal generator. The gain and offset of the selected ADC is adjusted to match with the reference ADC. The gain and offset adjustment are made using simplified

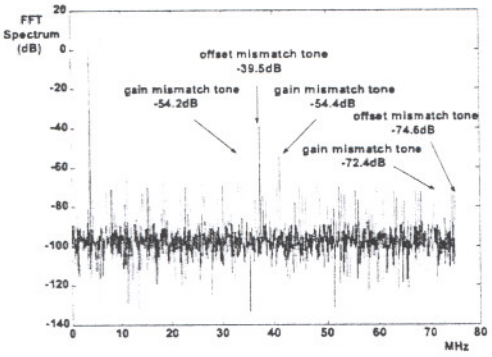


Fig.12: ADC's output spectrum before calibration.

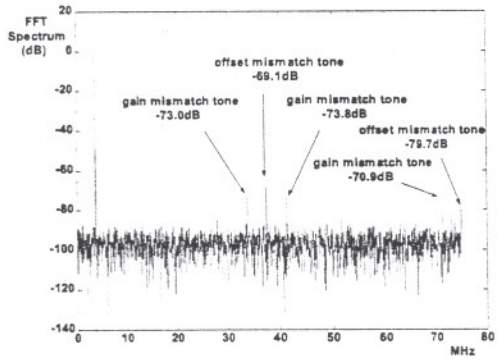


Fig.13: ADC's output spectrum after calibration.

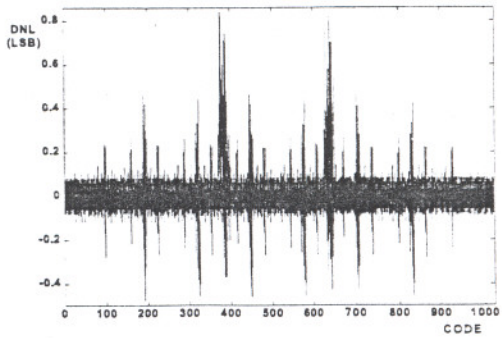


Fig.14: Differential nonlinearity versus code.

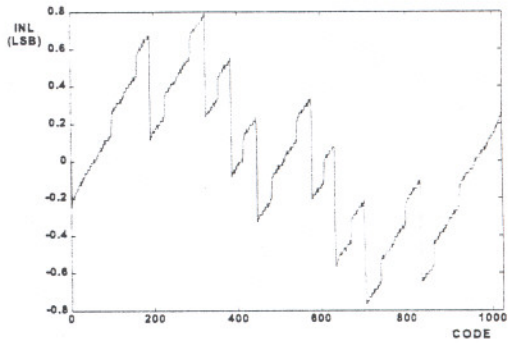


Fig.15: Integral nonlinearity versus code.

version of the Least Mean Square (LMS) algorithm [11]. Once the calibration cycle is completed, another ADC is selected for calibration, and the most recently calibrated ADC replaces it in the conversion mode.

Fig.11 shows the calibration loops of one of the five ADC channels. Here the ADC under calibration is ADCi; o_i is ith channel offset adjustment coefficient; g_i is ith channel gain adjustment coefficient; e_i is the difference between the output codes of ADCi and the reference ADC, and n is the sampling time index. The LMS loop adjusts o_i and g_i of ADCi, until the error power is minimized. This occurs when the overall offsets and gains of the reference ADC and ADCi are the same. The gain and offset terms are updated using the following equations [8]:

$$o_i(n+1) = o_i(n) + \mu\,\mathrm{sgn}[e_i(n)] \qquad (1)$$

$$g_i(n+1) = g_i(n) + \mu sign[Y_i(n)]\mathrm{sgn}[e_i(n)] \qquad (2)$$

Equation (1) and (2) are simplified versions of the standard LMS equations [11]. This configuration simplifies the required hardware. In this equations, the sgn() function is defined as:

$$\mathbf{sgn}(e_k) = \begin{cases} +1, & e_k > \delta \\ 0, & -\delta \le e_k \le \delta \\ -1, & e_k < -\delta \end{cases} \qquad (3)$$

TABLE II: Performance summary

Parameter	Performance
Resoultion	10 bit
Sampling Rate	150Msample/s
DNL	0.85 LSB
INL	0.80 LSB
SNDR@Fin=75MHz	≥ 57*dB* In All Corner Cases
Offset Mismatch (σ_o)	3.94 LSB
Gain Mismatch (σ_g)	0.295%
μ - Update Step Size	0.0002
Power Consumption	1200mW
Supply Voltage	3.0V

The δ in (3) is an LSB of the ADC.

VI. Simulation Results

The circuit is simulated in a 0.6-μm CMOS process. The circuit operates at a 3.0V supply, and with $2V_{pp}$ input differential voltage.

Fig.12 shows a Fast Fourier Transform (FFT) of the output before calibration, when a 3.9453125MHz full-scale sine wave input is sampled at the full clock rate (150MS/s). The tones caused by the gain and offset mismatches are at 33.801MHz, 41.198MHz, 71.301MHz, 37.5MHz, and 75MHz with amplitude of –54.2dB, -54.4dB, -72.4dB, -39.5dB, and -74.6dB, respectively.

These tones correspond to the gain mismatch of 0.295% and an offset mismatch error of 3.94LSB. These spurious tones limit the SNDR of this ADC to 39.1dB.

Fig.13 shows an FFT of the ADC output after calibration, the same input was applied. The calibration loop was activated for 2000 calibration cycles. After 150 cycles the calibration loop converged and the gain and offset of the selected ADC channel was adjusted with the reference ADC. Tones caused by gain and offset mismatches are –73dB, -73.8dB, -70.9dB, -69.1dB, and -79.7dB, which were reduced by –18.8dB, -19.4dB, 1.5dB, -29.6dB, and –5.1dB, respectively.

The system level Monte Carlo simulations were done, and the simulation results show that the DNL and INL are better than 0.85LSB and 0.8LSB, respectively as shown in Fig.14, and in Fig.15.

VII. Conclusion

This paper describes a 10bit 150MS/s parallel pipeline ADC. The gain and offset mismatches of channels are reduced by adaptive background calibration. The power consumption and silicon area of time-interleaved ADC increase linearly by the number of channels.

VIII. References

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