A Wide-Band CMOS Active Mixer with Linearity Improvement Technique

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Abstract— **In this paper, a wide-band second and third order nonlinearity cancelation technique is introduced to increase second and third input intercept points (IIP2 and IIP3) of the double- balanced Gilbert- cell mixer. In this topology an auxiliary path is used to suppress second and third order nonlinearity of the main path. Also in order to increase the robustness of the proposed mixer against process, voltage and temperature (PVT) variation a constant G_m bias circuit is employed. Post layout simulation results is done for 1 – 5 GHz RF frequency by using a 90 nm RF CMOS process with Spectre-RF. Simulation results reveals that the IIP2, IIP3 and conversion gain of the proposed mixer are improved approximately 6, 5.8 and 2.9 dB in average compared to the conventional mixer, respectively. In addition flicker noise of the proposed mixer decreased. Also, the mixer consumes 8.65 mW of power with a 1 V supply, while the power consumption increases about 10% compared to the conventional one.**

Keywords- Linearity, IIP2, IIP3, Conversion Gain, Noise Figure, Flicker Noise, CMOS Active Mixer

I. INTRODUCTION

Since the linearity of the receiver is mainly dominated by the latter blocks, the linearity of mixer is important. So mixer is a critical block in WB Radio-Frequency (RF) front ends. Passive mixers can easily achieve high linearity, whereas the conversion gain (CG) of passive mixers is smaller than one and the noise that comes from backend IF blocks are more effective to the whole receiver. Double-balanced Gilbert Mixer is popular in direct conversion receiver (DCR) due to relatively high conversion gain, low RF-LO feedthrough and high isolation performance [1], but it often has poor linearity performance.

For evaluating the extent of nonlinearity, two parameters of IIP2 and IIP3 are typically determined which represent second and third order intermodulation distortions. The second order nonlinearity can be reduced by employing differential structure but the third order nonlinearity still remain a problem.

Several linearization techniques have been proposed to enhance the linearity of CMOS down conversion mixers. A commonly technique for linearity enhancement is multiple gated transistors (MGTR) that demonstrated in [2]-[3]. In this technique an auxiliary transistor is connected to the main transistor in parallel. If the size and bias of auxiliary transistor are chosen properly the third order nonlinearity (g_m'') of the main transistor will be reduced. Another approach to cancel third order intermodulation (IM3) current of transconductance stage is IM2 injection method [4]. The post distortion technique in [5] uses a diode- connected transistor at the output of the transconductance stage to make IM3 current with equal amplitude and opposite sign to cancel IM3 current of the transconductance stage. In [6] negative impedance at switching stage is employed to cancel IM3 and reduce the flicker noise. Using the gate–bulk interaction in [7] and using interaction between two nonlinear systems in [8] are another approach to increase linearity of the mixers, too.

In this paper, a new linearization technique is proposed to decrease IM2 and IM3 current of the transconductance stage to increase IIP2 and IIP3 of the Gilbert mixer. Furthermore by using this technique, the DC current of the switching stage decreases so, the flicker noise of the proposed mixer decreases. Also, it used a constant G_m bias circuit to increase robustness of the proposed mixer against process, voltage and temperature (PVT) variations.

This paper is organized as follows: In section II description of the proposed mixer and linearization technique based on Taylor analysis is presented. Complete circuit of the proposed mixer and constant G_m bias circuit expressed in section III. Post layout simulation results by using a 90 nm RF-CMOS technology are given in section IV. Finally, conclusion presented in section V.

II. PROPOSED WIDE-BAND HIGH LINEAR MIXER

A. Proposed mixer

Assume the bulk terminal of NMOS transistor is connected to the ground, by neglecting of conductance nonlinearities effects such as g_{ds}, g_{ds}', g_{ds}'' and higher order of nonlinearity coefficients, the small signal drain current of the transistor expressed as follows:

$$i_{ds} = g_m(v_g - v_s) + g_m'(v_g - v_s)^2 + g_m''(v_g - v_s)^3 + \ldots \quad (1)$$

Where g_m, g_m' and g_m'' coefficients are the transconductance, second and third-order nonlinearity of the transistor transconductance, respectively. In addition v_g and v_s are gate and source voltages, respectively. Fig. 1 shows the coefficients of g_m' and g_m'' of a 10um/100nm NMOS transistor by sweeping gate source voltage (V_{GS}), while drain source voltage (V_{DS}) of NMOS transistor is constant. This figure indicates that g_m' of the NMOS transistor is positive in all sweeping voltage and g_m''

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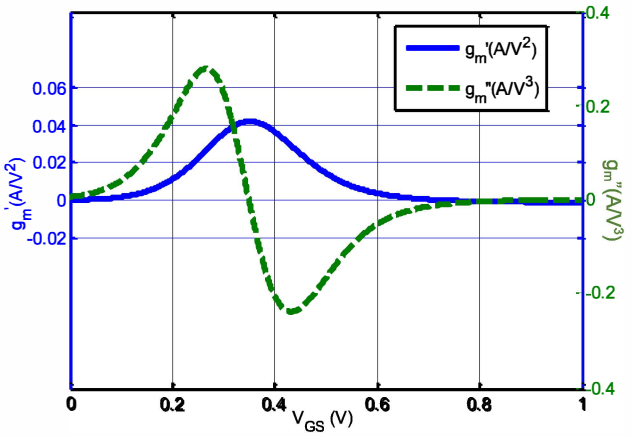

Figure 1. g_m' and g_m'' of the NMOS transistor with (W/L=10µm/0.1µm).

is positive and negative at the small and large gate-source voltage, respectively. By suppressing second and third order nonlinearity of the transistor, the linearity of the mixer improves and IIP2 and IIP3 of the mixer increase, subsequently.

Fig. 2 shows the transconductance stage of the proposed mixer. This structure is a common gate pseudo differential topology that M_1 and M_2 transistors at the input stage convert RF voltage to current which this current is proportional to the transconductance of the input transistors. Also, M_1 and M_2 transistors can be used as input matching network since the impedance looking into the source is about $1/g_{m1,\ 2}$. The nonlinearities of M_1 and M_2 transistors can be cancel by creating second and third order nonlinearities equal to M_1 and M_2. These nonlinearities are produced by using M_5-M_8 transistors. So, linear currents appear at the switching stage that comes from M_3 and M_4 transistors. In addition, M_9 and M_{10} transistors is used to enhance gain of the input stage by decreasing current and subsequently G_m of the M_3-M_6 transistors. A detailed design analysis of the linearity of the proposed mixer is provided at the following section.

B. *Second and Third Order Nonlinearity Cancellation Analysis*

Fig. 3 illustrates the small- signal equivalent half circuit of the proposed mixer. In this design a new path consist of M_5 and M_7 transistors is used to cancel second and third order nonlinearity of the input transistor. In addition transistor M_9 at drain of the input transistor decreases current of the M_3 and M_5 transistors to create linearity condition. Taylor series expansion Demonstrate this expression.

The small-signal drain current of M_1 transistor can be expressed by Taylor series expansion as follows:

$$i_1 = g_{m1}(-v_1) + g_{m1}'(-v_1)^2 + g_{m1}''(-v_1)^3 \quad (2)$$

The current of M_5 transistor similar to i_1 is obtained by:

$$i_2 = g_{m5}(-v_2) + g_{m5}'(-v_2)^2 + g_{m5}''(-v_2)^3 \quad (3)$$

Linear gain from v_1 to v_2 can be obtained easily as follows:

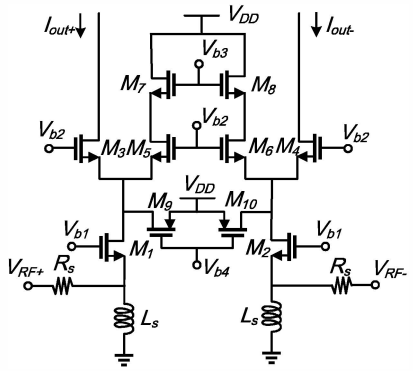

Figure 2. Transconductance stage of the proposed mixer.

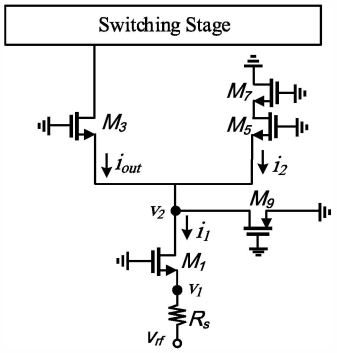

Figure 3. Small- signal equivalent half circuit of the transconductance stage.

$$v_2 = \frac{g_{m1}}{g_{m3} + g_{m5}} v_1 \equiv \alpha v_1 \quad (4)$$

Equation (4) reveals that this gain can be greater than one if $g_{m1} > g_{m3}+g_{m5}$. Because G_m of transistor is proportional to drain current of transistor, therefore M_9 transistor is employed to decrease current and subsequently G_m of the M_3 and M_5 transistors. So, α *can* become greater than one.

Thus, the output current is obtained as follows:

$$i_{out} = i_1 - i_2 = -(g_{m1} - \alpha g_{m5})v_1 + (g_{m1}' - \alpha^2 g_{m5}')v_1^2 - (g_{m1}'' - \alpha^3 g_{m5}'')v_1^3 \quad (5)$$

From equation (5), equivalent G_m of the proposed mixer is achieved by (6). Also to enhance IIP3, the coefficient of v_1^3 must be zero, therefore IIP3 enhancement condition is obtained by equation (7).

$$G_m = -(g_{m1} - \alpha g_{m5}) \quad (6)$$

$$g_{m1}'' = \alpha^3 g_{m5}'' \quad (7)$$

Since, by using this structure, the equivalent G_m of the mixer which is obtained by (6) decreases and the conversion gain of the mixer which is achieved by (8) reduces, subsequently. Thus the coefficient of α must be large enough to lead α^3 becomes large. So, the linearity condition with smaller g_{m5} is established in order that equivalent G_m of the proposed mixer dose not

decrease more. In this design, α is considered approximately 2 to make linearity condition.

$$CG = \frac{2}{\pi} G_m R_L \tag{8}$$

In differential Gilbert mixer even order nonlinearities at the IF stage will be deleted, but in the presence of a mismatch between the transistors, some of even order nonlinearities appear at the IF stage. Therefore, the IIP2 of the mixer reduces. According to equation (5) in the proposed mixer the coefficient of the v_1^2 at the output current is reduced, because g_m' of the M_1 and M_5 transistors are positive at the all V_{gs} voltage. So, it is expected that the IIP2 of the proposed mixer increases compared to the conventional mixer.

III. COMPLETE CIRCUIT OF THE PROPOSED MIXER WITH CONSTANT G_M BIAS CIRCUIT

The complete circuit of proposed mixer is illustrated in Fig.4. Transconductance stage of proposed mixer consists of $M_{1\text{-}10}$ transistors, $M_{sw1\text{-}sw4}$ transistors are switching stage and R_L and C_L are IF stage. The mixer bandwidth can be affected by the output capacitance from M_3 and M_4 transistors and switching pairs. Therefore inductors L_{pk} can be used for bandwidth extension. The value of this inductor is obtained as follows [9]:

$$L_{pk} = \frac{\left(\frac{1}{g_{msw1,2}} \| \frac{1}{g_{msw3,4}}\right)^2 C_p}{1.41} \tag{9}$$

Where C_p is equivalent capacitance at the output of the transconductance stage and input of the switching stage.

To create bias voltage for proposed transconductance stage that shown in Fig. 5, a low voltage cascode constant transconductance (G_m) bias circuit is designed in order to improve the robustness of the proposed mixer against process, voltage and temperature (PVT) variations. Transistors M_{b1}-M_{b4} with R_T resistance make the conventional constant G_m bias circuit where transistor M_{b2} is a factor K times wider than M_{b1} and M_{b3} is equal to M_{b4}.

To apply constant G_m bias circuit to proposed mixer, this topology is combined with low voltage current mirror structure to create bias voltages that is required. For constant G_m bias circuit a startup circuit is required that it is implemented by M_{s1}, M_{s2} and M_{s3} transistors. Also, to eliminate noise of bias circuit, it used from MOS capacitance at the bias voltage nodes.

IV. POST LAYOUT SIMULATION RESULTS

In order to verify the validity of the proposed design, post layout simulation results by using a 90nm RF-CMOS process with Spectre-RF are provided. Also, a conventional pseudo differential common gate mixer (Fig. 6) is designed and simulated to provide a fair comparison. The proposed mixer is designed for 1 GHz to 5 GHz RF signal frequency and 20 MHz IF band-width. Also, a local oscillator drive the switching pair with 3.5 dBm power. The IIP2 and IIP3 simulated by applying a two-tone test with 5 MHz spacing. Layout of the proposed mixer

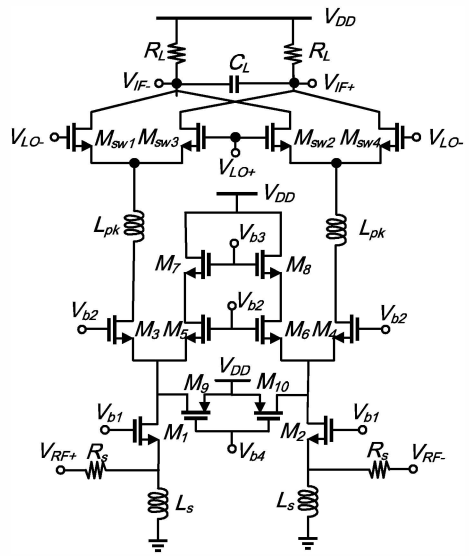

Figure 4. Complete schematic of the proposed mixer.

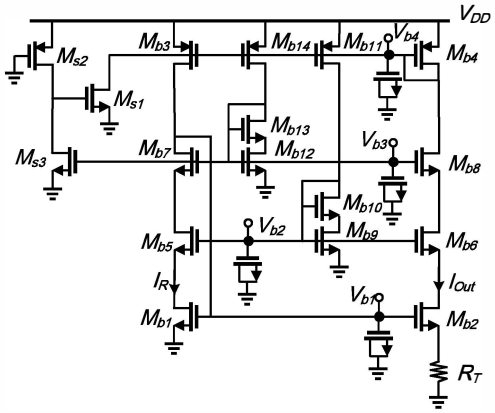

Figure 5. Constant G_m bias circuit of the proposed mixer.

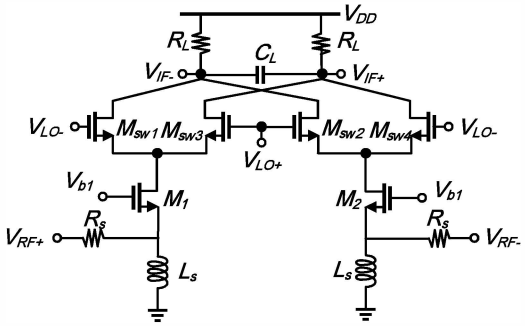

Figure 6. Conventional mixer.

and bias circuit is shown in Fig. 7 which occupies 835 µm × 642 µm silicon die area. The following results are related to the post layout simulations. The simulated IIP3 of the proposed and conventional mixers versus RF frequency is shown in Fig. 8. This figure shows that the proposed mixer has +9.9 dBm IIP3 in average that is improved ~5.8 dB compared to the conventional

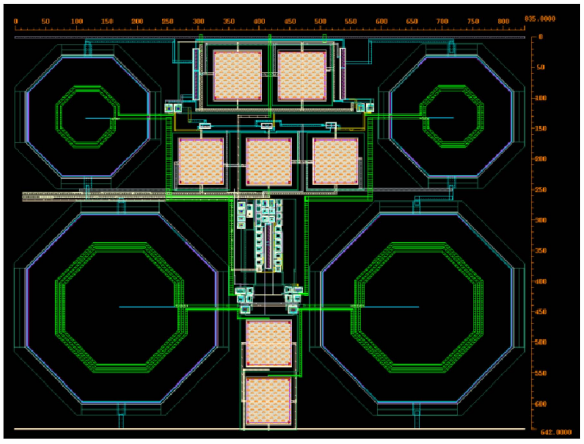

Figure 7. Layout of the proposed mixer.

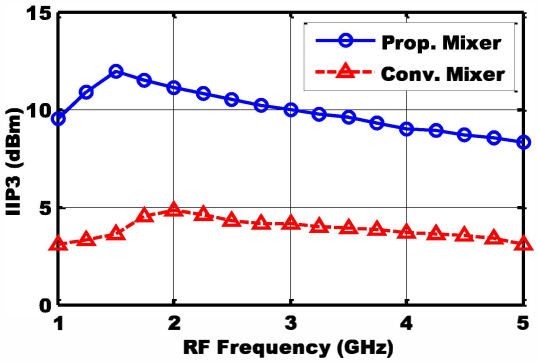

Figure 8. IIP3 of the proposed mixer versus RF frequency.

mixer. The simulated conversion gain of the proposed and conventional mixer versus RF frequency are shown in Fig. 9. This figure indicates that the conversion gain of the proposed mixer is improved about 2.9 dB compared to the conventional mixer since, DC current of the switching stage and also load stage decrease by M_9 and M_{10} transistors and load resistance can be selected larger than conventional mixer. In addition the noise figure of the proposed and conventional mixer versus IF frequency and RF frequency are shown in Fig. 10 and Fig. 11, respectively. Fig. 10 indicates that the flicker noise of the proposed mixer decreases because, M_9 and M_{10} transistors operate similar to current bleeding [10] topology. Also, Fig. 11 shows that the noise figure of the proposed mixer is deteriorated about 0.9 dB in average compared to the conventional mixer. Finally, IIP2 of the proposed mixer is illustrated in Fig. 12 that represents 6 dB improvement in average compared to the conventional one.

The post layout simulation results of the proposed mixer for different process corner cases and temperature variations are summarized in Table I. The simulation results show that the proposed mixer has small variation in corner cases because of using constant G_m bias circuit.

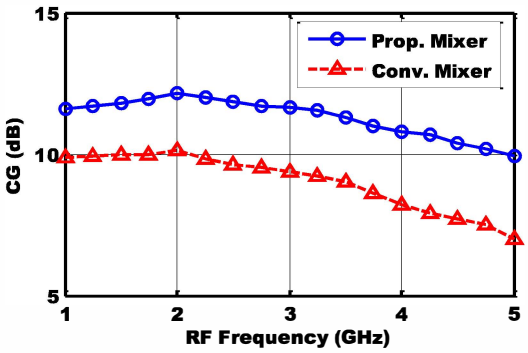

Figure 9. CG of the proposed mixer versus RF frequency.

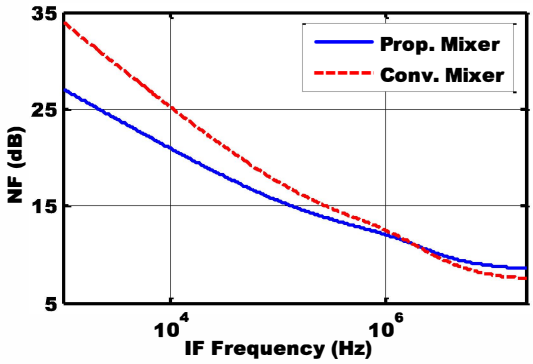

Figure 10. NF of the proposed mixer versus IF frequency at 3 GHz.

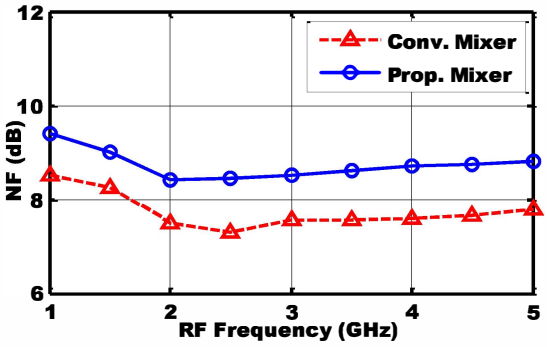

Figure 11. NF of the proposed mixer versus RF frequency.

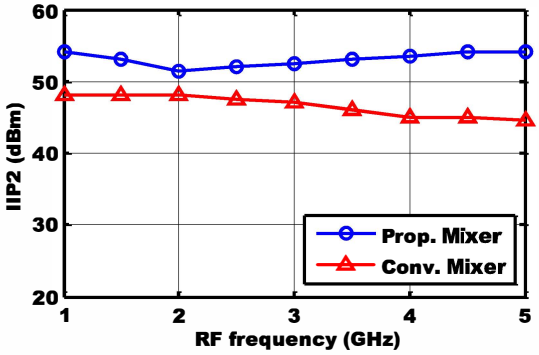

Figure 12. IIP2 of the proposed mixer versus RF frequency.

TABLE I. SIMULATTION RESULTS OF THE PROPOSED MIXER IN CORNER CASES.

Corner cases	*IIP3 (dBm)*	*IIP2 (dBm)*	*NF (dB)*	*CG (dB)*	*Power (mW)*
TT @ 27 ºC	9.9	53	8.6	11.1	8.65
FF @ -40 ºC	9.3	51.4	8.2	11.7	9.3
SS @ 85 ºC	10.2	54.8	8.9	10.4	7.9

Table II summarizes the simulation results of the proposed and conventional mixer and several previously reported linearization works [11], [12], [13], [14], [15] by using the following figure-of-merit [11]:

$$FOM = \frac{BW\,(GHz).Gain(lin).IIP3(mW)}{P_{dc}\,(mW).[F_{DSB}\,(lin)-1]} \qquad (10)$$

Where F_{DSB} is double side band noise figure of the mixer, BW represents the -3 dB bandwidth, IIP3 denotes the average third input intercept point, Gain represents the conversion gain and P_{dc} is the power consumption.

As it is seen from Table II, by using the proposed mixer structure an excellent FOM is achieved compared to the conventional and previously reported WB mixers listed in Table II.

TABLE II. PERFORMANCE COMPARISON OF THE PROPOSED MIXER WITH SEVERAL RECENTLY REPORTED WORKS.

Param	*Prop**	*Conv&*	*[14]*	*[15]*	*[16]*	*[17]**	*[18]**
Freq. (GHz)	1~5	1~5	0.5~5.8	0.85~1.8	0.8~2.1	0.045~2.5	2~5
IIP3 (dBm)	+9.9	+4.1	2.5#	3.7~5.3	15	0.6~7.2	-10.5
IIP2 (dBm)	53	47	N/A	55~75	N/A	N/A	N/A
CG (dB)	11.1	8.2	15#	7.2~9.3	3~5	5.8~8.6	16.8
NF (dB)	8.6	7.7	4.2	5.8	15.4	7.4-9.7	6
Pow. (mW)	8.65	7.84	25.5	1.92	65	16.4	2.1
Supp. (V)	1	1	1.5	1.2	2.5	1.8	1.8
Tech. (nm)	90	90	130	110	130	180	180
FOM	9.3	1.75	7	3.3	0.05	0.3	2.05

* Post Layout Simulation Results & Pre Layout Simulation Results # Measurement results at 5 GHz

V. CONCLUSIONS

In this paper, a wide band linearized active mixer introduced in a 90 nm RF-CMOS technology. In order to enhance the linearity, an auxiliary path is used to cancel second and third order nonlinearity of the main path. In addition a constant G_m bias circuit is employed to improve the robustness of the proposed structure against process, voltage and temperature. The mixer is designed for 1-5 GHz which the IIP2 and IIP3 of the proposed mixer improved are about 6 and 5.8 dB respectively, compared to the conventional one. Also, the conversion gain and flicker noise of the proposed mixer are improved and thermal noise increases about 0.9 dB compared to the conventional mixer. Power consumption of the proposed mixer is 8.65 mW from a 1 volt supply.

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