A Systematic Design Procedure for CMOS Three-Stage NMC Amplifiers

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Abstract— **This paper presents a new time-domain design procedure for CMOS three stage amplifiers with nested Miller compensation. The optimal design issues of power dissipation are considered to achieve the lowest power consumption while satisfying the required design specifications such as the dc gain, settling time, and noise budget. These parameters are critical for switched-capacitor applications. HSPICE simulation results are provided for a three-stage single-ended class A amplifier to verify the efficiency of the proposed design technique.**

Keywords: Three-Stage Amplifiers, Nested Miller Compensation

I. INTRODUCTION

Multistage amplifiers are widely used in the analog and mixed signal circuits to achieve high dc gain and large output signal swing simultaneously, because, although the cascoding of transistors is a well-known means to increase the dc gain of the single-stage amplifiers, however, this is not possible in the recent sub-micron CMOS technologies due to the reduced power supply voltage dictated by the technology scaling. Nonetheless, multistage amplifiers have additional frequency poles and zeros resulting in inherent instability and reduced signal bandwidth if any frequency compensation technique is not employed. Therefore, a frequency compensation technique is needed to design stable three-stage amplifiers [1].

Nested Miller compensation (NMC) is one of the well known techniques which is suitable for three stage amplifiers. In this technique, two compensation capacitors are used. The first capacitor is connected between the first and third stages, and the other capacitor is connected between the second and third stages. The concept of this technique is the pole splitting. In this way, there are two poles. One of them moves toward the origin and another is placed in much higher frequencies. So, a higher phase margin is achieved, however, this solution results in the bandwidth and slew rate reduction [1].

To design three stage NMC amplifiers many design procedures have been reported which are basically using the frequency domain equations such as the phase margin and gain bandwidth [2-6]. On the other hand, there are some design procedures which are basically using the time domain equations, but, in this type, they only design the size of the compensation capacitors and they don't report any equations about the transconductances, currents, and transistor sizes [7, 8].

In this paper, a new time domain design procedure for three stage amplifiers with NMC frequency compensation is presented which considers almost all of the amplifier's design parameters and achieves the transistors' transconductances, bias currents, and aspect ratios. Besides, the minimum required power consumption for the specific settling time and the noise budget is considered. The proposed design technique employs the same design methodology presented in [9] for two-stage cascode compensated operational amplifiers and extends that for three stage NMC amplifiers. Besides our proposed design procedure is suitable for switched-capacitor applications where we need an exact control on time domain parameters.

This paper is organized as follows. In Sect. II the proposed design procedure is presented. Section III provides the design example and simulation results. Section IV concludes the paper.

II. PROPOSED DESIGN PROCEDURE

Figure 1 shows the typical and basic schematic of a three stage NMC amplifier where M1-M5, M6-M9 and M10-M11 constitute the first, second, and third stages, respectively. C_{C1} and C_{C2} are the compensation capacitors. The proposed design procedure for this amplifier is presented as follows. It is worth mentioning that this topology was selected as a test bench and the proposed design method can easily be used in other implementations of NMC amplifiers as well.
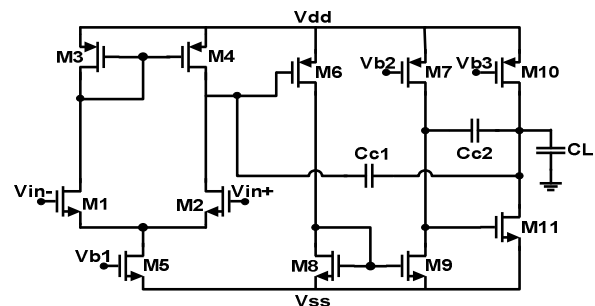

Fig 1: Typical schematic of a three-stage NMC amplifier.

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A. Closed Loop Analysis of an NMC Amplifier

In small signal analysis, the effect of parasitic capacitances is neglected since they are generally very smaller than the compensation capacitors. Under these assumptions, the closed loop unity feedback transfer function of the circuit shown in Fig. 1 is expressed by [8]:

$$A_{close}(s) = \frac{1 - s\dfrac{C_{C2}}{g_{m3}} - s^2\dfrac{C_{C1}C_L}{g_{m2}g_{m3}}}{1 + \left(\dfrac{C_{C1}}{g_{m1}} - \dfrac{C_{C2}}{g_{m3}}\right)s + \left[\dfrac{C_{C1}C_{C2}(g_{m3}-g_{m2}-g_{m1})}{g_{m1}g_{m2}g_{m3}}\right]s^2 + \dfrac{C_{C1}C_{C2}C_L}{g_{m1}g_{m2}g_{m3}}s^3} \tag{1}$$

where g_{mi} is the ith-stage transconductance. Since, in many applications such as the heavily capacitive load conditions g_{m3} is much greater than g_{m1} and g_{m2}, the zeros are located at much higher frequencies than the unity gain bandwidth. So, the effect of the zeros on both phase margin and loop gain magnitude can be neglected [5]. Therefore, we will neglect the effect of zeros in the closed loop transfer function.

B. Settling of a Standard Third Order System

Since the order of the closed loop system transfer function is three, so, a third order standard system is considered to investigate the settling behavior rather than considering the closed loop transfer function by itself [9]. Equation (2) shows the standard third order system:

$$H(s) = \frac{k}{(s+\alpha\zeta\omega_n)(s^2+2\zeta\omega_n s+\omega_n^2)} \tag{2}$$

As is seen there are three system parameters, α, ζ, and ω_n in the transfer function. ω_n and ζ are called the natural frequency and damping factor, respectively.

The settling time error in definite time period of t_{ss} defined as $\varepsilon(s) = \dfrac{s(\infty)-s(t_{ss})}{s(\infty)}$ is given by:

$$\varepsilon_s = \frac{1}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)} \times e^{-\alpha\zeta\omega_n t_{ss}}$$
$$+ \frac{\alpha\zeta e^{-\zeta\omega_n t_{ss}}}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)}(-2\zeta+\alpha\zeta)Cos\left(\omega_n t_{ss}\sqrt{1-\zeta^2}\right) \tag{3}$$
$$+ \frac{\alpha\zeta e^{-\zeta\omega_n t_{ss}}}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)}\frac{(1-2\zeta^2+\alpha\zeta^2)}{\sqrt{1-\zeta^2}}Sin\left(\omega_n t_{ss}\sqrt{1-\zeta^2}\right)$$

where $s(t)$ is the step response. This equation is very complex to analytically obtain the value of system parameters, α, ζ, and ω_n, for a specific settling error in a definite time, t_{ss}. So, we have to use the graphical or numerical calculations. Also, the value of the system parameters is very important because they affect the system total power consumption [9]. In other words, for a specific value of α and ζ we must choose the minimum possible value for ω_n to achieve the minimum possible power dissipation.

C. Choosing the Values of α, ζ, and ω_n

For a specific settling error, the value of ζ in which the value of $\omega_n t_{ss}$ is minimized, is an optimum value because it results in the narrowest required bandwidth [10].

If α is decreased, it makes clear sense from equation (2) that the amplifier would be less sensitive to changes in the pole positions because the step response behavior of this system is similar to a single pole response. This represents a trade-off between optimal linear settling which minimizes $\omega_n t_{ss}$ and robust design because decreasing α, increases the required $\omega_n t_{ss}$. A good approximation is to set α in the range of 0.8 to 0.9 which results in less sensitivity to the pole positions but does not excessively increase the amplifier bandwidth and cost too much power [10].

All things considered, for a definite settling error level, we plot the equation (3) with the above-mentioned specific range for α and ζ. Then, to minimize the power consumption a point which has a minimum value of $\omega_n t_{ss}$ is selected. To minimize the value of $\omega_n t_{ss}$, we can use genetic algorithm toolbox in MATLAB or minimize function in MATHEMATICA. For instance as shown in Fig. 2, for -60 dB settling error, the system parameters of $\alpha = 0.9$, $\zeta = 0.84$ and $\omega_n t_{ss} = 10.3$, are obtained.
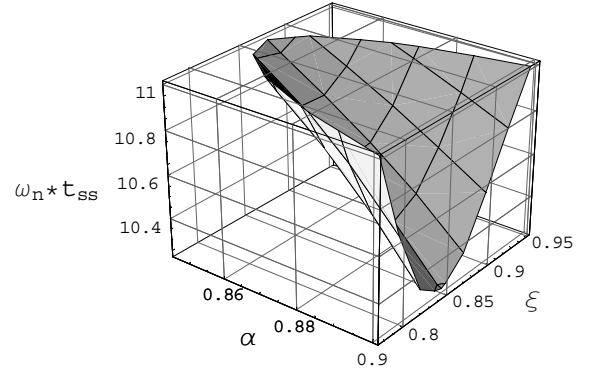

Fig. 2: Plot of equation (3) with -60-dB settling error level.

Having known the system parameters for a specific settling error in a defined time and the amplifier closed loop transfer function given in (1), the device parameters are given by:

$$\frac{g_{m3}-g_{m2}-g_{m1}}{C_L} = 2\zeta\omega_n + \alpha\zeta\omega_n \tag{4}$$

$$\frac{(-C_{C2}\times g_{m1}+C_{C1}\times g_{m3})g_{m2}}{C_{C1}C_{C2}C_l} = \omega_n^2 + 2\alpha\zeta^2\omega_n^2 \tag{5}$$

$$\frac{g_{m3}\times g_{m2}\times g_{m1}}{C_{C1}C_{C2}C_l} = \alpha\zeta\omega_n^3 \tag{6}$$

In these equations, two of system parameters, α and ζ, are known. The value of ω_n is not known. However the value of $\omega_n t_{ss}$ is known. The optimal value of linear settling time, t_{ss}, is obtained in the next subsections to determine the value of ω_n efficiently.

D. Calculation of Compensation Capacitors

The compensation capacitors can be calculated due to the circuit noise considerations. For calculation of total input-

referred thermal noise, we neglect the noise of second and third stages because the input noise from the first stage is much greater than the second and third stages contribution. Hence, the total input referred noise power of the amplifier shown in Fig. 1 is given by:

$$S_{N,input} = 2\times 4kT \times \frac{2}{3} \times \frac{1}{C_{C1}} \left(1+\frac{g_{m3}}{g_{m1}}\right)\left(\frac{(1+2\alpha\zeta^2)}{\alpha\zeta\omega_n}\right) \quad (7)$$

The value of C_{C1} is obtained in such a way to achieve the required noise budget. Note that the value of ω_n and C_{C2} will be determined in the next subsections.

E. Optimization of the Bias Current

The total settling time of an opamp consists of two distinct regions. The first region is nonlinear settling in which the input signal amplitude is large and some of transistors may turn off. The second region is linear settling in which the behavior of an opamp obeys the small signal relation. The nonlinear settling region describes by a quantity called slew rate and its relations for the circuit shown in Figure 1 are as follows [6]:

$$SR = \min\{SR_1, SR_2, SR_3\} \quad (8)$$

$$SR_1 = \frac{2I_{DS1}}{C_{C1}}, SR_2 = \frac{2I_{DS9}}{C_{C2}}, SR_3 = \frac{I_{DS10}-2I_{DS9}-2I_{DS1}}{C_L} \quad (9)$$

To minimize the dc current consumption we set all three relations for slew rate to be equal [2], i.e.:

$$SR_1 = SR_2 = SR_3 = SR_{min} \quad (10)$$

Another assumption for minimizing the power dissipation and optimizing the bias current is considered as follows: the current of input transistor M1 is chosen equal with the value obtained from the slewing relation [9], i.e.:

$$I_{DS1} = 0.5C_{C1}\times SR_1 = 0.5C_{C1}\times \frac{V_{FS}}{t_{ls}} = 0.5g_{m1}v_{eff1} \quad (11)$$

$$t_s = t_{ls} + t_{ss} \quad (12)$$

where V_{FS} is the differential output step t_{ss}, t_{ls} are the linear and nonlinear settling times, respectively.

The transconductance of input transistor M1 can be obtained from equations (4-6) and hence is given by:

$$g_{m1} = \frac{\alpha\zeta\omega_n t_{ss}}{(1+2\alpha\zeta^2)}\times C_{C1}\times \frac{1}{t_{ss}} \quad (13)$$

So, the optimal bias current of input transistors and also the optimal linear settling time are obtained as follows:

$$I_{DS1,opt} = \frac{1}{2t_s}C_{C1}\left(V_{FS} + \frac{\alpha\zeta\omega_n t_{ss}}{(1+2\alpha\zeta^2)}\times v_{eff1}\right) \quad (14)$$

$$t_{ss} = \frac{\alpha\zeta\omega_n t_{ss}\times v_{eff1}}{\alpha\zeta\omega_n t_{ss}v_{eff1}+V_{fs}(1+2\alpha\zeta^2)}\times t_s \quad (15)$$

According to equation (14), the value of $I_{DS1,opt}$ is obtained. Then, according to equation (9) the value of slew

rate is obtained. Finally, we can obtain the optimum current values of the second and third stages. From previous equations and simplified denominator of closed loop transfer function, we can rewrite the equations (4-6) and find the value of g_{m1} and g_{m3} as:

$$g_{m1} = \frac{\alpha\zeta\omega_n}{(1+2\alpha\zeta^2)}\times C_{C1} \quad (16)$$

$$g_{m3} = \zeta\times\omega_n\times(2+\alpha)\times C_L \quad (17)$$

The value of g_{m2} is not important by itself because, from the simplified closed loop transfer function, it is clear that the ratio of g_{m2} to C_{C2} determines the system parameters. So, for choosing a value for g_{m2}, we have several tradeoffs among area, gain, and slew rate. We choose the value of g_{m2} to be equal to g_{m1} [2].

$$g_{m2} = g_{m1} \quad (18)$$

According to denominator of equation (1) the value of C_{C2} is obtained as follows:

$$C_{C2} = \frac{(2+\alpha)\times\zeta}{(1+2\alpha\xi^2)\times\omega_n}\times g_{m2} \quad (19)$$

After all these steps we can find good initial points for opamp's parameters. Then, a circuit simulator can be used to drive these specifications. The gain of amplifier can be modified by tuning the transistors sizes in this level. In the next section, we test the proposed design procedure to show the accuracy of this method and robustness of designed amplifier at different conditions.

III. DESIGN EXAMPLE AND SIMULATION RESULTS

To show the usefulness of the proposed design procedure, the NMC amplifier shown in Fig. 1 was designed and simulated using a 0.18-μm BSIM3v3 level 49 mixed-signal CMOS models with HSPICE. The design is targeted for realization of an amplifier with the specifications shown in Table I.

To get 0.1% or -60-dB settling error, the system parameters are obtained using Fig. 2 as $\alpha = 0.9, \zeta = 0.84, \omega_n t_{ss} = 10.3$. The compensation capacitor C_{C1} is chosen 40-pF from noise consideration. Table II shows the derived system parameters using the proposed design equations.

Table I: Design parameters.

Parameter	value
Settling accuracy	-60-dB
Input referred noise	$14nV/\sqrt{HZ}$
Maximum differential output signal step(VFS)	0.2 Volt
Settling time	$1.5\times 10^{-6} s$
Power supply voltage	$1.5 - Volt$
Load capacitor	100-pF
Technology	0.18 μm

Table II: calculated and simulated device size.

Parameter	Calculation		Simulation	
	(W/L)	$g_m(\mu A/V)$	(W/L)	$g_m(\mu A/V)$
M1,M2	2	118	0.4/0.18	116.5
M3,M4	3.3	85	0.6/0.18	80
M6,M7	7.5	85	1.4/0.18	89
M8,M9	3.5	118	0.65/0.18	112
M5	3.6	250	0.65/0.18	280
M10	125	1500	22.5/0.18	1754
M11	69	2160	12.5/0.18	1987
C_{C1} (pF)	40			
C_{C2} (pF)	14.7			

The designed amplifier was simulated with HSPICE with the device parameters shown in Table II. Table III shows the simulation results in three process corner cases as well as considering the temperature variations. In Table IV the magnitude of designed capacitors and transconductances were shifted by amount of ±10% and then the specifications were measured to show the robustness of the designed amplifier to the variation of the parameters.

Table III: Simulation results.

Parameter	TT @ 25	SS @ 85	FF@ -40
Gain(dB)	94.1	93.2	95.4
$f_t(kHz)$	451	375	570
$SR+/-(V/\mu s)$	0.138/0.204	0.117/0.140	0.166/0.172
Phase margin (degree)	67	70	65
$T_s+/-(\mu s)$	1.44/0.98	1.7/1.42	1.2/1.16
Noise($nV/\sqrt{Hz}$)	16	20	12
Power consumption(μW)	425	423	427

Figure 4 shows the transient response of the simulated amplifier. The frequency response of the amplifier in three process corner cases is depicted in Fig. 5. The final simulated device values are also shown in Table II. As is seen the proposed design technique gives a good initial design point and the circuit level simulations can be used to further optimize the design parameters only with a few iterations.

Table IV: Results of shift in designed parameters

	Gain(dB)	f_t(kHz)	T_s +/-(μs)	Phase margin
-10%	95.2	476	1.23/0.82	66º
+10%	93.8	430	1.57/1.15	69º

IV. CONCLUSIONS

In this paper a novel time domain design methodology for three stage NMC amplifiers was proposed. The proposed design procedure gives the whole circuit parameters such as the transconductance and aspect ratio of transistors, compensation capacitors, and bias currents for a specific settling error in a definite time period by minimizing the power dissipation. This method helps IC designers to have a valuable control on time domain specifications.
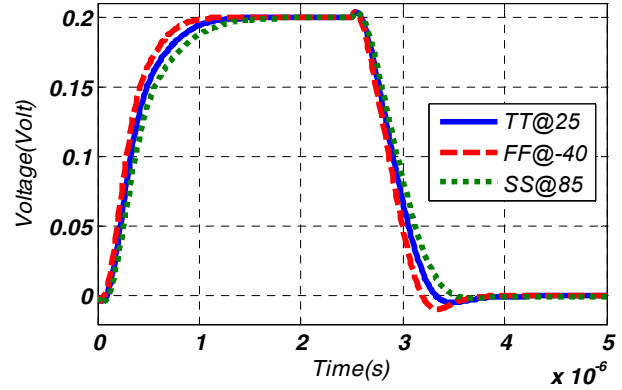

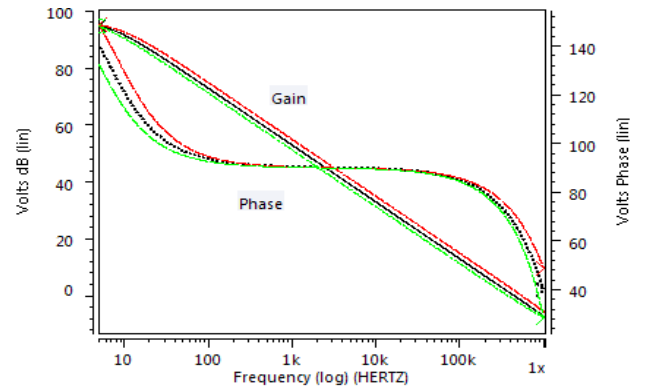**Fig. 4:** Settling simulation results.

Fig. 5: Simulated frequency response in three corner cases.

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