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A highly linear wideband balun-LNA with symmetrical loads

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***Abstract*— This paper presents a novel structure on balun-LNAs which has differential outputs with symmetrical loads without any need for current-bleeding circuit. The proposed structure is based on the CG-CS cascode LNA with identical transconductances for the CG and CS stages using a positive feedback for input matching compensation. This paper also introduces a new linearity improvement method based on the mixture of post distortion and superposition techniques to utilize the positive points of both of them, which are no effect on input matching and low power consumption. This novel method, despite other linearity improvement techniques, not only does not decrease the voltage gain but also improves it without any considerable increase in power consumption and any effect on input matching. The proposed LNA structure is designed in 65 nm CMOS technology and covers the frequency range of 0.07-1.7 GHz. It has symmetrical loads with a differential voltage gain of 15.3 dB, a minimum NF of 2.65 dB, and IIP3 of +2.75 dBm with power consumption of 12.35 m watt.**

***Keywords*: balun-LNA, positive feedback, linearity improvement, symmetrical loads.**

I. INTRODUCTION

Low-noise amplifier (LNA) is the first block of wireless receivers, which is needed to amplify the signal receiving from the antenna without adding much noise to it. LNAs should also provide good input matching, sufficient and flat gain, high linearity, and low NF over the desired bandwidth. Among different LNAs, balun-LNAs have become more demanding during the past decades since they provide differential outputs, which leads to have higher common-mode rejection ratio (CMRR) and lower second-order distortion, without any need for a passive balun that has loss and takes up a large space increasing the costs.

In recent studies, several broadband active-balun LNAs have been reported. Fig.1(a) shows the basic CG-CS balun-LNA in which the CG transistor provides the input matching, and the CS transistor cancels the noise and distortion generated by the CG transistor while providing the differential outputs [1]. For decreasing the NF of the balun-LNA, the noise of the CS transistor is needed to be decreased since the NF in this structure is almost limited by the CS transistor. By increasing the size and the transconductance of the CS transistor, its noise will be diminished to a good amount. Fig.1 (b) shows the proposed structure in [2] in which the size of the CS transistor is N times higher than that of the CG transistor, so the NF is decreased compared to [1].

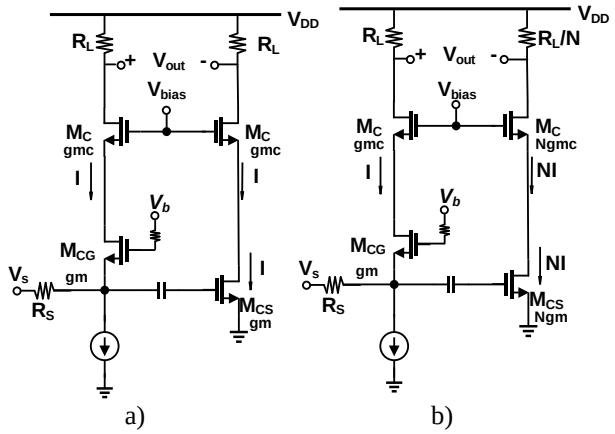

Fig. 1: CG-CS Balun-LNAs: (a) conventional topology with $g_{m,CS} = g_{m,CG}$, $R_{CS} = R_{CG}$ and $I_{CS} = I_{CG}$, (b) practical topology with $g_{m,CS} = Ng_{m,CG}$, $R_{CS} = R_{CG}/N$ and $I_{CS} = N\,I_{CG}$.

For having differential outputs in this structure, the load resistor in CS stage should be N times smaller than that of the load resistor of the CG stage which leads to a mismatch in phase and gain of the differential outputs, increasing the second-order distortion and makes the noise-cancellation less perfect. In [3] a balun-LNA with balanced loads is introduced. In this structure, a modified current-bleeding technique is employed to enable the balun-LNA to have the same current in differential outputs. As a result, the balun-LNA can have differential outputs with symmetrical loads and without any phase or gain imbalances. For modifying the structure in [3], [4] utilizes a local feedback to decrease the power consumption. In [5] a new current-bleeding circuit is proposed, which consist of PMOS transistors instead of NMOS transistors. Another local feedback is also used in [6] and [7] between the CG and CS stage to boost the transconductance of the CG transistor and lower the power consumption, but these structures still have the gain and phase mismatches in differential outputs for having non-symmetrical load resistors. This brief introduces a balun-LNA with symmetrical loads without using any current-bleeding circuit. A new linearity technique is also introduced which improves IIP3 and voltage gain simultaneously without any considerable increase in power consumption since it works in weak-inversion region. This new method is

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based on two linearity improvement techniques of post distortion and superposition to utilize the positive points of both them, which are no effect on input matching and low power consumption. The rest of the paper is organized as follows. Section II describes the structure of the proposed balun-LNA in details. Section III provides a description on the circuit design and also post-layout simulation results, and finally, Section IV provides the conclusion.

II. Structure of The Proposed Balun-LNA

The schematic of the proposed LNA is depicted in Fig.2. The purpose of this structure is having symmetrical loads without using any additional current-bleeding circuit which controlling its current is challenging. For serving this purpose, current and transconductance of both CG and CS stages should be identical. Designing a balun-LNA in which the transconductance of the both CG and CS stages are the same is very challenging because on the one hand, for having low NF, the transconductance of the CS transistor should be high as mentioned in Sect. I, and one the other hand, the transconductance of the CG transistor is limited to 20 mS because of the input matching condition. For overcoming this challenge and satisfying this condition, this paper employs a positive feedback (M_F) to compensate for the input matching and allow the CG transistor to have a larger transconductanc. Under this condition, the transconductance of the both CG and CS transistors can be identical and high enough, in the meantime, to reduce the NF. As the result, differential outputs with symmetrical resistor loads would be achievable.

In Fig. 2, M_c is the cascode transistor for improving the input-output isolation. M_a is the auxiliary transistor, biased in weak-inversion region, for linearity improvement, which improves the voltage gain and 3-dB bandwidth of the balun-LNA at the same time with consuming negligible current. The details of linearity and gain improvement by this method is mentioned in Sect II.D, and finally L_B is an external RF chock which places the source of the CG transistor (M_{CG}) at dc ground. The details of the input impedance matching condition, the voltage gain, NF, and linearity of the proposed balun-LNA are presented in the following sections.

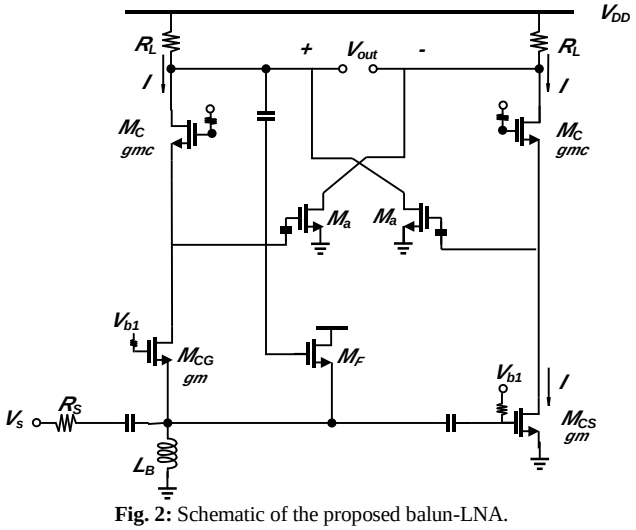

Fig. 2: Schematic of the proposed balun-LNA.

A. Input matching

We have the input impedance matching when

$$R_S = \frac{1}{g_{m,CG} - g_{m,F}(g_{m,CG}R_L - 1)} \quad (1)$$

Where R_S is the source impedance, $g_{m,CG}$ and $g_{m,F}$ are the transconductance of the CG and positive feedback (M_F) transistors, respectively, and R_L is the symmetrical load resistor. As it can be seen, adding the positive feedback transistor, adds another degree of freedom to the input matching condition allowing the CG transistor to have higher transconductance, which would be identical to the CS.

B. Voltage gain

Under the input matching condition and regardless of considering r_{ds} resistors, the differential voltage gain is obtained as

$$A_V = g_m\left(1+\frac{g_{m,a}}{g_{m,c}}\right)R_L \quad (2)$$

Where g_m is the transconductance of the CG and CS transistors that are the same, R_L is the load resistor, and $g_{m,a}$ and $g_{m,c}$ are the transconductance of M_a and M_c transistors. From the second term in (2), it can be concluded that the less the transconductance of the cascode transistor from the CG transistor, the higher the effect of M_a in increasing the voltage gain.

C. Noise

When the input impedance matching and differential output balance conditions are met, the noise generated by the CG transistor can be totally cancelled at the differential outputs. Moreover, the noise generated by cascode transistors is negligible because most of their noise is rotated in their loops and does not appear at the output. Therefore, the noise factor of the proposed balun-LNA is almost limited by the CS, positive feedback and load resistors and can be expressed as

$$NF = 1+\frac{\gamma}{g_m R_s}+\gamma g_{m,F}R_s+\frac{1}{g_m^{\,2}R_L R_s}+\frac{(1+g_m g_{m,F}R_L R_S)^2}{g_m^{\,2}R_L R_s} \quad (3)$$

The second and third terms of (3) stand for the thermal noise of M_{CS} and M_F respectively, and the fourth and fifth terms represent the thermal noise of R_L of the out^- and out^+ branches. It is noteworthy to mention that the noise of the R_L does not appear at the differential output identically because of the effect of the positive feedback transistor.

D. Linearity

The linearization technique introduced in this paper consists of a combination of two linearization methods, the post distortion technique and the derivative superposition method. In the idea presented in this paper, which is shown in Fig. 2, M_a auxiliary transistors are placed at the output of the main transistor, like the post distortion method, so as not to affect the input matching, while the working area of the auxiliary transistors is the weak inversion region, like the derivative superposition method, so that their bias current is

low and therefore has low power consumption. By using this novel linearization method, not only will we have the advantages of the both linearization methods (no effect on input matching, no reduction in voltage gain and low power consumption) at the same time, but in addition to improving linearity, we can improve voltage gain and the 3 dB bandwidth as well.

By using M_a auxiliary transistors for improving linearity and with considering third order equation for the current of transistors, i_{out^-} , which is the current of the *out*$^-$ branch, can be obtained as below, and the current of *out*$^+$ can also be obtained in the same way.

$$i_{out^-} = i_{CS} + i_{a,1} = g_m(1+\frac{g_{m,a}}{g_{m,c}})v_s + (g_m^{'} + \frac{g_{m,a}g_m^{'}}{g_{m,c}} + g_{m,a}^{'}\frac{g_m^2}{g_{m,c}^2})v_s^2 + \quad (4)$$

$$(g_m^{''}(1+\frac{g_{m,a}}{g_{m,c}}) + 2\frac{g_m g_{m,a}^{'} g_m^{'}}{g_{m,c}^2} + \frac{g_m^3}{g_{m,c}^3}g_{m,a}^{''})v_s^3$$

Where g_m is the transconductance, and g'$_m$ and g''$_m$ are the second-order and third-order nonlinearity coefficients of the CG and CS transistors. According to the above equation, by biasing the M_a transistor in the weak inversion region, the sign of $g_{m,a}$ will be positive, while the sign of g_m is negative , and as a result, it will be possible to place the third-order distortion at zero and improve IIP3 in this way. In addition, the first term of the above equation, which is the linear component of the current, shows that adding this auxiliary transistor, also helps to improve the voltage gain in addition to improving the third-order linearity.

III. Circuit Design and Simulation Results

This structure is designed for wideband transceivers covering the frequency range of 0.1-1.5 GHz. In the design of the CG, CS and positive feedback transistors it is considered to meet the input-matching condition and in the meantime having the lowest noise figure, with considering the limitation of power consumption and voltage-headroom. The size of the cascade trransistors is selected sixty percent less than that of the CG and CS transistors to increase the effect of M_a in gain improving, as it can be seen in (2). The size of the M_a is obtained from simulation for the highest improve in IIP3. It is also noteworthy to mention that the CG and CS transistors are biased via a current mirror circuit, and L_B is an off chip chock used for placing the source of the CG at dc ground. The circuit-level and post-layout simulations of the proposed balun-LNA were carried out with Spectre RF using a 65 nm RF-CMOS technology. Fig. 3 shows the layout of the proposed balun-LNA in Cadence 65 nm. It is noteworthy to mention that Poly resistors and MIM capacitors are used for resistors and capacitors, respectively. S_{11}, S_{21} and NF of the proposed LNA is depicted in Fig. 4. According to this figure, S_{11} is below −10 dB over the whole frequency range of 0.0.7-1.7 GHz, and the maximum S_{21} is 15.3 dB over this frequency bandwidth in the corner case of TT@27°C, with the supply voltage of V_{DD} and changes to 15.25 and 13.74 in the corner cases of SS and FF, in 85°C, 0.9 V_{DD} and -40°C, 1.1 V_{DD}, respectively. Moreover, it can be seen that the proposed LNA achieves a minimum NF of 2.65 dB across the whole bandwidth in the corner case of TT@27°C, supply voltage of V_{DD}, and changes to 3.02 and 2.2 in the corner cases of SS and FF, in 85°C, 0.9 V_{DD} and -40°C, 1.1 V_{DD}, respectively. Fig. 5 illustrates the stability factor K_f and Delta. Since K_f is larger than 1, and the magnitude of Delta is less than 1 over a frequency range three times larger than the desired bandwidth, it can be concluded that the proposed LNA is unconditionally stable.

Fig. 6 shows the simulated differential voltage gain of the proposed LNA before and after adding the auxiliary transistors (M_a). As it is clear, the proposed idea has improved the voltage gain and 3-dB bandwidth in the amount of 1 dB and 500 MHz in a 3 GHz bandwidth. Finally, Fig. 7 shows the simulated IIP3 before and after adding the auxiliary transistors (M_a) with the main RF tone at 1 GHz and with 10 MHz spacing. As it is seen, the proposed idea has improved IIP3 In the amount of 5.53 dB. Table 1 represents the post-layout simulation results of the proposed balun-LNA in the worst process corner cases and with the variation of the supply voltage. As it is clear, the proposed LNA is well robust against process, voltage, and temperature (PVT) variations. Table 2 represents a comparison between the proposed LNA and some of the previous wideband LNAs. According to Table 2, the proposed structure has a much higher linearity than the previous structures, with almost the same or even lower NF, and is the only balun-LNA with symmetrical loads that has positive IIP3, introduced so far. Compared to [3], [9], and [14] which are all balun-LNAs with balanced loads, the proposed balun-LNA has a higher BW, higher IIP3, and lower power consumption than [3] and [14] and about 6 dB higher IIP3 than [9]. Compared to [7] which has a positive IIP3, the proposed structure not only has the advantage of having balanced loads, but also a lower NF (about 1.5 dB). Compared to [11], which has positive IIP3 as well, the proposed LNA has a 5 dB higher gain with about 3 mW less power consumption. The following figure of merit (FoM) defined in [8] is used in Table 2 to have a better comparison.

$$FoM = \frac{S_{21}[abs]\times IIP3[mW]\times BW\ [GHz]}{(F-1)\times P_{dc}[mW]} \quad (5)$$

Where S_{21} is the maximum magnitude of power gain, BW is the bandwidth of the LNA (minimum between input-matching, 3-dB, and Noise bandwidth), F is the magnitude of the minimum NF over the entire bandwidth, and P_{dc} is the LNA's power consumption.

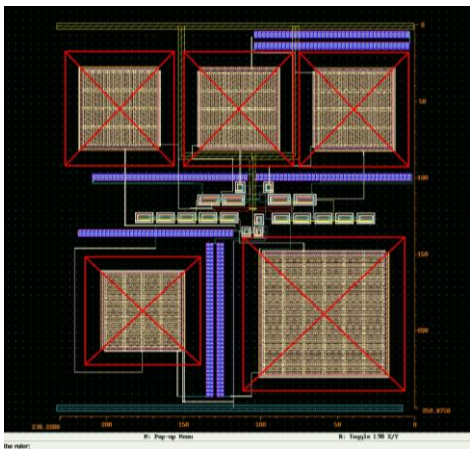

Fig. 3: Layout of the proposed balun-LNA.

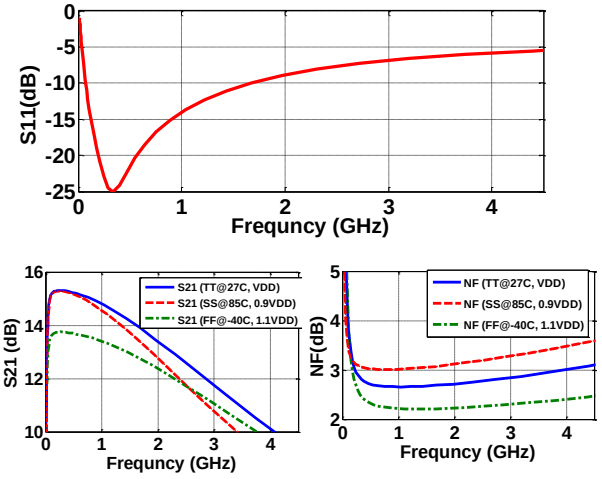

Fig. 4: Simulated S_{11}, S_{21} and NF of the proposed balun-LNA.

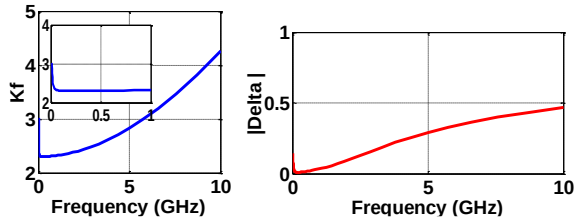

Fig. 5: Stability factors of K_f and Delta.

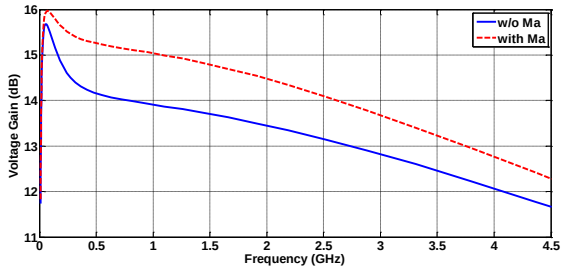

Fig. 6: Simulated differential voltage gain of the proposed balun-LNA before and after adding M_a.

Table 1: Corner case simulation results.

Corner Case	TT @ 27°C, V_{DD}	SS @ 85°C, 0.9 V_{DD}	FF @ -40°C, 1.1 V_{DD}
BW (GHz)	0.07-1.7	0.086-1.2	0.068-1.8

S11 (dB)	<-10	<-10	<-10
S21 (dB)	15.3	15.25	13.74
NF (dB)	2.65-3.5	3.02-3.5	2.20-3.5
IIP3 (dBm)	+2.75	-2.79	+6.71

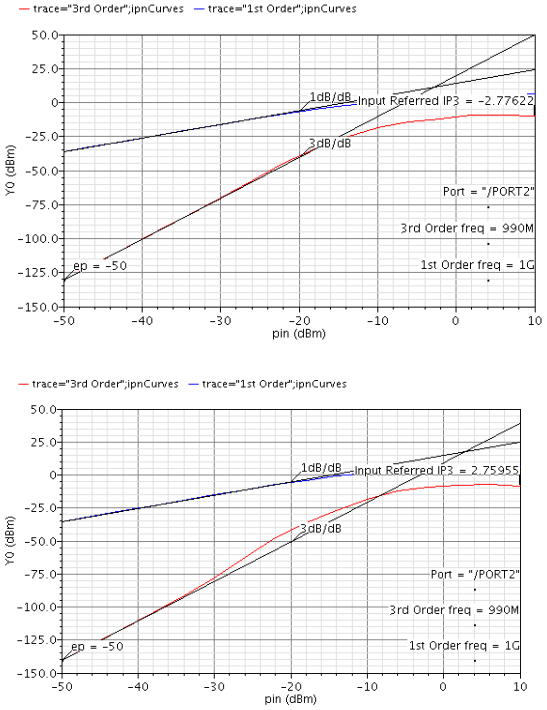

Fig. 7: IIP3 of the proposed balun-LNA before and after utilizing the proposed linearity improvement technique with 10 MHz spacing.

IV. CONCLUSION

In this paper, a new approach employing a positive feedback is introduced for balun-LNAs to have symmetrical loads without using any additional current-bleeding circuit. This paper also introduces a new linearity improvement technique, based on the post distortion and derivative superposition methods, which not only does not decrease the voltage gain, but helps to improve it and also modifies the 3 dB bandwidth of the LNA with consuming very low and even negligible power.

Table 2: Performance comparison.

Ref.	CMOS Process	BW (GHz)	S11 (dB)	S21(dB)	NFmin (dB)	IIP3(dBm)	Symmetric load	Balun function	Powe(mW)	FoM
[10]	65 nm	0.2-5.2	<-10	15.56	2.9	0	No	Yes	21	1.5
[3]	65 nm	0.05-1	<-10	30	2.3	-4.1	Yes	Yes	19.8	0.845
[7]	130 nm	0.1-2	<-9	16.6	4.15	+0.5	No	Yes	3	3
[8]	130 nm	2-7.6	<-10	13.8	1.85	-15.2	No	No	2.15	0.72
[9]	90 nm	0.8-6	<-10	20	2.5	-3.5	Yes	Yes	12.5	2.22
[10]	90 nm	2.5-4.5	<-10	21.2	4	-8	No	Yes	8	0.3
[11]*	90 nm	2.5-10.9	<-11	10.3	2.6	+10.4	Yes	No	15.6	21.4
[12]*	90 nm	0.05-10	<-11	13.4	2.8	-5	No	No	6	2.4
[13]*	130 nm	4.7-11.7	<-12	12.4	2.88	-3	No	No	13.5	2.06
[14]	180 nm	0.05-0.86	<-10	17	2.5	-0.5	Yes	Yes	30	0.21
[15]	180 nm	DC-1.4	<-10	16.4	3	-13.8	No	Yes	12.8	0.026
This Work**	65 nm	0.07-1.7	<-10	15.3	2.65-3.5	+2.75	Yes	Yes	12.35	2.4

*Schematic Simulation Results **Post-Layout Simulation Results

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