A Low Power Wideband Balun-LNA Employing Local Feedback, Modified Current-Bleeding Technique and Balanced Loads

Bahareh Shirmohammadi
Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran
Email: bahar_2660@aut.ac.ir

Mohammad Yavari
Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran
Email: myavari@aut.ac.ir

Abstract— In this paper, a new structure for a noise-canceling and highly-linear wideband LNA with intrinsic balun based on the common-gate common-source (CG-CS) topology is presented for low-voltage and low-power applications. Since unsymmetrical loads make a mismatch in the phase and the gain of the differential output, a modified current-bleeding technique is utilized to let the balun-LNA have a differential output with symmetric loads. Adding this additional branch increases the power consumption. For reducing the power, a local feedback is used to boost the transconductance of the CG stage by the gain provided by the CS stage so the current of the CG stage can be decreased by the same factor and the power consumption is reduced accordingly. Utilizing local feedback improves the NF and the gain of the LNA as well. The linearity in this structure is improved by using the post-distortion technique. The proposed balun-LNA is simulated in 65 nm RF CMOS technology and covers the frequency range of 0.65-8.5 GHz. It has a differential voltage gain of 17 dB, an S_{11} of less than -13 dB, and an NF of 2.75-3.5 dB across the whole bandwidth. It consumes only 7.5 mA from a 1-V power supply.

***Keywords*— Wideband CMOS low-noise amplifiers, balun-LNA, gm boosting, local feedback, balanced loads, linearity.**

I. INTRODUCTION

In past few decades, multi-mode transceivers supporting software-defined radios have become more demanding, and this has led to extensive research on the wideband low-noise amplifiers (LNAs) in the standard CMOS technology [1]. For covering a wide frequency range, multiple narrowband LNAs or a single wideband LNA can be used. A single wideband LNA is preferred because it has less complexity and saves power. Such a wideband LNA must provide good input matching, low noise figure (NF), high linearity, and an adequate flat gain over the whole desired bandwidth.

Among different LNAs, single-ended ones are preferred since they do not need off-chip balun that is lossy and occupies a large area and increases the cost. On the other hand, a differential output is more preferred due to a high common-mode rejection ratio (CMRR) and low second-order distortions. So, a single-ended input should be converted to differential output. Such an LNA is called the balun-LNA. In recent decades, several wideband balun-LNAs have been introduced [2]-[5]. The shortcomings of some of these LNAs are presented in Section II.

To overcome the limitations of the aforementioned LNA structures, this paper presents a new noise-cancelling low-noise and highly-linear balun-LNA that utilizes a modified current-bleeding technique, symmetric loads, and local feedback. Boosting the g_m of the CG stage can bring both the power consumption and supply voltage down. Moreover, the size of transistors can be chosen smaller, and as a result, parasitic elements decrease and the bandwidth will be increased. This balun-LNA not only has symmetric loads and good control on the bleeding branch but also is low-power and low-voltage and has higher bandwidth than the previous works. The linearity in this structure is improved by using the post-distortion technique.

This paper is organized as follows. Section II reviews the limitations of previous balun-LNA design topologies and compares their NF, power consumption, and load symmetry. The proposed LNA is introduced in Section III. Section IV presents the simulation results. At last, Section V provides the conclusion.

II. LIMITATION OF PREVIOUS WORKS

A. Conventional CG-CS Balun-LNA

Figure 1(a) shows the conventional way of having a balun-LNA by using a CG-CS topology [2]. CG stage provides the input impedance matching and the CS stage cancels the noise and distortion produced by the CG stage. Achieving an NF of less than 3 dB is not possible in the traditional CG-CS balun topology unless by decreasing the noise of the CS stage. Figure 1(b) shows the practical CG-CS topology where the transconductance (g_m) of the CS stage is N times larger than the g_m of the CG stage. For having a balanced differential output, the load resistor of the CS stage should be N times smaller than the load resistor of the CG stage [3]. These unsymmetrical loads make a mismatch in the phase and the gain of the differential output that increase the second-order distortions and do not allow noise to be completely eliminated.

B. Balun-LNA Employing Balanced Loads and A Modified Current-Bleeding Circuit

Figure 2 shows the proposed structure for a balun-LNA with balanced loads [4]. Utilizing the current-bleeding circuit in this structure leads to having the same current in CG and CS load resistors. As a result, having a balanced differential output with balanced loads is achievable.

This structure suffers from high power consumption because the supply voltage and the current of the CS transistor are noticeably high for using the current-bleeding circuit. So, this structure is not suitable for low-voltage low-power applications. Moreover, in the circuit shown in Fig. 2,

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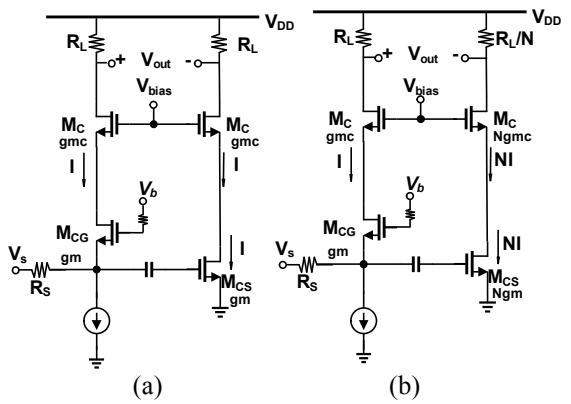

Fig. 1. CG-CS Balun-LNAs: (a) conventional topology with $g_{m,CS} = g_{m,CG}$, $R_{CS} = R_{CG}$ and $I_{CS} = I_{CG}$, (b) practical topology with $g_{m,CS} = Ng_{m,CG}$, $R_{CS} = R_{CG}/N$ and $I_{CS} = N\,I_{CG}$.

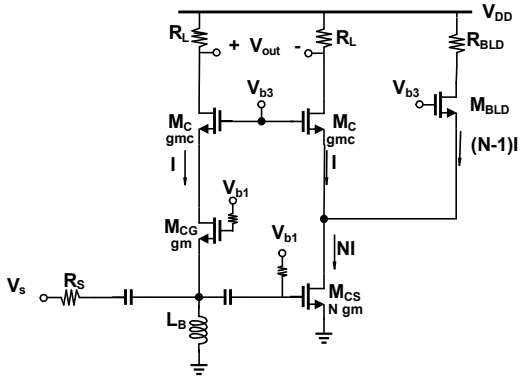

Fig. 2. Proposed balun-LNA in [4].

the low impedance of the source of M_{BLD} decreases the equivalent resistor of the drain of the CS transistor that leads to a reduction in the voltage gain of out− over out+ because of the effect of the cascode stage's source resistance on out voltages. For solving this problem and having a balanced differential output, this paper has increased the channel length of the transistors to increase the drain-source resistance (r_{ds}) and decrease the effect of the source impedance of cascode stages. Increasing the channel length of transistors leads to an increase in parasitic elements and a decrease in the bandwidth. Moreover, the supply voltage in this structure is 2.2 V and we prefer to use transistors at the standard supply voltage of 1.2 V instead of thick oxide transistors at 2.2 V supply.

C. Balun-LNA with Local Feedback

Figure 3 shows the structure of the proposed balun-LNA introduced in [5] which utilizes local feedback between the CG and CS stage to boost the g_m of the CG stage by the gain provided by the CS stage. As a result, the current of the CG stage, and consequently, the power consumption is significantly reduced. A current-bleeding circuit is added to this structure to release larger voltage headroom to allow the LNA to have larger resistors for improving the noise and the gain.

Nonetheless, in this structure, controlling the current of the bleeding branch is difficult and the loads are unsymmetrical. As it was mentioned before, the asymmetric loads cause an unsymmetrical RC time constant making a mismatch in the phase and the gain of the differential output that increase the second-order distortions and do not allow noise to be completely eliminated.

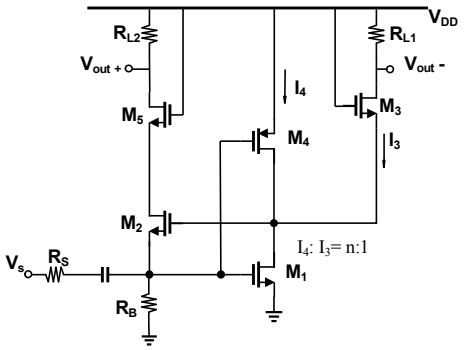

Fig. 3. Balun-LNA with local feedback proposed in [5].

III. PROPOSED LNA

The proposed wideband balun-LNA employing local feedback, modified current-bleeding technique and symmetric loads for low-power applications is shown in Fig. 4. Since unsymmetrical loads make a mismatch in the phase and the gain of the differential output, a modified current-bleeding technique is utilized to let the balun-LNA have a differential output with symmetric loads. The current-bleeding circuit consists of two PMOS cascode transistors (M_{BLD}) instead of an NMOS to increase the impedance seen at the source of the cascode transistor (M_C) (in comparison to the proposed current-bleeding technique in [4]) to prevent a reduction in the voltage gain of out− over out+. The dc current of the current-bleeding branch (M_{BLD}), CG transistor (M_{CG}), and CS transistor (M_{CS}) are provided by a wide-swing cascode current mirror.

Adding this additional branch increases power consumption. For reducing the power, a local feedback is used to boost the transconductance of the CG stage by the gain provided by the CS stage so the current of the CG stage can be decreased by a factor of $1+A_{VM}$ where A_{VM} is the open-loop gain of the local feedback. So, power consumption can be decreased by the same factor. Utilizing local feedback improves the NF and the gain of the LNA as well.

The noise generated by the CG transistor and the right cascode transistor can be canceled by the CS transistor (M_{CS}) when the input impedance matching and differential output balance conditions that are given in Sections III−A and III−B are met. M_a transistors are used as auxiliary transistors to increase the linearity. The details of the linearity improvement by adding these transistors will be described in Section III−D. The cascode stage is used to improve isolation. L_B is an external RF chock that places the source of the CG transistor (M_{CG}) at dc ground.

The details of the input impedance matching condition, the voltage gain, NF, and linearity of the proposed LNA are presented in the following sections.

A. Input Impedance Matching

We have the input impedance matching when

$$R_s = \frac{1}{g_m\left(1 + A_{VM}\right)} \tag{1}$$

where R_S is the source impedance and it is usually 50 Ω and g_m is the transconductance of the CG transistor (M_{CG}). The required transconductance for input impedance matching is decreased by a factor of $1+A_{VM}$ compared with the

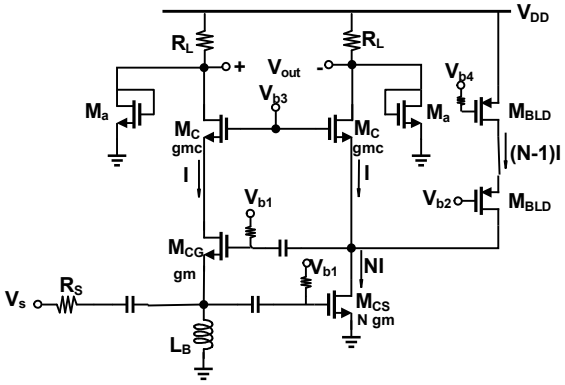

Fig. 4. Proposed balun-LNA.

traditional CG-CS LNA [2, 3] that A_{VM} is the local open-loop gain that is defined in the next section.

B. Voltage Gain

It is notable that adding the auxiliary transistors (M_a) as post-distortion does not change the equations because they only add two equivalent resistors of $(1/g_{ma})\|r_{o,a}$ in parallel with R_L that creates an equivalent resistor of R'_L. Since the size of these transistors are small, the equivalent resistor of $(1/g_{ma})\|r_{o,a}$ is large enough (about 2 kΩ) that does not change the R_L so much.

The open-loop gain of local feedback is given by

$$A_{VM} = Ng_m\left(\frac{R_L + r_{oc}}{1+g_{mc}r_{oc}}\,\|R_{BLD}\right) \tag{2}$$

where N is the size ratio of CS transistor to CG transistor, g_m and g_{mc} are the transconductance of CG transistor (M_{CG}) and cascode transistors (M_C), respectively, r_{oc} is the drain-source resistor of cascode transistors and R_{BLD} is the resistor seen at the drain of the bleeding branch and it is calculated as

$$R_{BLD} = r_{oBLD} + \left[1+\left(g_{mBLD}+g_{mb,BLD}\right)r_{oBLD}\right]r_{oBLD} \tag{3}$$

When the input impedance matching condition in (1) is satisfied, we have

$$V_{out+} = \frac{R_L}{R_S}\frac{V_s}{2} \tag{4}$$

$$\begin{aligned} V_{out-} &= \frac{1+g_{mc}r_{oc}}{1+r_{oc}/R_L}\times Ng_m\left(\frac{R_L+r_{oc}}{1+g_{mc}r_{oc}}\,\|\,R_{BLD}\right)\frac{V_s}{2} \\ &= \frac{1+g_{mc}r_{oc}}{1+r_{oc}/R_L}A_{VM} \end{aligned} \tag{5}$$

where V_s is the input signal and R_L is the symmetric load of the LNA. The differential outputs are balanced when

$$\frac{1+g_{mc}r_{oc}}{1+r_{oc}/R_L}A_{VM} = \frac{R_L}{R_S} \tag{6}$$

Equation (6) also provides the noise cancelation condition. If $r_{oc} >> R_L$, the differential outputs balance condition is simplified as

$$g_{mc}A_{VM} = 1/R_S \tag{7}$$

Under this condition, the voltage gain can be written as

$$A_V = \frac{R_L}{R_S} = \frac{1+g_{mc}r_{oc}}{1+r_{oc}/R_L}\times Ng_m\left(\frac{R_L+r_{oc}}{1+g_{mc}r_{oc}}\,\|\,R_{BLD}\right) \tag{8}$$

C. Noise Factor

As mentioned before, the noise generated by the CG transistor and the right cascode transistor can be totally canceled by the CS transistor when the input impedance matching and differential output balance conditions are met. The noise generated by the other cascode transistors is negligible because most of their noise is rotated in their loops and does not appear at the output. So the noise factor of the LNA can be roughly expressed as

$$\begin{aligned} NF = 1 &+ \frac{4\gamma Ng_m\left(2+g_{mc}R_L\right)^2}{\left(\frac{Ng_m{}^2R_S}{1+g_mR_S}+g_{mc}+\frac{1}{g_{mBLD}r_{oBLD}{}^2}\right)^2\left(\frac{R_L}{R_S}+\frac{Ng_mg_{mc}R_L}{g_{mc}+1/r_{oBLD}}\right)^2} \\ &+ \frac{\frac{4\gamma}{g_{mBLD}}\left(\frac{g_mR_L}{1+g_mR_S}+g_{mc}R_L\right)^2}{\left(1+\left(\frac{Ng_m{}^2R_S}{1+g_mR_S}+g_{mc}\right)r_{oBLD}\right)^2\left(\frac{R_L}{R_S}+\frac{Ng_mg_{mc}R_L}{g_{mc}+1/r_{oBLD}}\right)^2} \\ &+ \frac{8R_L}{R_S\left(\frac{R_L}{R_S}+\frac{Ng_mg_{mc}R_L}{g_{mc}+1/r_{oBLD}}\right)^2} \end{aligned} \tag{9}$$

The second and third terms of (9) stand for the thermal noise of M_{CS} and M_{BLD}, respectively, and the last term represents the thermal noise contribution of R_L. As it is seen, most of the NF is related to the CS transistor.

Figure 5 shows an overview of the NF with different values of N where N is the size ratio of CS transistor to CG one. With increasing N, NF decreases but at the same time the power consumption increases and IIP3 gets worse because the size of the CS transistor has been increased. Therefore, we choose the N for which the NF is reasonably low, but the power consumption is not so high and IIP3 for this case will be improved by the post-distortion technique that its details are presented in Section III–D. For the design of the proposed LNA, N = 20 is chosen. It is notable that with the increasing of N, A_{VM} remains almost constant because from (2) and (3), with increasing of N, R_{BLD} decreases as well, and as the result, A_{VM} does not change so much.

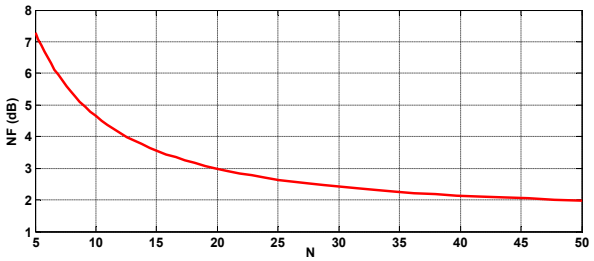

Fig. 5. Relationship between NF and N at 1 GHz.

D. Linearity

For improving the linearity, the post-distortion technique proposed in [6] is implemented on the LNA as shown in Fig. 6. M_{1a} is a diode-connected transistor that linearizes M_1 as follows. First, we can model the drain current of M_1 and M_{1a} to the third-order as

$$i_1 = g_m v_1 + g_2 v_1{}^2 + g_3 v_1{}^3 \tag{10}$$

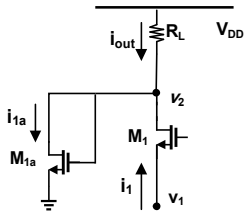

Fig. 6. Linearity improvement by post-distortion technique.

where g_m, g_2, and g_3 are the main transconductance and second- and third-order nonlinearity coefficients, respectively. The drain current of M_{1a} is also modeled as

$$i_{1a} = g_{ma}v_2 + g_{2a}v_2^2 + g_{3a}v_2^3 \tag{11}$$

Next, consider v_2 is related to v_1 by

$$v_2 = \alpha_1 v_1 + \alpha_2 v_1^2 + \alpha_3 v_1^3 \tag{12}$$

The α_1–α_3 terms can be extracted from simulation results because they are frequency dependent. Two nonlinear current i_1 and i_{1a} sum up at the output node producing the output current as

$$i_{out} = i_1 - i_{1a} = (g_m - \alpha_1 g_{ma})v_1 + (g_2 - \alpha_1^2 g_{2a} - \alpha_2 g_{ma})v_1^2 + (g_3 - \alpha_1^3 g_{3a} - g_{ma}\alpha_3 - 2g_{2a}\alpha_1\alpha_2)v_1^3 \tag{13}$$

A good IIP3 is achieved when the third term in (13), which is the third-order distortion, is close to zero. It is necessary to mention that M_{1a} decreases the linear term as well but it does not tangibly degrade the gain and NF because its size is much less than the size of M_1. To examine the linearity improvement, a two-tone test with RF frequencies of 1 GHz and 1.1 GHz is performed on the proposed LNA. Simulation results that are given in the next section show that the proposed idea has improved the value of IIP3 about 3 dB.

IV. Simulation Results

The circuit-level simulations of the proposed balun-LNA were carried out with Spectre RF using a 65 nm RF-CMOS technology. Poly resistors and MIM capacitors are used for resistors and capacitors, respectively. Figure 7 shows the S-parameters of the proposed LNA. According to this figure, S_{11} is below –13 dB, S_{21} is 14-17 dB, and S_{12} is below –50 dB over the whole frequency bandwidth. Figure 8 shows that the flat differential voltage gain of 17 dB with –3 dB bandwidth of 15 MHz – 9.3 GHz is obtained. Moreover, as shown in Fig. 9, the proposed LNA achieves an NF of 2.75-3.5 dB across the whole bandwidth of 0.6-8.5 GHz. Figure 10 illustrates the stability factor K_f that is defined in (14). Since it is larger than 1 over the large bandwidth, the LNA is unconditionally stable.

$$K_f = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \tag{14}$$

Figures 11 and 12 show the simulated IIP3 before and after adding the auxiliary transistors (M_a). As it is seen, the proposed idea has improved IIP3 about 3 dB.

Table 1 represents a comparison between the proposed LNA and some of the previous wideband LNAs. As it is seen, the proposed LNA achieves higher power gain, larger bandwidth, and better IIP3 without adding additional noise with much less power consumption than the previously reported ones. In comparison with [4], the proposed LNA, not only has symmetrical loads and balun function but also has reduced power consumption about 12.5 mW and has improved the value of IIP3 about 2.7 dB without adding any additional noise. Compared with [5], that has employed the local feedback, the proposed LNA has symmetrical loads and 2.8 dB IIP3 improvement without adding additional noise and almost with the same power consumption. The design parameters are summarized in Table 2. Also, Table 3 represents the circuit simulation results of the proposed balun-LNA in the worst process corner cases. As it is clear, the proposed LNA is well robust against process, voltage, and temperature (PVT) variations.

The following figure of merit (FoM) defined in [7] is used in Table 1 to have a better comparison.

$$FoM = \frac{S_{21}[abs] \times IIP3[mW] \times BW\ [GHz]}{(F-1) \times P_{dc}[mW]} \tag{15}$$

where S_{21} is the maximum magnitude of power gain, BW is the 3 dB bandwidth of the LNA, F is the magnitude of the minimum NF over the entire bandwidth, and P_{dc} is the LNA power consumption.

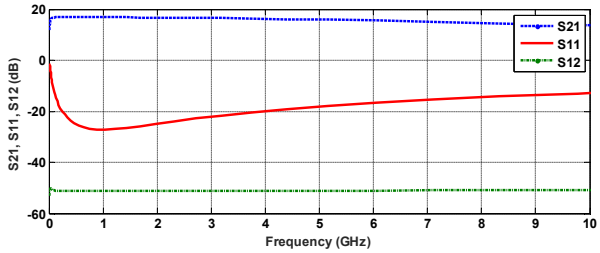

Fig. 7. Simulated S-Parameters of the proposed LNA.

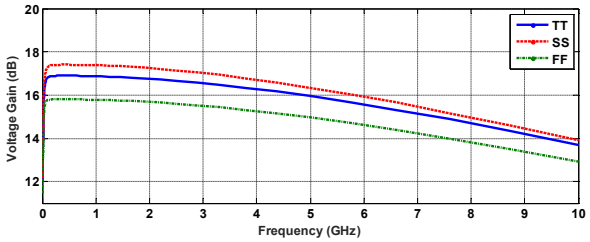

Fig. 8. Simulated differential voltage gain of the proposed LNA.

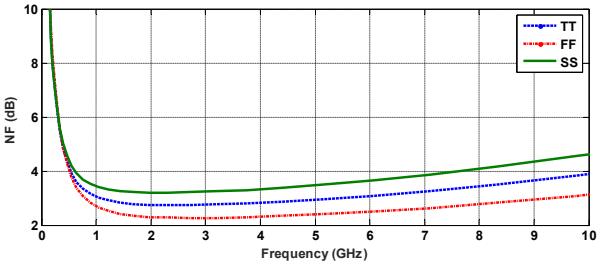

Fig. 9. Simulated NF of the proposed LNA.

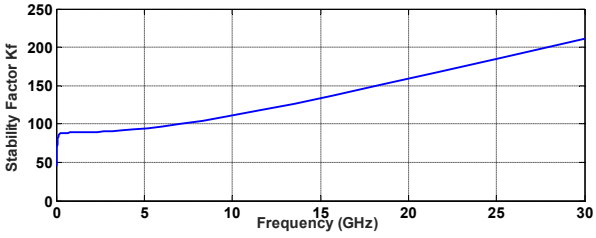

Fig. 10. Stability factor K_f.

Table 1. Performance Comparison.

Ref.	CMOS Process	BW (GHz)	S_{11} (dB)	S_{21}(dB)	NF (dB)	IIP3 ** (dBm)	Symmetric load	Balun function	V_{dd} (V)	Power (mW)	FoM
[3]	65 nm	0.2-5.2	<-10	15.56	2.9-3.5	0	No	Yes	1.2	21	1.5
[4]	65 nm	0.01-1	<-10	30	2.3-3.3	-4.1	Yes	Yes	2.2	19.8	0.845
[5]	130 nm	0.2-3.8	<-9	19	2.8-3.4	-4.2	No	Yes	1	5.7	2.53
[7]*	130 nm	2-7.6	<-10	13.8	1.85-2.1	-15.2	No	No	1.1	2.15	0.72
[8]	90 nm	0.8-6	<-10	20	2.5-3.5	-3.5	Yes	Yes	2.5	12.5	2.4
[9]	90 nm	2.5-4.5	<-10	21.2	4-5.4	-8	No	Yes	1.2	8	0.3
[10]*	90 nm	2.6-13.7	<-10	11	3.8-5	+4.6	Yes	No	1.2	12	4.85
[11]*	130 nm	4.7-11.7	<-11.9	12.4	2.88-3	-3	No	No	1.2	13.5	2.06
[12]*	90 nm	2.5-10.9	<-11	10.3	2.6-3	+10.4	Yes	No	1.2	15.6	21.4
This work*	65 nm	0.65-8.5	<-13	17	2.75-3.5	-1.358	Yes	Yes	1	7.5	6.1

*Simulation results **At RF frequency of 1 GHz with 100 MHz spacing

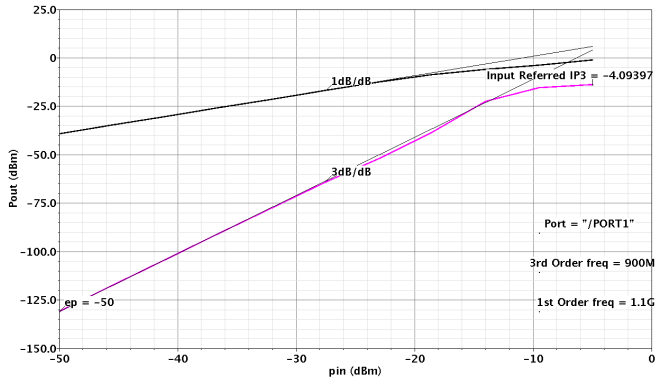

Fig. 11. IIP3 of the proposed LNA before utilizing the post-distortion technique at $f_1 = 1$ GHz and $f_2 = 1.1$ GHz.

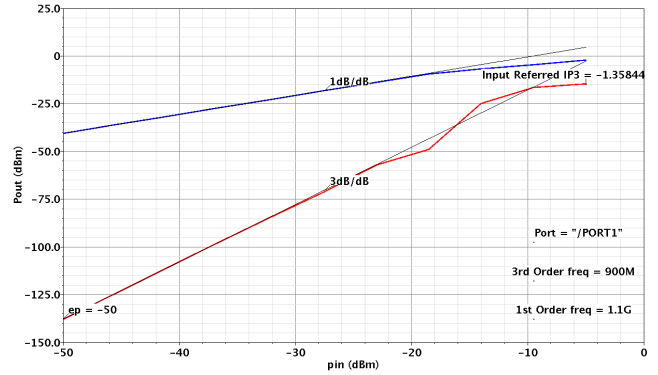

Fig.12. IIP3 of the proposed LNA after utilizing the post-distortion technique at $f_1 = 1$ GHz and $f_2 = 1.1$ GHz.

Table 2. Design values of the proposed LNA.

M_{CG}	10×600 nm/60 nm	A_{VM}	4
M_{CS}	10N×600 nm/60 nm	R_L	495 Ω
M_C	10×1.2 µm/60 nm	C	10 pF
M_a	600 nm/60 nm	I_b	36 µA
M_{BLD}	10 (N-1) ×600 nm/60 nm	N	20

Table 3. Corner case simulation results.

Corner Case	TT @ 27°C	SS @ 85°C	FF @ -40°C
BW_{3dB} (GHz)	0.015-9.3	0.016-8.9	0.013-10
S11 (dB)	<-13	<-13	<-13
S21 (dB)	17	17.4	15.8
NF_{min}* (dB)	2.75	3.19	2.26
IIP3 (dBm)**	-1.358	-1.75	-2.748

*Minimum NF in bandwidth **At RF frequency of 1 GHz with 100 MHz spacing

V. Conclusions

In this paper, a new approach employing a modified current-bleeding technique, symmetric loads and local feedback is proposed for a wideband and highly linear noise-cancelling balun-LNA based on the CG-CS LNA. The linearity is improved by employing a post-distortion technique. Simulated in a 65 nm RF-CMOS technology, the proposed balun-LNA attains analogous and even better NF, and IIP3 than those of previously reported wideband balun-LNAs at lower power consumption and larger bandwidth while providing balun functionality and differential output with symmetric loads.

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