A Six-Order Wideband Bandpass Sigma-Delta Modulator

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ABSTRACT

This paper proposes a behavioral simulation of a Wideband, 1.25MHz, Six-Order, Two-Path, Double-Sampled, Bandpass, Sigma-Delta Modulator at IF-frequency 40MHz with 78dB Dynamic Range in a 0.35μm CMOS process.

I. INTRODUCTION

Oversampling bandpass A/D is widely used because of its increased accuracy and decreased analog front-end circuitries in transceiver systems. High frequency digital processing is more robust than its analog counterpart, and does not have the analog circuit imperfections. Digital IF extraction is also very beneficial since it adds the programmability to the system, for adapting to various standards.

As shown in Fig.1, the higher IF frequency improves the suppression of the image signal, permitted by a non-ideal channel-selecting filter to enter in the signal bandwidth [1]. Therefore in this paper it has been tried to achieve a higher IF frequency and a reasonable resolution in the design of the wide band sigma-delta modulator.

This paper describes a design and a behavioral simulation procedure of a fully integrated Switched Capacitor, Wideband, and Bandpass Sigma-Delta Modulator in a 0.35μm CMOS process. The modulator IF frequency is 40MHz, achieving 78dB Dynamic Range.

In section II, the concepts of high order bandpass sigma-delta modulators are illustrated. In section III, the two-path architecture and low-pass filter technique are investigated. Finally the simulation results are summarized in section IV.

II.HIGH ORDER BANDPASS SIGMA-DELTA MODULAROR

In a bandpass sigma-delta modulator, the quantization noise is pushed from the signal band at the desired center frequency f_{IF} As the bandwidth of the signal is increased, the in band quantization noise is enhanced, which leads to a lower SNR. In wideband applications in order to overcome this problem, a higher order sigma-delta modulator associated with a combination of multi-bit and single-bit quantizers are used [2].

Bandpass sigma delta structures can be obtained from baseband structures. In order to convert a baseband architecture to a bandpass system, the transformation of $Z^{-1} \rightarrow -Z^{-2}$ in z-domain is used [3].

For higher order sigma-delta modulators, the loop stability becomes a serious issue. Making use of a multi-bit quantizer in the loop leads to a better stability and also a higher SNR. However, disadvantages of a multi-bit sigma-delta modulator are the inherent non-linearity of the multi-bit DAC decreasing the SNR and also the added complexity of the system dissipating more power.

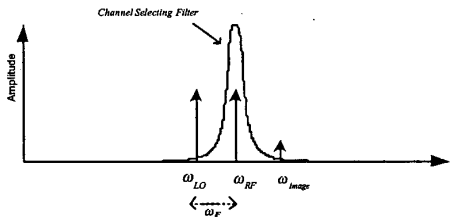

Fig.1: A non-ideal RF channel-selecting filter doesn't reject the image signal completely

Using a global feedback, through a single-bit quantizer, and a local multi-bit quantizer improves the linearity of the system without the need of a high-resolution multi-bit quantizer. The proposed architecture [2], [4] is shown in Fig.2 (a). In [2], the mathematical concepts and manipulations of this architecture are precisely described.

The simulation of the system, shown in Fig.2 (a), with MATLAB proves that the best choice for coefficients is $\alpha 1=0.5$, $\alpha 2=1$ and $\alpha 3=1$.

III.TWO-PATH ARCHITECTURE AND LOW-PASS FILTER TEQNIQUE

Not being able to achieve complete settling in high frequency IF analog blocks, has forced designers to think of parallel structures, providing more time for settling of

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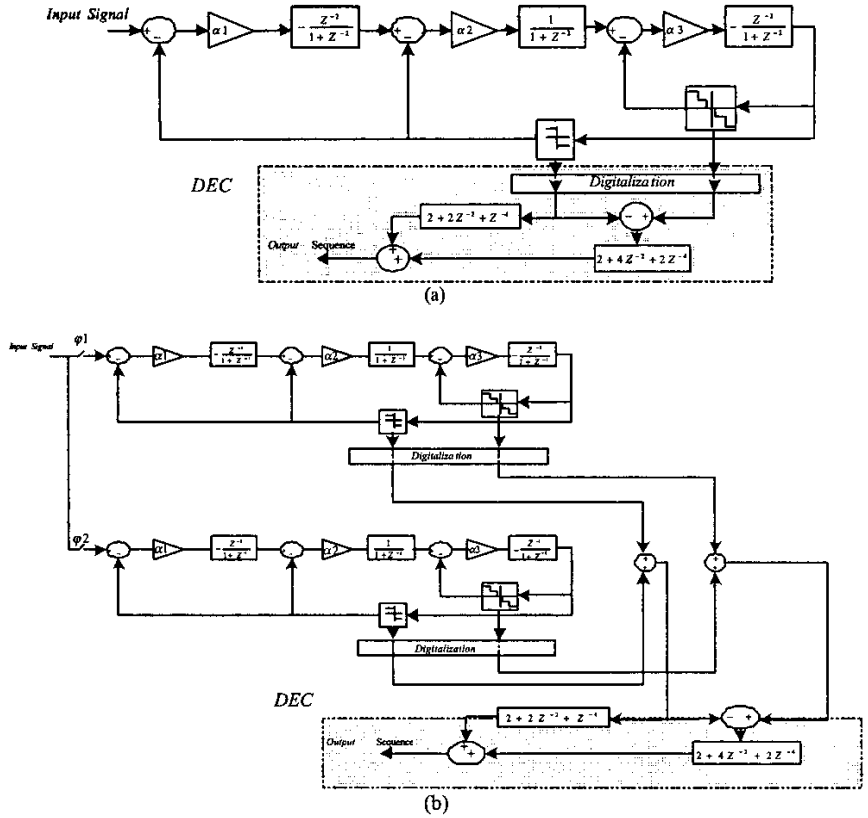

Fig.2: (a) The Main blocks of the system without using two-path architecture.
(b) The Main blocks of the two-path architecture in which high-pass filter is used.

OP-AMP. The two-path structure shown in Fig. 2(b) can be realized by employing a transformation reported in [3], in which all Z^{-2} are converted to Z^{-1} because of the doubled clock period in each path.

By this transformation, the main blocks of each path will become high-pass filters whose circuit implementation is shown in Fig. 3(a) involving two major disadvantages: The first disadvantage of the high-pass filter implementation, shown in Fig. 3(a), is that the output noise of op-amps are added to the input noise.

The other disadvantage of the high-pass filter is that the output equivalent capacitance of the op-amp is increased. It should also be noticed that the op-amp feedback factor $\beta=CI/(Cs+Cf+CI)$ is decreased [5].

The bigger op-amp output capacitance and its lower

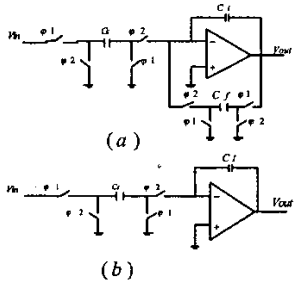

Fig.3: (a) High-pass filter implementation, using switched capacitor circuit.
(b) Low-pass filter implementation, using switched capacitor circuit.

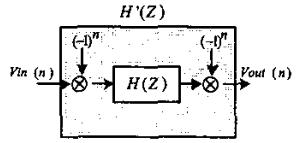

Fig.4: This transformation converts LP filter to HP filter.

feedback factor both makes the op-amp design more challenging.

Substituting the high-pass filters by the low-pass filters makes the system more relaxed. The low-pass integrator is shown in Fig. 3(b).

The transfer functions of high-pass and low-pass filter are shown in equations (1) and (2) respectively:

$$\mathbf{H(z)} = \frac{\mathbf{z^{-1}}}{\mathbf{1+z^{-1}}} \quad (1)$$

$$\mathbf{H(z)} = \frac{\mathbf{z^{-1}}}{\mathbf{1-z^{-1}}} \quad (2)$$

The quality between two transfer functions shown in Fig. 4 can be easily verified.

By employing this technique, the low-pass implementation of the bandpass sigma-delta modulator, shown in Fig.5, can be achieved. In this paper, this approach is taken to implement a bandpass sigma-delta modulator.

One problem, to be mentioned, is that two-path architecture suffers from mismatches between two paths, particularly if double sampling technique is used, producing the image signal [3], [5]. There are some methods, not investigated in this paper, to reduce image signal, such as Individual Level Averaging (ILA) [6]. However, the typical range of I.R (Image Rejection), regarded in this paper, is about 40dB.

IV.SIMULATION RESULTS

In this section some mathematical analysis, using MATLAB software, are described. The first step in the design of the system is to approximate the Dynamic

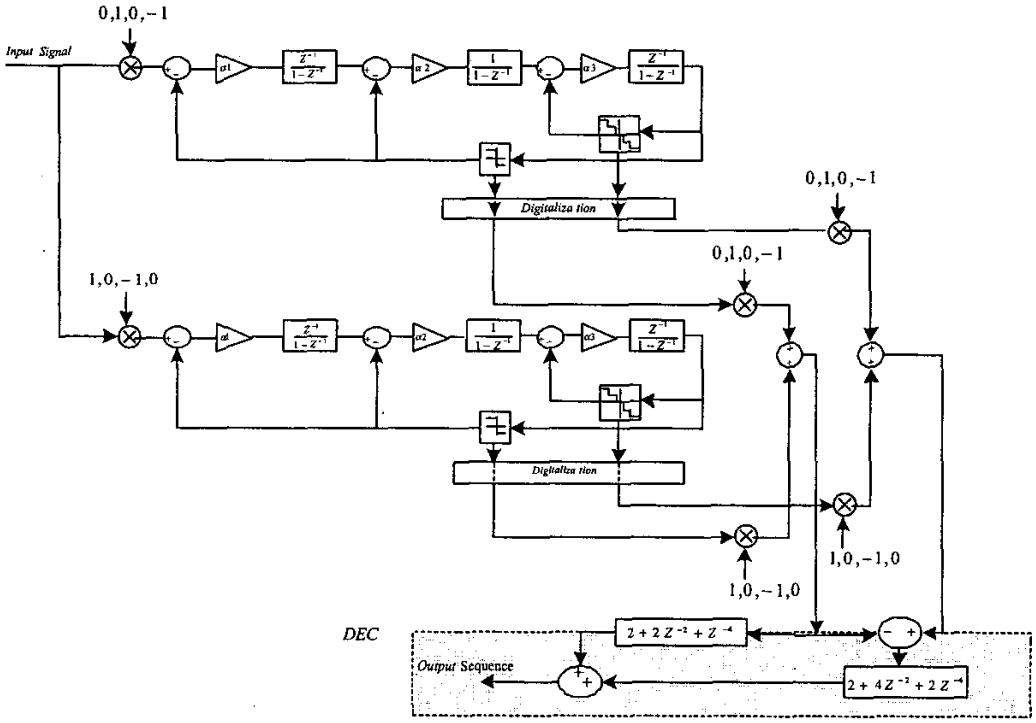

Fig.5: The Main blocks of the two-path architecture in which low-pass filter is used.

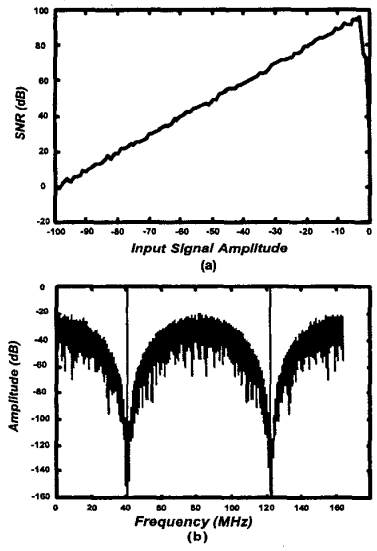

Fig.6: (a) DR (dB) versus input signal (dB). (b) Spectrum of the output signal

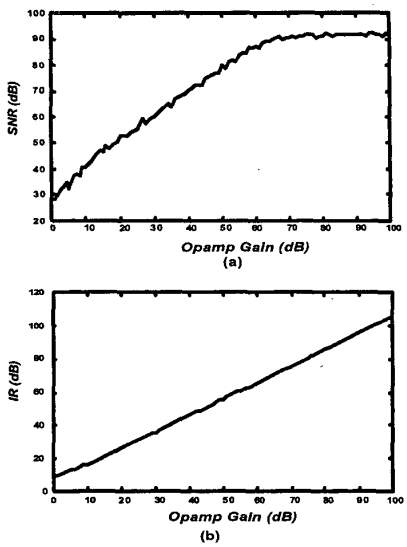

Fig.7: (a) SNR_{max} (dB) of the system versus op-amp gain (dB). (b) IR (dB) of the system versus op-amp gains (dB).

Range, DR, of it. Thus by modeling the system shown in Fig. 5, in MATLAB, it can be derived that Dynamic Range, shown in Fig. 6(a), is about 95dB which is better than the aimed target.

The spectrum of the output signal, representing the highest 91dB SNR, is shown Fig. 6(b). Of course, this DR is a mathematical result, and the non-linearity effects of the 5-bit DAC and other imperfections, described in the next step, will decrease it.

In order to model the effect of opamp finite gain and parasitic capacitor in a low-pass filter transfer function, equations (3), (4), (5), (6) and (7) can be used [3], in which c_p represents the parasitic capacitance.

$$H(z) = \frac{c_s}{c_I} \cdot \frac{r_2 . z^{-1}}{1 - \frac{r_2}{r_1} . z^{-1}} \quad (3)$$

$$r_1 = \frac{f_{dc1} . A}{1 + f_{dc1} . A} \qquad r_2 = \frac{f_{dc2} . A}{1 + f_{dc2} . A} \quad (4), (5)$$

$$f_{dc1} = \frac{c_I}{c_I + c_p} \qquad f_{dc2} = \frac{c_I}{c_I + c_s + c_p} \quad (6), (7)$$

By using these relations and assuming that path1 is ideal and path2 is not, the SNR of the system, excluding the image signal, versus op-amp finite gain is simulated, and shown in Fig. 7(a), implying that the minimum op-amp gain must be about 65dB.

Another problem determining the minimum op-amp gain is the image signal that must be rejected more than 40dB.Similar to the previous simulation the simulation result, shown in Fig.7.b, confirms that 65dB op-amp gain is adequate.

It must be mentioned that in the op-amp finite gain analyses described before, a parasitic capacitor, about 0.25PF in the inputs of op-amp, is assumed and the value of the capacitors, *CI, CS,* has been chosen about .5PF except in the first stage of the system, shown in Fig. 5, in which the value of the capacitor, *CI,* has been chosen 1PF.

Another bottleneck in the design of sigma-delta modulators is the op-amp finite bandwidth. There is a simple conventional approach to select the bandwidth 3 to 5 times of the maximum clock frequency [7]. Thus, in the double sampling technique, op-amp bandwidth must be about 350MHzs in that the maximum clock frequency is 80MHz.

The other problem destructing the performance of the system leading to creation of the image signal is the capacitor mismatches causing the ratio of *CI/CS* to vary. This problem affects both SNR_{max} and IR. In order to

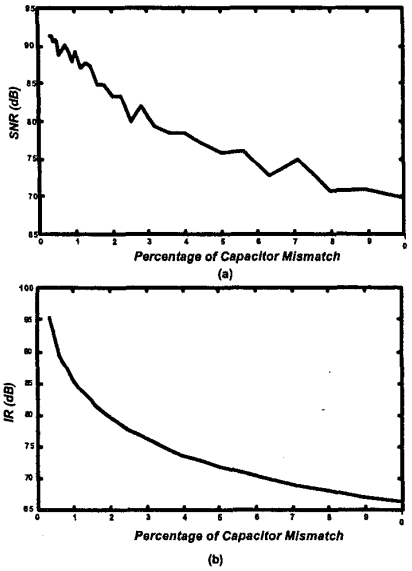

Fig.8: (a) the variation of SNR_{max} versus the variation of capacitor mismatches in percentage mode.
(b) The variation of IR versus the variation of capacitor mismatches in percentage mode.

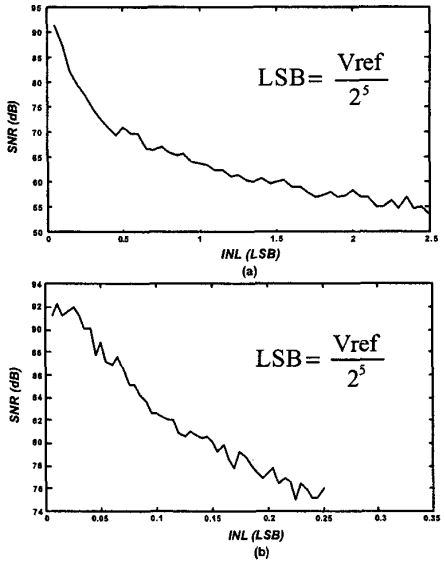

Fig.9: (a), (b) These figures show the SNR_{max} versus INL in percentage mode

simulate this problem, it is assumed that path1 is ideal and in path2 there is a mismatch between *CI* and *CS*. The effect of the mismatch on SNR_{max} and IR is shown in Fig. 8(a) and Fig. 8(b) respectively, implying that a mismatch bigger than 2% is harmful.

The other far more important problem is the non-linearity of the 5-bit DAC, modeled in MATLAB. In order to model non-linearity of 5-bit DAC, INL parameter was used [7].

Fig. 9(a) and Fig. 9 (b), representing the SNR_{max} versus INL, demonstrate that the resolution of the 5-bit DAC must be about 8bit, to get a maximum 78dB SNR. It must be mentioned that DAC non-linearity doesn't produce image signal, but decreases the SNR figure.

All of the specifications considered for opamp and 5-bit DAC, can be implemented in a 0.35μm CMOS process.

The simulation of the system with HSPICE confirms the above results. In order to design opamp, two-stage structure is used in which first stage is a telescopic-cascade.

The power dissipation of the sigma-delta modulator, excluding the power dissipation in 5bit DAC, is about 90mW.

Considering the topology of the system, shown in fig.5, it appears that the first stage and second stage are delayed integrators, and third stage is delay-less integrator.

In the circuit implementation, considering double sampled technique used in this design, there is not any time for comparator circuit decision. Therefore the third stage integrator has been designed as a delay-less integrator, and its delay is performed in the comparator.

The circuit implementation and its clock phases are shown in fig.10.

In this circuit, sampling switches turn on sooner preventing glitch in the output voltage of opamps

CONCULOSION

A wideband, six order, switched capacitor, bandpass Sigma-Delta modulator at 40MHz IF frequency has been designed and simulated behaviorally in a 0.35μm CMOS technology. The bandwidth of the system is about 1.25MHz and its Dynamic Range is 78dB.

In order to achieve higher accuracy and more stability a 5-bit quantizer as a local feedback and a single bit one as a global feedback were used. Also in order to relax the op-amp settling time requirement, two path and double sampling architectures were employed.

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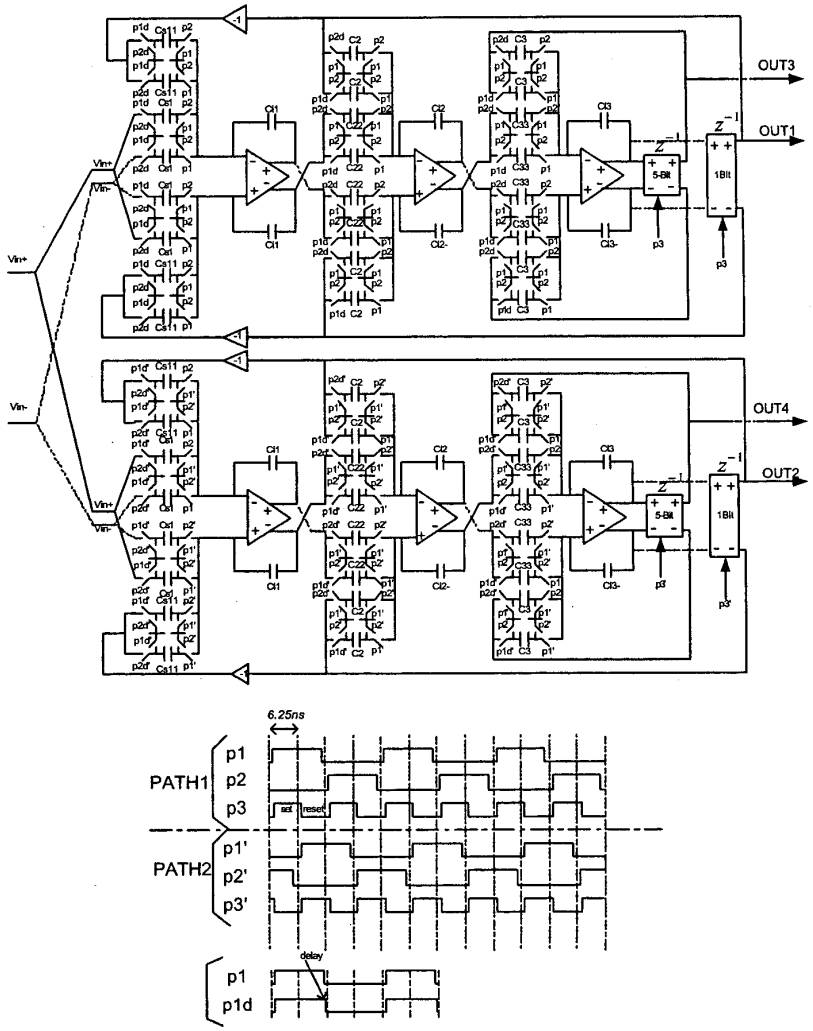

Fig.10: Circuit implementation of the sixth-order modulator

everyone who has guided him in his education, and also all of his friends in the University of Tehran IC Design Lab.

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