A Novel Low Phase Noise and Low Power DCO in 90 nm CMOS Technology for ADPLL Application

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Abstract— **A novel structure with low phase noise and low power dissipation fully differential cross-coupled CMOS LC-DCO is presented. Two effective techniques including adding two digitizer and utilizing two top switching transistors, are used in order to optimize the phase noise. The performance of the proposed DCO well meets all the requirements for low phase noise and low power All-Digital Phase Locked-Loop (ADPLL). Simulation results are obtained by the Cadence IC Design software in 90nm CMOS technology with Spectre simulator. Carrier frequency of Proposed DCO is tuned in the range of 10 to 10.7 GHZ. The measured phase noise at 1 MHz offset from the 10 GHz carrier frequency is around -116 dBc/Hz, while the DCO consumes 4.9 mw at the 1.2 volt supply voltage and finally, FOM is -189 dBc/Hz.**

Keywords-component; DCO, Carrier, ADPLL, Phase Noise, Power Dissipation, Radio Frequency.

I. INTRODUCTION

In recent years, all-digital phase locked loops (ADPLLs) have been explored as local oscillator (LO) sources for low phase noise and power-constrained applications such as cellular phones and mobile wireless devices [1]-[4]. The performance of ADPLLs is directly related to the characteristics of the digitally-controlled oscillator (DCO), such as the phase noise and power consumption. In 2003, a DCO for cellular mobile phones was first proposed and demonstrated, and after that DCOs are widely used along with the rapid development of wireless communications [5], [6]. So far, low power CMOS technologies have been employed for DCO designs. One of the commonly used CMOS oscillator topologies is the controlled delay ring oscillator that exhibits poor phase noise performance for most RF applications [7]. For low phase noise applications, LC-oscillators are used [8]. However, the oscillation frequency is normally controlled by an analog tune voltage. In deep submicron CMOS process, the voltage headroom is greatly reduced and analog tuning for wide tuning oscillators becomes more and more difficult. Varactors in deep submicron process are highly nonlinear with reduced linear operation region and poor frequency tuning resolution. In this paper, a novel structure with low phase noise and low power dissipation fully differential cross-coupled CMOS LC-DCO is presented that implements digital frequency tuning by switching the varactors to achieve

one of two distinct capacitance values. The design process involves an effective method to decrease flicker noise. This DCO is suggested for low phase noise and low power ADPLL that operates at 3cm band, exactly, Radiolocation band frequencies. This work compared with conventional cross-coupled LC-DCO (with constant bias transistors) at the same condition and better performance of novel LC-DCO rather than conventional LC-DCO is demonstrated.

The organization of the paper is as follows; in section II, the conventional cross-coupled architecture for DCO is explained, and the important required features for the DCO are presented. Section III is devoted to description of proposed CMOS LC-DCO and how to improved phase noise. Simulation results and conclusion are presented in sections IV and V, respectively.

II. CONVENTIONAL LC-DCO TOPOLOGY

Fig. 1, shows the conventional cross-coupled CMOS DCO which is composed of the Inductor and Capacitor (LC) tank, complementary cross-coupled pair MOSFETs, varactors, constant bias current transistor and pair inverters.
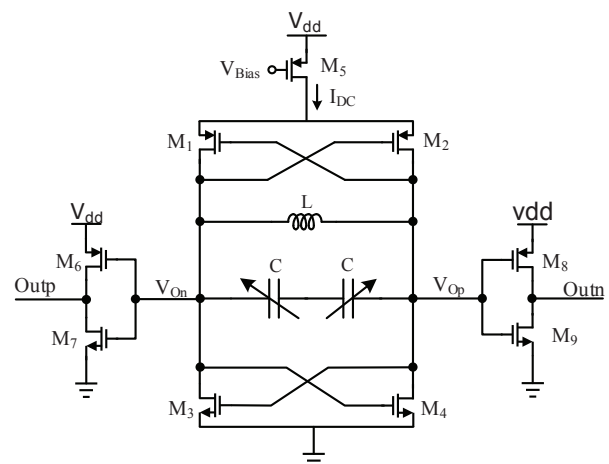

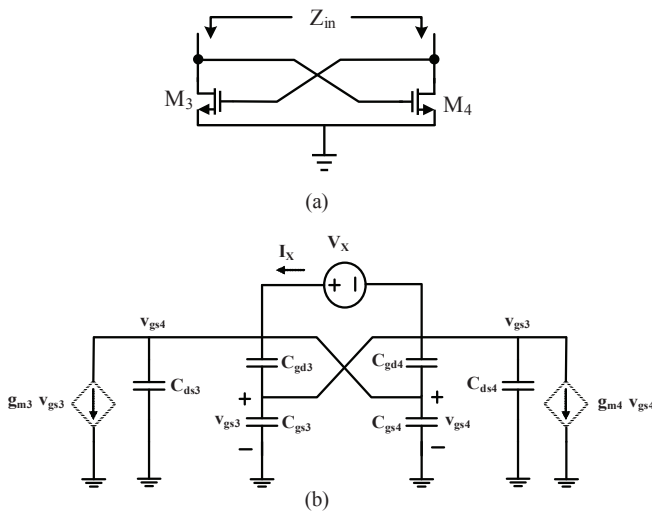Figure 1. Circuit schematic of conventional LC-DCO

(a)

(b)

Figure 2. Cross coupled pair (a). Circuit diagram (b). high-frequency equivalent circuit

A simplified schematic of cross-couple pair is shown in Fig. 2 (a). M_3 and M_4 demonstrate NMOS transistors. The high-frequency equivalent circuit with capacitive parasitic is shown in Fig. 2 (b).

Let assume

$$C_{gd}=C_{gd3} \| C_{gd4} \qquad (1)$$

$$C_{gs}=C_{gs3} \| C_{gs4} \qquad (2)$$

C_{gs} of M_6, M_7, M_8 and M_9 transistors are considered in C_{ds} of M_3 and M_4 transistors. We can calculate the input impedance Z_{in} as follows:

$$Z_{in} = \frac{V_X}{I_X}$$

$$= \frac{\left(\frac{1}{g_{m3}}+SC_{ds}\right)+\left(\frac{1}{g_{m4}}+SC_{gs}\right)}{1+\left(SC_{gd}-\frac{g_{m1}}{g_{m1}}+SC_{ds}\right)+\left(SC_{gd}-\frac{g_{m2}}{g_{m2}}+SC_{gs}\right)} \qquad (3)$$

If the transistors size is the same, we can assume that $g_{m3}=g_{m4}=g_m$ and $C_{gs} \approx C_{ds}$ for RF range in simplified calculation with small dimension transistor [9]. Equation (3) becomes as following:

$$Z_{in} = \frac{2}{-g_m + 2SC_{gd} + SC_{ds}} \qquad (4)$$

When the parasitic capacitance is removed, the common negative resistance of the input is demonstrated by $-2/g_m$. Howbeit the complementary topology has more transistors than the NMOS pair, the differential output voltage swing is larger for the same power dissipation resulting in diminished phase noise. The M_1–M_4 transistors of a complementary cross-coupled pair are shown in Fig. 1, which yields $-((2/g_{mn})\|(2/g_{mp}))$ negative resistance to compensate the passive
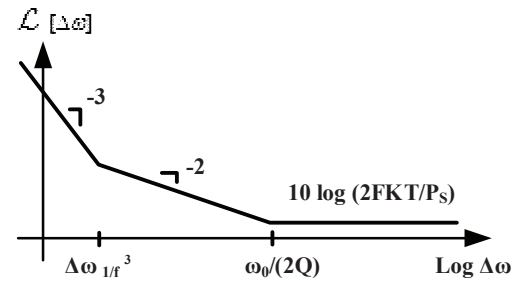

Figure 3. Typical plot of the phase noise of an oscillator versus offset from carrier

devices loss of LC tank. It can be achieved to start up for oscillation [10] and output waveforms of the circuit are differential. The conventional LC-DCO in Fig. 1 keeps oscillation by negative resistance generated by the NMOS and PMOS differential switch pair in parallel with LC-tank (L=250 pH). In Fig. 1, the drain-source voltages of the M_3, M_4 are identified as V_{On}, V_{Op} because the source of M_3, M_4 are connected to ground. The gate-drain voltages of M_3, M_4 are V_{Op}-V_{On} and V_{On}-V_{Op}, respectively. Due to the symmetry of the differential structure, the gate-drain voltages are equal in magnitude but opposite in signs. When V_{Op} and V_{On} are small, the differential output waveform $|V_{Op}$-$V_{On}|$ is near to zero, so that both M_3 and M_4, similarly, M_1 and M_2 operate in saturation region. With raise in output voltage swing, for example, during the first semi oscillation cycle, when V_{Op}-V_{On} raises above the threshold voltage of NMOS transistor (V_t), the gate-drain of M_3 exceeds +V_t, forcing M_3, similarly, M_2 into triode mode operation. While the gate-drain of M_4 falls below -V_t, driving M_4, similarly, M_1 deeper into saturation mode operation. Phase noise is one of the essential characteristic of any oscillator and it is an important index of an oscillator's frequency stability. The basic sources of phase noise are flicker and thermal noises which will be converted into phase noise because of AM to PM up-conversion and fast switching of cross-coupled pair, respectively, as well as the varactors will detect envelope fluctuations due to AM noise on the oscillation, and by modulating the average capacitance convert this into FM noise [11], [12]. The lesson's model estimates the phase noise at a given offset frequency, $\Delta\omega$, from the centre frequency, ω_0, as below [13], [14]:

$$\mathcal{L}[\Delta\omega] = 10Log \left\{\left[\frac{2FKT}{P_s}.(1+(\frac{\omega_0}{2Q_L\Delta\omega})^2).(1+\frac{\Delta\omega_{\frac{1}{f^3}}}{|\Delta\omega|})\right]\right\} \qquad (5)$$

where F is an empirical parameter (often called the "device excess noise number"), K is Boltzmann's constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, Q_L is the effective quality factor of the tank with all the loadings in place (also known as loaded Q), $\Delta\omega_{1/f^3}$ is the frequency of the corner between the $1/f^3$ and $1/f^2$ regions, as shown in the sideband spectrum of Fig. 3 [14]. In a sensibly designed oscillator circuit, with constant bias current, in [12] it is picked that the fixed current transistor takes a main portion approximately 75% in phase noise function. This reality should not be connived during the design. For the proposed of

reducing the effect of the constant current transistor noise, the noise filter technique is adopted in the design [12].

III. PROPOSED LC-DCO TOPOLOGY

The method has been reported that repress the noise share of the constant bias transistor in the differential LC-oscillator [12]. One usual method is putting an LC filter in parallel with the constant bias transistor to transfer the noise signal to the ground. In this method, an additional inductor is required to go up the constant bias transistor impedance at the oscillation frequency. However, the additional inductor goes up the chip size and leads to unforcasted effects of two inductors working at different resonant frequencies. Fig. 4, shows the proposed cross-coupled CMOS DCO which is composed of all conventional DCO element in additional two digitizer and utilizing two top switching transistors. In this section we debate the component such as LC tank and switching capacitor modules, then discuss the proposed circuit performance with top switching transistors and two digitizer.

A. Tank of the DCO

We utilize circuit model of spiral_std inductor from the Cadence IC Design library for simulation. The resonating tank leads to the current in the tank to be Q times larger. Therefore the metal lines connecting the LC tank need to be enough large to resist the large current [15]. The quality factor of the inductor in conventional DCO is approximately 13 over the working frequency range.

Frequency tuning of a low-voltage deep-sub micrometer CMOS oscillator is quite a challenging task due to its highly nonlinear frequency-versus-voltage characteristics and low voltage headroom. Fig. 5 shows normalized representative curves of a MOS varactor capacitance versus control voltage (C–V) curve for both a traditional CMOS process and a deep-sub micrometer process. Previously, a large linear range of the C–V curve could be exploited for a precise and wide operational control of frequency. With a deep-sub micrometer process, the linear range is now very compressed and has undesirable high gain, which makes the oscillator extremely susceptible to noise and operating point shifts [5].
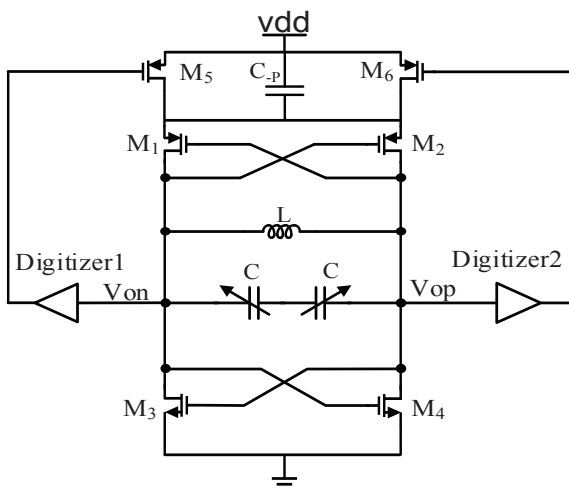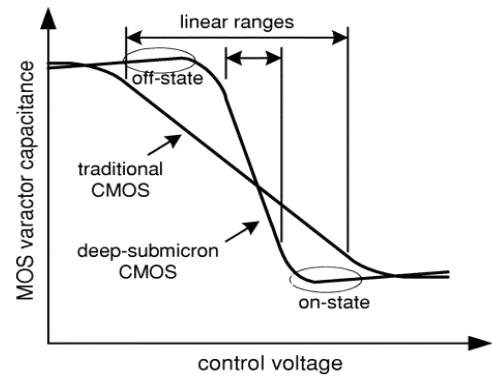

Figure 5. Idealized capacitance versus voltage curves of a MOS varactor for both a traditional and a deep-submicrometer CMOS process.

In Fig. 5, the flat on-state region and the flat off-state region are used as two stable binary-controlled operating points. NMOS-varactor could not be implemented in the distinct P-well, so the NMOS-varactor has high sensitivity to noise that due to substrate than PMOS-varactor. According to this, we used the PMOS-varactor. In other word, Because of the well isolation properties in N-well process, the PMOS transistor is a best option for a MOS-varactor. Fig. 6 shows an implementation of the differential PMOS-varactor and the driver stage [5]. The High and Low rail supply levels of the inverter are set to correspond with the two stable operating points, (In this work High = 1.2V and Low = 0V). The var- actor used in this work is a differential structure. The balanced capacitance is between the gates of PMOS devices M_1 and M_2 (Fig. 6), whose source, drain, and bulk connections are connected together and exerted to the M_3/M_4 inverter output. as the voltage control is now exerted to the bulk and source/drain, the negative and reducing values of VG in [5] covering the inversion mode are of interest. The circuit of Fig. 6 as well as determines a phase noise portion from the static tuning input. When either of the driving transistors (M3 or M4) is turned on, its channel resistance generates thermal noise:

$$\overline{V_n^2} = 4KTR\,\Delta f \tag{6}$$

where $\overline{V_n^2}$ is the root-mean-square (rms) open-circuit noise voltage generated by the driving resistance R over the bandwidth Δf at a given temperature T, and k is Boltzmann's constant.

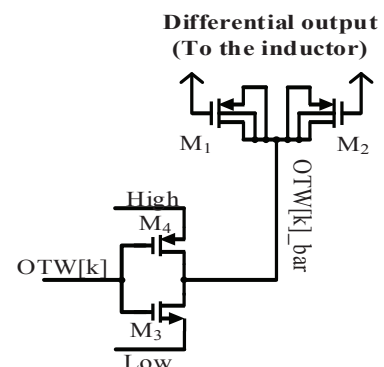Figure 4. Proposed CMOS LC-DCO under investigation

Figure 6. Differential varactor and an inverting driver

Proposed DCO output is a periodic waveform whose frequency f is a function of the input oscillator tuning word (OTW).

B. Proposed DCO Performance

In Fig. 4, the proposed LC-DCO has additional MOS transistors M_5 and M_6 that are connected to the source of the two cross-coupled transistors M_1 and M_2, respectively. The gates of M_5 and M_6 are connected to the output of digitizer1 and digitizer2, respectively. Digitizer1 and digitizer2 are two buffer to digitize output signal. This leads to M_5 or M_6 completely becomes in triode mode or cut-off region, in a half cycle. The gate-drain voltages of M_3, M_4 are $V_{Op}-V_{On}$ and $V_{On}-V_{Op}$, respectively. Due to the symmetry of the differential structure, the gate-drain voltages are equal in magnitude but opposite in signs. When the differential output waveform $|V_{Op}-V_{On}|$ is near to zero, so that both M_3 and M_4, similarly, M_1 and M_2 operate in saturation region, but M_5 and M_6 operate in triode or cut-off region. With raise in output voltage swing, for example, during the first half oscillation cycle, when $V_{Op}-V_{On}$ raises above the threshold voltage of NMOS transistor (V_t), the gate-drain of M_3 exceeds $+V_t$, forcing M_3, similarly, M_2 and M_5 into triode mode operation. While the gate-drain of M_4 falls below $-V_t$, driving M_4, similarly, M_1 deeper into saturation mode operation and M_6 is cut-off. In the next half oscillation, M_1, M_4 and M_6 operate in triode mode and M_2 and M_3 operate in saturation mode and M_5 is cut-off. Therefore over the complete oscillation cycle, both of the switch transistors M_5 and M_6 are performed as a one transistor that always operate in triode mode. The conventional LC-DCO cannot improve the phase noise performance because it has the constant bias transistor (that always operate in saturation mode) which is known as the main noise contributor of the cross-coupled LC-DCO. Also the transistor in triode mode operation has less flicker noise rather than the transistor in saturation mode operation [16]. The carriers movement under the gate oxide has an important contribution to determine flicker noise in a MOSFET. So constant bias transistor has more flicker noise than switching transistor [17]. As mentioned above, M_5 and M_6 use two method first switching transistors and second acts as a transistor that always operate in triode mode. Because of lower flicker noise in both method, it is expected, phase noise is decreased.

C. The Capacitance of C_P (Phase Noise Improvement)

We are considered parasitics capacitance and modeled our LC-tank in Fig. 7. The quality factor of the inductor, capacitor and whole parasitic capacitance are assumed Q_L, Q_C and Q_P that are modeled by parallel resistance, as shown in (7), (8) and (9) equations.

$$R_{PL} = \omega L Q_L \tag{7}$$

$$R_{PCP} = \frac{Q_P}{\omega C_P} \tag{8}$$
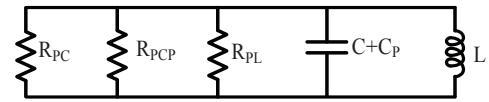
$$R_{PC} = \frac{Q_C}{\omega C} \tag{9}$$

Figure 7. LC-tank of proposed DCO

C_P demonstrates the capacitance caused by the whole parasitic capacitance of digitizer, the switching devices and the losses parallel resistance. According to equations (7), (8) and (9), the parallel quality factor of Fig. 7 calculated as follow:

$$Q_{parallel} = \cfrac{1}{\cfrac{\omega L}{\omega L Q_L} + \cfrac{1}{\omega(C+C_p)}\left(\cfrac{\omega C_P}{Q_P} + \cfrac{\omega C}{Q_C}\right)} \tag{10}$$

Equation (10) demonstrate that relationship between parallel total quality factor and whole parasitic capacitance is inverse of each other. In other word, the less parasitic capacitance in the circuit have higher the total quality factor and then better phase noise, according to the equation (5). For this purpose, we utilize a big capacitance in parallel with the M_5 and M_6 transistors to reduce effect of parasitics capacitance, as shown in Fig. 4.

D. Start up condition

Using smaller active devices lead to less parasitic capacitance and thus better phase noise function. Nevertheless, smaller active devices may produce not enough negative conduction and results in start-up obstacle in the oscillator. Accordingly, the start up circuit can be utilized. As shown in Fig. 8, two transistors M_7 and M_{10} are always on, the current coming to gate-source capacitance (C_{gs}) of M_8 and the current getting out of C_{gs} of M_{11}. After a short time, M_8 and M_{11} become on and lead to M_2 and M_3 become on, respectively. After several oscillations cycle, through the positive feedback, the DCO begins to oscillate.
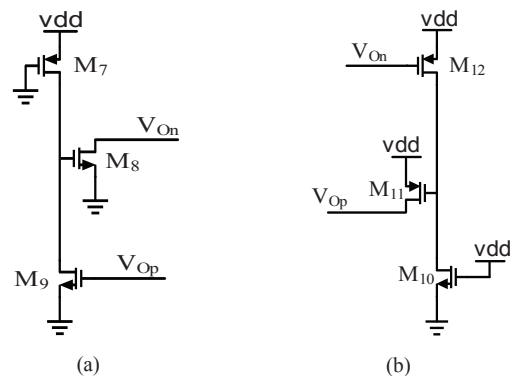

Figure 8. start up circuit (a). Left side (b). Right side

IV. SIMULATION RESULTS

The proposed complementary CMOS LC-DCO is designed and simulated by the Cadence IC Design based on 90 nanometer CMOS technology. The circuit is simulated in three corner case of technology means NMOS Fatst PMOS Fast at -40ºC, NMOS Typical PMOS Typical at 27ºC and NMOS Slow PMOS Slow at 85ºC. Also phase noise performance is shown under varying the supply voltage from 0.9 volt to 1.2 volt in table I.

TABLE I.   MEASURED PHASE NOISE OF THE DCO

Vdd (V)	Corner Case	Phase noise of conventional DCO (dBc/Hz)	Phase noise of proposed DCO (dBc/Hz)
		@ 1MHz Offset Frequency	
1.2	FF@-40°C	-107.4	-115.5
	TT@27°C	-107.2	-116
	SS@85°C	-107.7	-115.3
1.1	FF@-40°C	-106.3	-115.4
	TT@27°C	-106.1	-114.7
	SS@85°C	-106.5	-114
1	FF@-40°C	-105	-115
	TT@27°C	-105.7	-114.3
	SS@85°C	-106.1	-112.6
0.9	FF@-40°C	-104.1	-113.8
	TT@27°C	-103.9	-112.9
	SS@85°C	-104.4	-112

The total power dissipation of the presented DCO at state TT@27°C is 4.9 mw while operates at the 1.2 V supply voltage. The phase noise performance of the proposed and conventional DCO is depicted in Fig. 9, which proposed DCO giving -116 dBc/Hz at 1 MHz offset from the carrier frequency of 10 GHz.
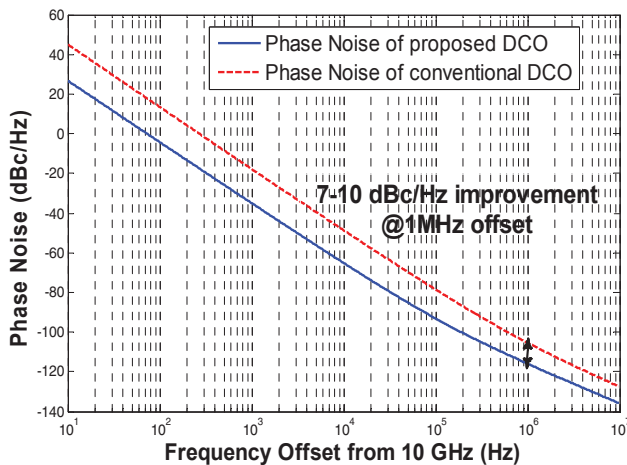

Figure 9. Measured phase noise of the DCO

The tuning word of varactor for 3-bit OTW is examined and results is presented in table II.

TABLE II.   FREQUENCY TUNING PERFORMANCE FOR 3-BIT OTW

OTW	Freq (GHz)	@1MHz Offset
000	10.018	-115.92
001	10.135	-115.64
010	10.254	-115.33
011	10.386	-115.09
100	10.447	-114.85
101	10.539	-114.69
110	10.671	-114.47
111	10.722	-114.21

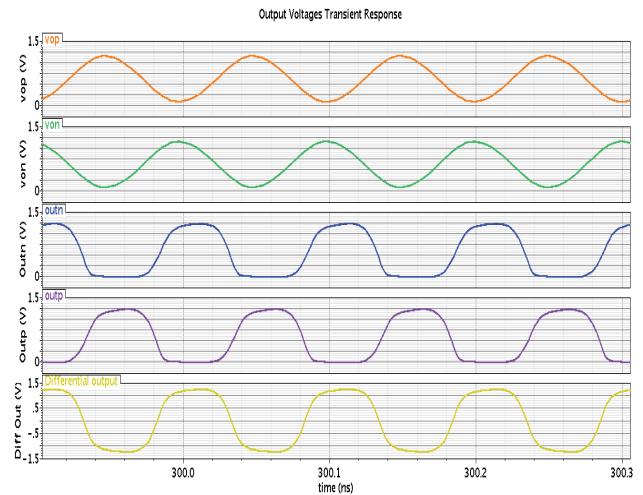The transient analysis for this DCO is shown in Fig. 10.

Figure 10. Transient analysis

The layout of inductor is in a symmetric method between Vop and Von to reduce the mismatch. Fig. 11, shows the layout of proposed DCO.
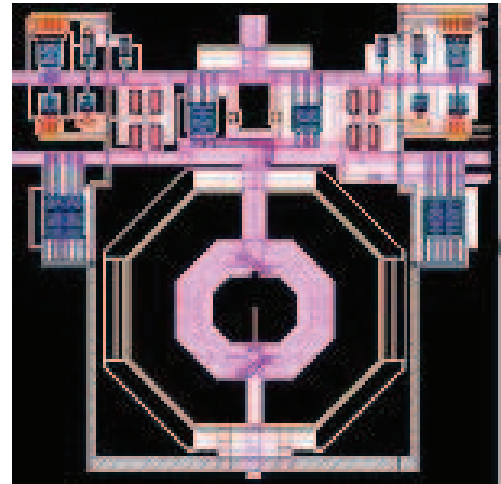

Figure 11. View of DCO layout consist of two spiral inductors with quality factor 17

Table III compares the proposed DCO with recent works, with respect to the center frequency, phase noise at 1 MHz offset from the carrier, power dissipation, tuning range, FOM and the utilized technology, which shows great improvement in this work especially in terms of phase noise value. In order to provide better comparison, Figure of Merit (FOM) for the DCO performance is used as Eq. (11)

$$FOM = \mathcal{L}[\Delta\omega] - 20\log[\frac{\omega_0}{\Delta\omega}] + 10\log[\frac{P_{DC}}{1mW}] \qquad (11)$$

Where £$[\Delta\omega]$ is the measured phase noise at the offset frequency of $\Delta\omega$, from the carrier at ω_0, and P_{DC} represents the DC power dissipation in mW. The FOM's value of the proposed DCO is -189 dBc/Hz at 1 MHz offset from 10 GHz center frequency which is not acquired before.

TABLE III. PERFORMANCE COMPARISON OF THE PROPOSED DCO AND SOME RECENT WORKS

Ref.	[18]	[19]	[20],[21]	Conventional	This work
Tech.	65 nm CMOS	90 nm CMOS	55 nm CMOS	90 nm CMOS	90 nm CMOS
Supply (V)	1.1	1.4	1.5	1.2	1.2
f_{osc} (GHz)	10	3.6	9	10	10
Tune range	10%	10%	10%	7%	7%
$\mathcal{L}$ (dBc/Hz)	-102	-127	-116	-107.2	-116
Offset Δf	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz
P_{diss}	3.3mW	25.2mW	9mW	10mW	4.9mW
FOM (dBc/Hz)	-177.2	-184	-185.6	-177.2	-189

V. CONCLUSION

In this paper, an integrated differential 10 GHz CMOS LC-DCO applied for ADPLL communication systems in radiolocation band frequencies based on 90 nm CMOS technology has been proposed. An effective technique in which two switching transistors are used is proposed, especially in order to develop the Phase noise requirement for ADPLL application. Also using two digitizer helps to switching top transistors operate in triode mode and achieve low power consumption without reduction of the phase noise. Simulation results illustrate considerable improvement in the characteristics of the proposed structure in which the phase noise value is -116 dBc/Hz at 1 MHZ offset from the carrier frequency with the 7% tuning range, under the supply voltage 1.2 V, the FOM value is -189 dBc/Hz while the circuit dissipates 4.9 mW power. the author's best knowledge, the proposed structure achieves the best phase noise in comparison with other DCOs.

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