# A Novel CMRR Enhancement Technique in Fully-Differential Class-AB OTAs

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***Abstract*—In this paper, a novel method of improving the Common-mode Rejection Ratio (CMRR) and Slew Rate (SR) of Operational Transconductance Amplifiers (OTAs) has been proposed. Our scheme suggests the elimination of the tail current source in class-A OTAs with the goal of SR enhancement and proposes a novel and intuitive CMRR enhancement technique to counteract the negative effect of the eliminated tail current source. One major advantage of our proposed scheme is its ability to be easily incorporated into various OTA architectures. Circuit-level simulations have been carried out using 180 nm CMOS technology with HSPICE. Our simulation results show that the resulting OTA from our technique exhibits a 2.38-time increase in SR and a 30 dB CMRR enhancement compared to the initially considered circuit, while maintaining approximately the same values in other metrics.**

***Index Terms*—Operational Transconductance Amplifier, CMRR Enhancement , SR enhancement, class-AB OTAs**

## I. Introduction

Operational transconductance amplifiers are an essential building block in analog integrated circuit design, making them essential for the increasing presence of electronic devices in people's day-to-day lives. In recent decades, with the continued downscaling of transistor sizes, designing an OTA with optimal speed and accuracy characteristics has become increasingly more challenging [1], [2]. In terms of speed-related parameters, SR is assumed to be one of the most important, particularly in switched-capacitor OTAs. Also, regarding the accuracy of an OTA, the CMRR parameter can be considered to be one of the most descriptive and intuitive parameters in differential circuits.

OTAs can be categorized into two types based on their mode of operation, namely class-A, and class-AB. Generally speaking, class-A amplifiers exhibit favorable CMRR, while experiencing some shortcomings in terms of their SR. On the other hand, class-AB amplifiers can be considered to be generally better in terms of SR, while exhibiting inferior performance in terms of CMRR characteristics. Accordingly, a trade-off can be witnessed between the SR and CMRR parameters of class-A and class-AB OTAs.

Transitioning from class-A to class-AB operation can be considered an easy way to obtain an increase in the SR of OTAs. However, regarding CMRR enhancement, the process can be more complex as it requires modifications to the architecture of the amplifier. In [3], an auxiliary amplifier block is employed within the circuit to create a dependency between one of the currents of the output branch and the common-mode input, $v_{cm}$. Hence, by choosing appropriate values for the auxiliary amplifier, it has been shown that it is possible to offset the common-mode signal before it reaches the output nodes, causing a degraded common-mode gain and an increase in CMRR. In [4], a local feedback block has been employed with the goal of ridding the small-signal currents at the output branches of the OTA of their dependency on the common-mode input. In [5], it has been proposed to add a transistor to some of the input branches of the initial circuit, and it has been shown that by doing so, it is possible to offset the common-mode signal at the input stage of the OTA. Although CMRR enhancement techniques have been discussed extensively in the literature, to the best of our knowledge, no previous work has proposed a systematic means of enhancing both the SR and CMRR of OTAs. Additionally, the methods within the literature are usually only applicable to the specific and pre-determined OTA architectures upon which the proposed method itself is introduced, and therefore, these methods cannot be easily generalized and incorporated into other OTA topologies. This inherent shortcoming translates into a limited generalization of the available methods, whereas our proposed scheme can be easily applied to various OTA architectures, due to its lack of assumptions on circuit architecture and simplicity.

In this paper, we start by considering a class-A OTA architecture and elaborating on how it's possible to increase the SR of the amplifier by eliminating its tail current source. In doing so, we show that we will be left with a class-AB OTA with an unacceptably enhanced common-mode gain, which results in a degraded CMRR value. Afterward, to alleviate the problem of degraded CMRR, we propose incorporating an intuitive and generalizable "CMRR Booster" module which can offset the input common-mode small-signal current at the input branch, long before it gets the chance to be amplified by the OTA. Consequently, we are able to benefit from the

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favorable SR values of class-AB OTAs, while maintaining a CMRR comparable to, or possibly better than, their class-A counterparts.

The rest of the paper is organized as follows. Section II provides a brief introduction to class-A and class-AB OTAs and discusses some of their benefits and drawbacks. Section III elaborates on our proposed method and the intuition behind it. Simulation results have been reported in section IV, and conclusions are drawn in section V.

## II. Background

In this section, we provide an overview of class-A and class-AB amplifiers and point out the shortcomings in each architecture. By doing so, we hope to provide the necessary information to elaborate on the main idea of this paper.

### A. Class-A Amplifiers

Class-A amplifiers are the most commonly used in the literature, in which the input-stage transistors are biased using a single tail current source, $I_b$, and various current mirroring techniques. The biasing current is usually kept to a minimum with the goal of keeping the amplifier's transistors in saturation while maintaining a low power consumption. Interestingly though, the main limitation of this class of amplifiers is inherently due to their incorporation of the tail current source, usually denoted by $I_b$ or $I_{tail}$, which limits the maximum rate at which the output voltage can change, i.e. slew rate. To illustrate, a simple class-A amplifier is shown in Fig. 1(a) and its corresponding AC equivalent circuit can be seen in Fig. 1(b). Note that $R_{cm}$ represents the equivalent AC resistance of a non-ideal tail current source, $I_b$.

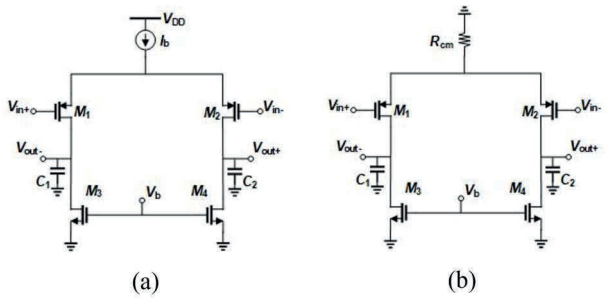


Fig. 1. A class-A amplifier (a), and its corresponding AC circuit (b)

The slew rate and common-mode gain of the amplifier in Fig. 1 are:

$$SR^+ = SR^- = \frac{I_b}{C_1} \tag{1}$$

$$A_{cm} = \frac{v_o}{v_{cm}} = -\frac{g_{m1}}{\left(\frac{1}{r_{ds1}\|r_{ds3}}\right) + \frac{2R_{cm}}{r_{ds1}r_{ds3}}\left(1 + g_{m1}r_{ds1}\right)} \tag{2}$$

As seen in (1), the slew rate's limitation is due to the $I_b$ term which basically restricts the value of the SR, as it is typically designed to be small in order to keep overall power consumption low.

### B. Class-AB Amplifiers

Class-AB amplifiers are an extension of class-A, in which the dependence of circuit biasing to the tail current source, $I_{tail}$, is alleviated either by removing $I_{tail}$, or by the use of novel biasing schemes such as flipped voltage followers (FVFs) [6]. These amplifiers exhibit a "Push-Pull" characteristic when faced with large inputs. The $SR$ of these amplifiers have the potential to be significantly larger than their class-A counterparts, as they leverage the non-linear nature of a transistor's current when faced with a large enough input, while not being limited by a small tail current, $I_{tail}$ at the input stage. However, this class of amplifiers normally suffers from an increased common-mode gain, $A_{cm}$, which degrades their differential performance by reducing their associated CMRR value. As an example, class-AB operation can be achieved by removing $I_b$ from Fig. 1(a) and connecting the sources of $M_{1,2}$ to $V_{DD}$, as shown by Fig. 2.

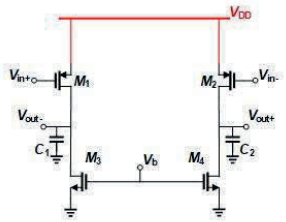


Fig. 2. Class-AB amplifier resulting from eliminating $I_b$ in Fig. 1(a)

As a result, the SR of the amplifier will no longer be restricted by the tail current source, enabling the amplifier to leverage the non-linear nature of CMOS currents when a large enough input voltage is applied.

The common-mode gain of the resulting circuit can be shown to be:

$$A_{cm} = \frac{v_o}{v_{cm}} = -g_{m1}(r_{ds1}\|r_{ds3}) \tag{3}$$

The major disadvantage of these class of amplifiers can be seen by comparing (2) and (3). From these equations, we see that the common-mode gain of the class-AB amplifier is significantly larger than its class-A counterpart, which is due to the absence of the tail current source's $R_{cm}$ in the AC equivalent circuit of Fig. 2. This large common-mode gain deteriorates the differential performance of class-AB amplifiers by reducing their CMRR. Therefore, developing methods to address the degraded CMRR of class-AB amplifiers can be considered beneficial, as they can enable us to leverage the enhanced SR associated with class-AB operation while maintaining a comparable CMRR to class-A amplifiers.

## III. Proposed Method

To elaborate on our proposed method, we first start by considering a class-A amplifier, shown in Fig. 3, and converting it into a class-AB amplifier by omitting the tail current source and connecting the sources of $M_{1,2}$ to $V_{DD}$, resulting in Fig. 4.

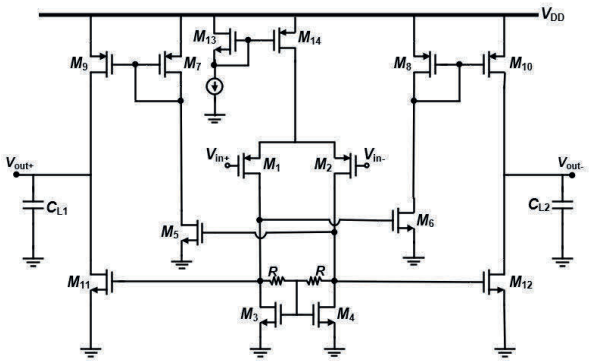


Fig. 3. Our initially considered class-A OTA

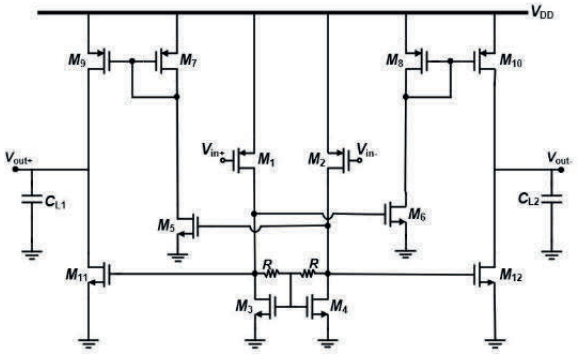


Fig. 4. Class-AB OTA resulting from the elimination of input stage's biasing elements in Fig. 3

Fig. 5 is used to provide an intuitive explanation of the CMRR degradation problem in class-AB amplifiers. Subsequently, we propose a "CMRR-booster" to address the illustrated issue. One advantage of our work is that the proposed "CMRR-booster" is a generalizable module that can be easily incorporated into other topologies of class-AB amplifiers.

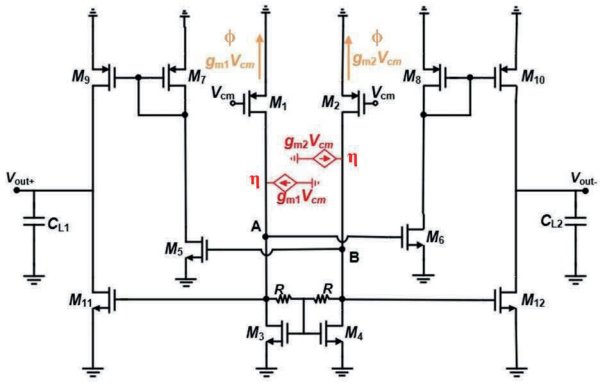


Fig. 5. Eqv. AC circuit of Fig. 4 in common-mode analysis. The currents in "orange" depict the CMRR degrading common-mode currents, and the dependent current sources in "red" illustrate the conceptual operation of our proposed scheme in compensating the "orange" currents before they are amplified by the circuit

### A. Our Considered Class-AB Amplifier

Fig. 4 shows our considered class-AB amplifier, which is the result of eliminating the tail current source from the input stage of Fig. 3 and connecting the sources of $M_{1,2}$ to $V_{DD}$. To provide a large-signal analysis of the proposed circuit, assume that a large step is applied to either input of the amplifier. In doing so, a large exponential current source, $I_{SR}$, starts to flow from the source of the transistor to which the input step has been applied. $I_{SR}$ has to pass through $M_3$ and $M_4$, and since these two transistors have identical gate-source voltages, the current is split in half, and thus, $I_{SR}/2$ passes through the two resistors between the drains of $M_3$ and $M_4$. This causes a voltage difference of $RI_{SR}$ between the drains of $M_3$ and $M_4$ which is in turn, sensed by the gates of $M_{5,6}$ and $M_{11,12}$, causing a large slew rate to be formed, quadratically proportional to $RI_{SR}$. Moreover, when considering the small-signal analysis of the circuit, the differential and common-mode gain of Fig. 4 can be shown to be equal to (4) and (5), respectively. According to (5), this structure suffers from a potentially large common-mode gain, due to the sources of $M_{1,2}$ being connected to the virtual ground in the equivalent common-mode small-signal circuit, allowing a small-signal current, $g_{m1}v_{cm}$ and $g_{m2}v_{cm}$ to be formed at the sources of $M_1$ and $M_2$ respectively.

$$A_{diff} = \frac{v_{o+} - v_{o-}}{v_{i+} - v_{i-}} = (g_{m2})(g_{m12} + \frac{g_{m10}}{g_{m8}} g_{m6})(r_{ds10} \| r_{ds12})R \tag{4}$$

$$A_{cm} = \frac{v_o}{v_{cm}} = (\frac{-g_{m2}}{g_{m4} + (\frac{1}{r_{ds2} \| r_{ds4}})})(\frac{g_{m10}}{g_{m8}} g_{m6} - g_{m12})(r_{ds10} \| r_{ds12}) \tag{5}$$

### B. Intuition Behind Our Proposed Method

In this subsection, we provide an intuitive explanation on why the CMRR of class-AB amplifiers is inferior in comparison to class-A and discuss our proposed method of addressing this issue. Consider Fig. 5, which is the equivalent AC circuit of Fig. 4 in common-mode operation. The currents in orange, denoted by $\phi$, start to flow due to the input signal $v_{cm}$. Without the presence of any means of compensation for these currents, they will inevitably be amplified by the circuit and make their way to the output node, causing a large common-mode gain. On the contrary, in class-A operation, due to the presence of an equivalent resistor, similar to $R_{cm}$ in Fig. 1(b), representing the tail current source in the small-signal regime, only a negligible current of $v_{cm}/2RI_b$ will be created instead of the large $g_m v_{cm}$. Therefore, in simple terms, the root cause of the degraded CMRR in class-AB operation is the presence of the $g_m v_{cm}$ current at the input stage, during common-mode analysis, which results in a large transconductance at the output node.

To address the problem, we propose designing a module to compensate the orange currents in Fig. 5 (shown using $\phi$), as

depicted by the red dependent current sources (shown using $\eta$), long before they get the opportunity to be amplified by the circuit. By doing so, we prevent the orange currents (shown using $\phi$) from flowing into $M_{3,4}$, and stop the amplification of the common-mode signal, $v_{cm}$, at the input stage of the circuit. Note that the proposed module should be active in common-mode operation, sensing the common-mode signal, $v_{cm}$, and generating a compensating current to prevent its amplification, while having a negligible effect in differential mode, as it could deteriorate the performance and the initial design specifications of the amplifier. We name the red module (shown using $\eta$) "CMRR booster" because it enhances the CMRR by minimizing the common-mode gain while having a negligible effect on the differential-mode operation.

### C. Proposed CMRR Boosting Scheme

This section discusses our implementation of the red current sources in Fig. 5 (shown using $\eta$), the roles of different sections within the proposed architecture, and a methodology for finding its device sizes. The blue elements depicted in Fig. 6, namely $R_{3,4}$ and $M_{13,14,15,16,17,18}$, show our proposed implementation. These elements can be subcategorized into four sections, namely "sensing", "signal inversion", "current generation", and "biasing".

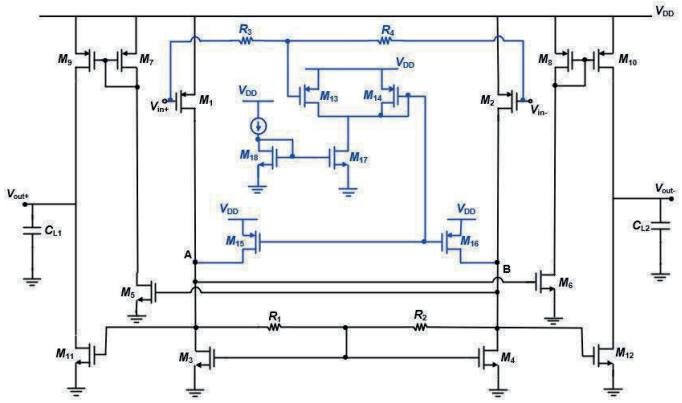


Fig. 6. The final OTA incorporating our proposed CMRR booster, depicted by the blue elements within the circuit. The blue elements effectively realize the operation of the red dependent current sources in Fig. 5, compensating the CMRR degrading common mode currents.

The two resistors, $R_{3,4}$, in Fig. 6 constitute the "sensing" portion of our architecture. By assigning them an equal value, the voltage at their junction node will be equal to the average of the two input nodes, $V_{in+}$ and $V_{in-}$. Therefore, these two resistors will be able to sense the biasing voltage and the common-mode signal of the input nodes, namely $V_{in+}$ and $V_{in-}$, and make them available at their junction node. Note that when considering a differential operation, as the two input signals are complementary by definition, the junction node of the two resistors will essentially be a virtual ground, and consequently, the "sensing" section of our proposed architecture will be indifferent to differential signals at the input. This inability to sense differential signals is actually advantageous, as we're normally aiming to minimize the common-mode gain of an amplifier while having a negligible effect on its initially designed differential specs. The two transistors, $M_{13}$ and $M_{14}$, in Fig. 6 depict the "signal inversion" section of our architecture, and are tasked with generating the inverse of the sensed common-mode signal, i.e. $-v_{cm}$, which will, in turn, be used by the "current generation" section, namely $M_{15}$ and $M_{16}$, to create the required common-mode compensation current. Lastly, $M_{17}$ and $M_{18}$ constitute the "biasing" section of our architecture. Assuming equal values for the two resistors, $R_3$ and $R_4$ in Fig. 6, the necessary conditions that need to be met for the CMRR-booster to work are shown in (6) and (7):

$$A_{inv} = -g_{m13}\left(\frac{1}{g_{m14}} \| r_{ds13} \| \, r_{ds14} \| r_{ds17}\right) = -1 \tag{6}$$

$$\begin{aligned} g_{m1} &= g_{m15} \\ g_{m2} &= g_{m16} \end{aligned} \tag{7}$$

Equation (6) indicates that the gain of the "signal inversion" section should be equal to $-1$ in order to ensure that the input common-mode signal is inverted. Moreover, the conditions in (7) are to ensure that the appropriate currents are generated by $M_{15}$ and $M_{16}$ for common-mode compensation.

In order to find the appropriate parameters for the elements within our architecture, i.e. device sizes that satisfy the conditions in (6) and (7), we can start by focusing on the fact that the two resistors sense the biasing voltage and the common-mode signal of the inputs at their connection node. As a result, it can be inferred that the DC voltage on the gate of $M_{13}$ is equal to the gate voltage of the input transistors and we can consider them to be current mirrors. By doing so, the biasing current of $M_{13}$ is set using (8):

$$I_{M_{13}} = \frac{(W/L)_{13}}{(W/L)_{1\&2}} I_{M_{1\&2}} \tag{8}$$

Using the simplifying assumption $(r_{ds13} \| r_{ds14} \| r_{ds17}) >> 1/g_{m14}$, we can assume that we should have $g_{m13} = g_{m14}$ for (6) to be satisfied. To do so, we can start by assigning $(W/L)_{13} = (W/L)_{14}$ and assuming equal currents for $M_{13,14}$, which can be achieved by initially setting the bias current for $M_{13}$ using (8) to be equal to the currents of $M_{1,2}$, and then, determining the current of $M_{17}$ using its current mirror ratio with $M_{18}$, such that its current will be twice that of $M_{13}$. By doing so, we can assure that $A_{inv} \approx -1$ and that (6) is satisfied. Regarding the satisfaction of (7), we can argue that since we've assumed identical currents and $(W/L)$ values for $M_{1,2}$ and $M_{13,14}$, the DC value of their source-gate voltage is approximately equal. Accordingly, since $V_{SG14} = V_{SG15,16}$, we assume that $M_1$ and $M_2$ have a current mirror with $M_{15}$ and $M_{16}$ respectively. Under this assumption, we can simply set the $(W/L)$ ratio for $M_{15,16}$ to be identical to that of $M_{1,2}$ for (7) to be satisfied, and with that, we can conclude the design of the proposed module. As is evident, our proposed method of CMRR enhancement by common-mode gain mitigation is generalizable and can be incorporated into

a variety of class-AB architectures, without majorly altering their previously designed specs.

When using our proposed method, it should be noted that since the drains of $M_{15,16}$ are connected to the nodes $A$ and $B$ in Fig. 6 respectively, their biasing currents need to be sinked using $M_{3,4}$. Consequently, this intricacy can change the originally designed bias point of the amplifier, and therefore, cause a divergence between the amplifier's actual performance and its original design expectations. In other terms, when incorporating our proposed method, the current-sinking transistors of the input stage, $M_{3,4}$, will be tasked with sinking twice the current they were initially designed to sink. To alleviate this problem with minimal alternation of our amplifier's original design, we can simply double the effective $(W/L)$ of $M_{3,4}$. By doing so, the gate-source voltage, $V_{GS}$, of $M_{3,4}$ will remain unchanged compared to its value prior to the incorporation of our "CMRR booster", and therefore, the initial design of the amplifier will remain intact.

## IV. Simulation Results

In order to show the problem of CMRR degradation, and the effectiveness of our proposed method in alleviating the problem, the amplifiers in Fig. 3, Fig. 4, and Fig. 6 have been designed and simulated using a 180 nm CMOS technology with HSPICE. We first designed and simulated the class-A amplifier in Fig. 3. Afterward, we simulated the circuit of Fig. 4 using the same parameters and dimensions that we had computed for Fig. 3, and in order to ensure a fair comparison, we set the input DC voltages of Fig. 4 such that its biasing current would be equal to that of Fig. 3. By doing so, we can show that the common-mode gain of the amplifier is increased when transitioning from class-A to class-AB operation, causing a large CMRR degradation. Subsequently, to demonstrate the effectiveness of our proposed method in alleviating the degraded CMRR problem, we simulated Fig. 6 and computed the parameters of our CMRR boosting elements using the methodology discussed in section III-C. In doing so, we kept the initially designed parameters and device dimensions for the initial amplifier of Fig. 4, with the exception of the $W/L$ values for the current-sinking transistors of the input stage in Fig. 6, i.e. $M_{3,4}$, which were doubled to keep the bias point of the elements intact after adding the CMRR boosting circuitry. One of the main advantages of our proposed method is the minimal required modification for the incorporation of our CMRR booster, as is evident from the previously explained procedure. Note that since the amplifiers operate in a fully-differential manner, a CMFB circuit is required to stabilize the output voltages. However, since the design of the CMFB was not the main goal of this project, an ideal CMFB circuit was used for the simulations. Moreover, the $SR$ of the initial class-A amplifier, as shown in Fig. 3, and the final class-AB OTA incorporating the proposed CMRR-booster, as in Fig. 6 have been reported as well. To perform the transient analysis, the amplifiers were used in a fully-differential sample-and-hold configuration, while driving an effective load capacitance of $C_L = 2pF$, with a sampling capacitance of $C_S = 1pF$.

The designed device dimensions for Fig. 3, and Fig. 6 are shown in Table I, and Table II respectively. The AC simulation results are summarized in Table III. To consider the transient characteristics of Fig. 3, and Fig. 6, a $1V$ input step was applied to the amplifiers' input, which resulted in the settling diagrams shown in Fig. 7. According to Fig. 7, the $SR^+/SR^-$ of our designed class-A circuit of Fig. 3 is equal to $421/419(V/\mu Sec)$, while the class-AB version in Fig. 6 exhibits an $SR^+/SR^-$ of $1003/1003(V/\mu Sec)$, indicating approximately 2.38 times increase in the slew rate of the amplifier when using our proposed method. The Monte Carlo analysis of the OTA in Fig. 6 can be seen in Fig. 8. Lastly, the harmonic analysis and total harmonic distortion (THD) computation results of Fig. 6 can be seen in Fig. 9.

TABLE I
Simulated device sizes of Fig. 3

| Element | W/L | $g_m$(mA/V) |
|---|---|---|
| $M_1$, $M_2$ | $4.4\mu m/0.18\mu m$ | 0.4 |
| $M_3$, $M_4$ | $1.3\mu m/0.18\mu m$ | 0.4 |
| $M_5$, $M_6$ | $1.3\mu m/0.18\mu m$ | 0.4 |
| $M_7$, $M_8$ | $8.6\mu m/0.36\mu m$ | 0.34 |
| $M_9$, $M_{10}$ | $17\mu m/0.36\mu m$ | 0.7 |
| $M_{11}$, $M_{12}$ | $5.2\mu m/0.36\mu m$ | 0.9 |
| $M_{13}$ | $0.88\mu m/0.18\mu m$ | 0.07 |
| $M_{14}$ | $9.6\mu m/0.18\mu m$ | 0.6 |
| $C_{L1}$, $C_{L2}$ | 1.5 pF | |
| R | 5 kΩ | |

TABLE II
Simulated device sizes of Fig. 6

| Element | W/L | $g_m$(mA/V) |
|---|---|---|
| $M_1$, $M_2$ | $4.4\mu m/0.18\mu m$ | 0.4 |
| $M_3$, $M_4$ | $2.4\mu m/0.18\mu m$ | 0.7 |
| $M_5$, $M_6$ | $1.3\mu m/0.18\mu m$ | 0.4 |
| $M_7$, $M_8$ | $8.6\mu m/0.36\mu m$ | 0.34 |
| $M_9$, $M_{10}$ | $17\mu m/0.36\mu m$ | 0.69 |
| $M_{11}$, $M_{12}$ | $5.2\mu m/0.36\mu m$ | 0.9 |
| $M_{13}$ | $1.1\mu m/0.18\mu m$ | 0.08 |
| $M_{14}$ | $1.1\mu m/0.18\mu m$ | 0.07 |
| $M_{15}$, $M_{16}$ | $4.9\mu m/0.18\mu m$ | 0.4 |
| $M_{17}$ | $0.64\mu m/0.18\mu m$ | 0.16 |
| $M_{18}$ | $0.32\mu m/0.36\mu m$ | 0.05 |
| $C_{L1}$, $C_{L2}$ | 1.5 pF | |
| $R_1$, $R_2$ | 5 kΩ | |
| $R_3$, $R_4$ | 100 kΩ | |

TABLE III
Summary of Simulation Results

| | Simulation Results | | |
|---|---|---|---|
| | ***Fig. 3*** | ***Fig. 4*** | ***Fig. 6 (Ours)*** |
| Differential Gain $A_{diff}(dB)$ | 42.69 | 42.88 | 42.46 |
| Common Mode Gain $A_{cm}(dB)$ | $-70.09$ | $-51.43$ | $-100.87$ |
| Phase Margin $(degree)$ | 68.92 | 68.25 | 68.02 |
| Unity-Gain Freq. $(MHz)$ | 290.57 | 301.04 | 270.36 |
| Power $(\mu W)$ | 693.64 | 694.67 | 816.35 |

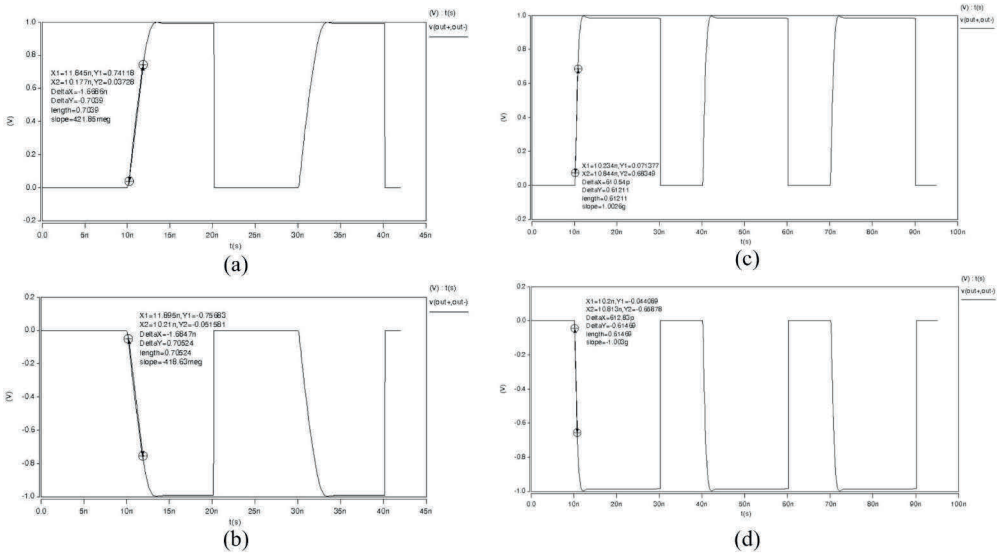


Fig. 7. The positive and negative settling diagrams of Fig. 3 are shown in (a) and (b) respectively, while the positive and negative step response of Fig. 6 are exhibited in (c) and (d). Note that the value of the "slope" variable in each of the images denotes the maximum rate of change of the output voltage.

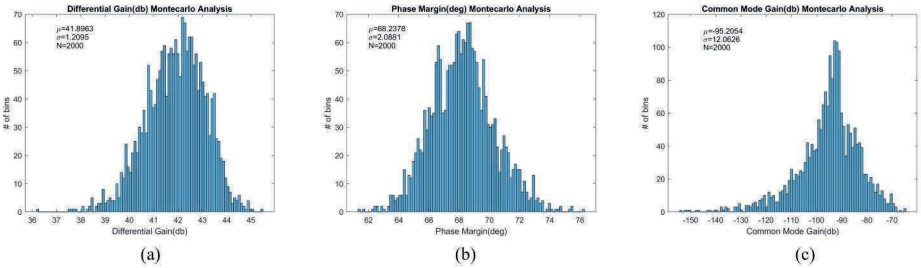


Fig. 8. Monte Carlo Analysis for $A_{diff}$ (a), Phase Margin (b), and $A_{cm}$ (c) of Fig. 6

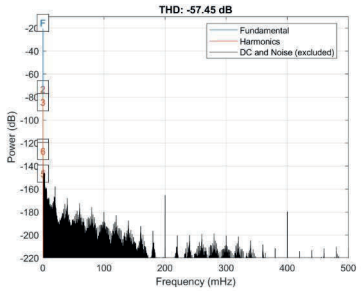


Fig. 9. Harmonic analysis and THD computation results of Fig. 6

## V. Conclusion

In this paper, the elimination of the biasing current source was proposed as a means of enhancing the SR of OTAs. Additionally, a novel, intuitive, and generalizable method of addressing the degraded CMRR, resulting from the bias current source elimination, was introduced. Simulation results demonstrated that, by using our proposed scheme, a 2.38-time increase in $SR$ and a 30 dB increase in the $CMRR$ of Fig. 6 has been achieved compared to the initial circuit of Fig. 3. Lastly, we've emphasized that our proposed scheme is not specific and limited to the circuit architectures discussed within this study, and can be easily incorporated into other OTA architectures as well, due to its simple and intuitive operation philosophy.

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