A Digital Background Correction Technique Combined with DWA for DAC Mismatch Errors in Multibit ΣΔ ADCs

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***Abstract*— A digital background correction technique combined with data weighted averaging (DWA) algorithm is presented to overcome the digital-to-analog converters (DACs) unit element mismatch errors in multibit sigma-delta modulators (ΣΔMs). This technique needs a background measurement process. The circuit-level simulation results confirm the validity of the measurement process and the system-level simulation results are provided to verify the usefulness of this correction technique in low oversampling ratios (OSRs). This method enhances the peak signal-to-noise and distortion ratio (SNDR) about 11.5 dB with respect to the DWA algorithm when the OSR is 8.**

I. INTRODUCTION

Using multibit quantization in sigma-delta modulators (ΣΔMs) enhances the stability and accuracy, relaxes the design of opamps, reduces the total quantization noise power, and helps the designer to decrease the oversampling ratio (OSR). Any decrease in OSR will lead to an increase in bandwidth provided that the reference clock of the system is fixed. Nonetheless, the unit elements of a multibit DAC, used in the feedback path, have inherent mismatches due to the fabrication processes. This limits the total accuracy of the modulator and results in harmonic distortion in the modulator's output spectrum since the outermost DAC mismatch errors are directly added with the input signal.

Several mismatch shaping algorithms have been presented thus far. DWA family and tree structure are examples of mismatch shaping algorithms [1, 2]. Using these mismatch shaping techniques, the DAC mismatch-induced errors can be adequately suppressed in the signal bandwidth if the OSR is sufficiently high (say, 16 or higher). However, in broadband applications where a low OSR should be used, the mismatch shaping techniques become ineffective even if a second-order mismatch shaping was employed [3]. A second order mismatch shaping technique (NS-DEM) is presented in [4]. It uses an accumulator and a differentiator before and after the feedback DAC, respectively, leading to a first order shaping. It also uses DEM and altogether has a second order mismatch shaping. As mentioned in [4], the accumulator is prone to overflow. The occurrence of the overflow depends on the input signal frequency and amplitude. The lower the frequency and the higher the signal amplitude, the more frequently it overflows. When overflow occurs frequently, the noise shaping is affected and hence the performance of the ΣΔM is degraded. Higher order mismatch shaping techniques also have significant latency. Using them in feedback path of ΣΔMs can cause instability when the sampling frequency is high. Hence, in wideband applications, the digital calibration and correction techniques can be used.

Digital calibration and correction techniques are good candidates for wideband applications [5, 6]. A digital correction technique based on the correlation method has been proposed in [5]. It calculates the correlation between the output signal and each of thermometer codes of DAC input to estimate the error of each unit element. The power spectral density (PSD) of output signal contains filtered PSD of both input signal and quantization noise. These two spectral contents affect both convergence time and accuracy of correlation process. In fact, the correlation convergence time and accuracy depend on the input signal. This correction technique also uses 2^N (N is the number of bits of the quantizer) digital filters to filter all thermometer codes with error transfer function (*etf*) of modulator, and 2^N real-time adders for correlation to estimate the errors. The proposed measurement technique of [6] needs hardware for minimization algorithm. It creates a notch in both noise transfer function (NTF) and signal transfer function (STF) outside the signal band, increases inband noise and changes the modulator's design.

In this paper a novel technique is proposed to estimate the DAC mismatch-induced errors. The correction time of this technique is exactly deterministic and does not depend on the input signal frequency and amplitude. This technique has excellent accuracy with low measurement time. It just requires a current source, a comparator, a counter and a divider to estimate the error. The correction part is similar to [5].

In Sect. II the idea of correction is described. The proposed error measurement idea is presented in Sect. III. In this Sect. the hardware requirements of the proposed technique are also expressed. The simulation results are presented in Sect. IV. Finally, Sect. V concludes the paper.

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II. PROPOSED CORRECTION TECHNIQUE

The block diagram of a multibit ΣΔM along with its DAC correction block is shown in Fig. 1. The modulator's output signal is given by:

$$y(k)=x(k)\otimes stf(k)+n_q(k)\otimes ntf(k) + \left(\sum_{i=1}^{M} b_i(k).e_i\right)\otimes etf(k) \quad (1)$$

where ⊗ is the convolution operator, $n_q(k)$ is the quantization noise, $\bar{e}$ is a vector of the DAC's errors, and $stf(k)$, $ntf(k)$ and $etf(k)$ are the impulse responses of $y(k)$ to $x(k)$, $n_q(k)$ and $\bar{e}$, respectively. In Fig. 1, $\bar{b}$ is a vector of quantizer output thermometer codes while $etf'(k)$ and $\bar{e}'$ denote the estimation of $etf(k)$ and $\bar{e}$, respectively. The vector $\bar{e}'$ will be obtained in the next section. The first term in (1) is the desired output. The second term is the shaped quantization noise whose effect in the signal bandwidth is negligible. The third term is the DAC's error transferred to the output.

The $\bar{b}$ and $etf'(k)$ are known. By estimating $\bar{e}$, we would be able to reduce the 3rd term in (1). The error cannot be eliminated unless the $etf(k)$ and $\bar{e}$ be measured exactly. In the proposed technique, this error is reduced and then the remaining part of the error is shaped by DWA. Using DWA reduces the sensitivity of the final result to the estimation accuracy of $\bar{e}$ and $etf(k)$. Measurement of $\bar{e}$ is sufficiently accurate but the estimation of $etf(k)$ is not so accurate. In a specific ΣΔM, $etf(k)$ is theoretically determined which differs from the real measurements because of the analog circuit non-idealities. Hence, the corrected output signal is given by:

$$y_{out}(k)=y(k)-\left(\sum_{i=1}^{M} b_i(k)e_i'\right)\otimes etf'(k) \quad (2)$$

If $|ETF'(e^{jw})| \approx 1$ over the signal bandwidth, then there is no need to implement $etf'(k)$. This condition is usually true in most ΣΔMs where a unity signal transfer function (STF) is employed due to advantageous properties of a unity STF [7]. Hence, in this case, the outermost DAC error transfer function is the same as STF. Therefore, the simulation results are reported with $etf'(k) = -1$.

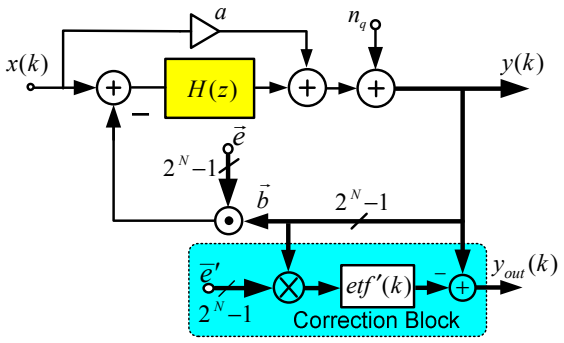

Figure 1. Linear model of a ΣΔM with its DAC correction circuit.

III. MEASUREMENT OF DAC's MISMATCH ERRORS

Assume an N-bit switched-capacitor DAC with 2^N-1 unit capacitors works as usual and an additional capacitor is used for measurement process. The nominal value of capacitors is C and the real value of j[th] capacitor is $C_j = C\times(1+e_j)$. Different values of capacitors cause different charging times of capacitors; therefore by measuring the charging time of all capacitors, their errors can be estimated. It takes 2^N measurement phases (φ_1 …, φ_{2^N}), to measure the error of all unit capacitors. Time duration of each measurement phase is T. During φ_j, C_j is selected for measurement and the additional capacitor takes its place. As illustrated in Fig. 2, firstly, C_j is discharged through M_1, when φ_d is high. After discharge of C_j at negative edge of φ_d, M_1 is turned off and the charging time, t_j, is started. During t_j, C_j is charged by the fixed current source, I_{ref} and capacitor voltage, V_C, linearly increases from zero to a specific voltage, V_{ref}, so we have:

$$V_C=\frac{1}{C_j}\int_0^{t_j} I_{ref}\,dt=\frac{1}{C_j}I_{ref}\,t_j=V_{ref} \quad (3)$$

During t_j, V_{out1} is high ($V_C < V_{ref}$) and φ_d is low; therefore, system clock pulses, CLK, is applied to a counter and the number of system clock pulses, a_j, is counted by the counter. When V_C exceeds V_{ref}, V_{out1} gets low and counter stops. At next positive edge of φ_d, the output of counter is latched by a digital unit to estimate the vector error $\bar{e}'$ by using (6) and C_j is discharged to be used in modulator at the end of φ_j.

As depicted in (4), t_j is proportional to C_j. Also, it is approximately an integer multiple, a_j, of the system clock period, T_{clk}.

$$t_j = \frac{1}{I_{ref}}C_j V_{ref}\approx a_j T_{clk} \quad (4)$$

where a_j is the integer number of clock pulses counted by counter in j[th] measurement time, and T_{clk} is the time period of system clock. There are 2^N different values ($a_1.a_2$ …, a_{2^N}) for different C_j (j=1, 2…, 2^N). a_1, a_2,…, a_{2^N} are the integer numbers approximately proportional to $(1+e_1)$, $(1+e_2)$,… and $(1+e_{2^N})$, respectively. The 2^N-th unit capacitor of DAC is used as the reference capacitor for correction. It means that the errors of other capacitors are normalized by the error of the 2^N-th capacitor. This is illustrated in (5). As an advantage, this normalization eliminates the effects of non-ideality of analog circuits, such as offset errors of both comparator and current source and gain error of $etf(k)$, on measurements.

$$\frac{1+e_j}{1+e_{2^N}}\approx\frac{a_j}{a_{2^N}},\quad j=1,2,...,2^N-1 \quad (5)$$

Assume $e_{2^N} \ll 1$ and hence $1+e_{2^N}\approx 1$, so the relation (5) can be rewritten as:

$$e_j' \approx \frac{a_j}{a_{2^N}} - 1, \quad j = 1, 2, ..., 2^N - 1 \tag{6}$$

where e_j' is the estimated value of e_j.

For example, assume V_{ref} = 0.4V, I_{ref} = 2nA and T_{clk} = 25ns, then C_j = 0.25×1.0022pF leads to a_j = 2004 and C_{2^N} = 0.25pF gives a_{2^N} = 2000. According to (6), e_j = 0.0022 results in e_j' = 0.002.

The accuracy of estimation of e_j' depends on the value of a_{2N}. Minimum error of e_j' is $1/a_{2N}$. The greater a_{2N}, the more accurate is e_j'. Considering (4), a_{2N} is directly proportional to V_{ref} and C_{2N}, and inversely proportional to I_{ref}. C_{2N} is fixed and V_{ref} is limited to less than V_{DD}. I_{ref} is the only free parameter. Any decrease in I_{ref} results in increasing of a_{2N}, and consequently the measurement accuracy increases.

The number of bits of counter (n_b) and the measurement time should satisfy (7) and (8), respectively. A good suggestion for the value of a_{2N} for measurement error less than 0.0005, could be 2000 results in n_b=11 and measurement time $2000\times2^N\times T_{clk}$.

$$2^{n_b} > \max(a_j) \quad \text{for} \quad j = 1, 2, \ldots, 2^N \tag{7}$$

$$T_{\text{measurement}} > \left(\sum_{j=1}^{2^N} a_j \right) \times T_{clk} \tag{8}$$

The proposed technique needs a comparator, a wide-swing cascode current source in nano ampere range, a counter, a divider and some switches. The comparator and the current source are common for measurement of all capacitors and their errors would not be important. So, the design of them as two analog parts of measurement circuit is not challenging at all. The current noise of analog circuit is negligible because the transistors of circuit have a very low gm. Also, considering (3), the current noise has no DC component to charge the capacitor. The other parts of measurement circuit are digitally implemented. As shown in Fig. 1, $etf'(k)$ should also be implemented. If $|ETF'(e^{jw})| \approx 1$ over the signal bandwidth then the $etf'(k)$ can be substituted by $etf'(k)$ = -1 (i.e. no digital filter is used). A phase generation unit is needed to generate the measurement phases. Also, a logic circuit is responsible for implementation of DWA.

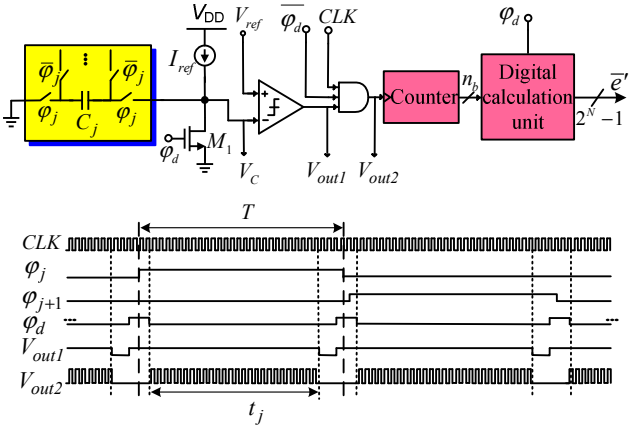

Figure 2. Capacitor measurement circuit.

IV. SIMULATION RESULTS

A circuit-level simulation was done in HSPICE to verify the validity of capacitor measurement of section III. 32 capacitors were used as capacitor bank of DAC with nominal value C = 0.25pF. 1.5% mismatch was introduced to capacitors. Alternatively, the value of capacitors was measured by the proposed circuit shown in Fig. 2 with V_{ref} = 0.4V, I_{ref} = 2nA and T_{clk} = 25ns. The standard deviation of difference between the real and measured values was 0.0003. This indicates that the measurement process has reduced the mismatch amount from 1.5% to 0.09%. According to (7) and (8), the number of bits of counter was n_b = 11 and the measurement time was less than $2000\times2^5\times25$ns. HSPICE simulation results for one of the capacitors is illustrated in Fig. 3. As shown in Fig. 3 that the capacitor voltage is charged linearly versus the time. Hence the simulated wide swing nano ampere current source (Fig. 2) worked correctly so it can be implemented in practice. The real and measured values of capacitors were used in the system-level simulations. The measured values were used in digital unit for correction and the real values were used as DAC's unit capacitors.

A single-loop 5th-order low pass ΣΔM with a 5-bit quantizer was simulated using MATLAB and Simulink to verify the validity of the proposed digital background correction technique. The input signal was a -4.4 dBFS sine wave with a frequency of f_s / 512 and an OSR of 8. Fig. 4 shows the modulator output spectrum in four different cases: real DAC, ideal DAC, real DAC with DWA algorithm and real DAC with the proposed correction technique. In Fig. 5 the SNDR versus the amplitude of input signal is shown when the ideal case, DWA algorithm and the proposed correction technique are separately utilized. Table 1 summarizes the simulation results for different mismatch values among the DAC unit elements, where the measurement time of both mismatch values is $2000\times2^5\times25$ ns.

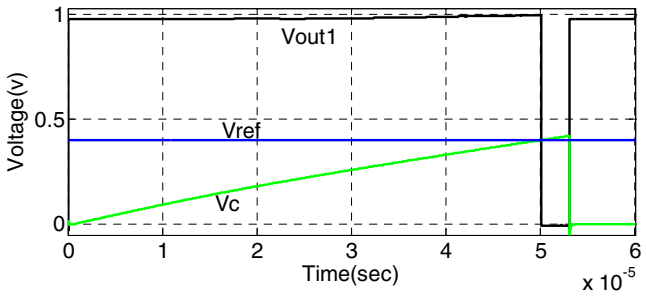

Figure 3. HSPICE simulation result of Fig. 2 for a unit capacitor (C = 0.25 pF).

V. CONCLUSIONS

A combination of DWA algorithm and a digital background correction technique was proposed to correct the DAC mismatch errors in multibit ΣΔMs. The proposed technique corrects the main part of the mismatch-induced errors in low OSRs where the error shaping techniques do not work properly. The remaining part is shaped by DWA algorithm. This combined technique approximately eliminates the nonlinear effects of DAC. Its advantage over DWA is more obvious when the amount of the mismatch is large. The error measurement part of this technique needs less than 2^{11+N} system clock periods.

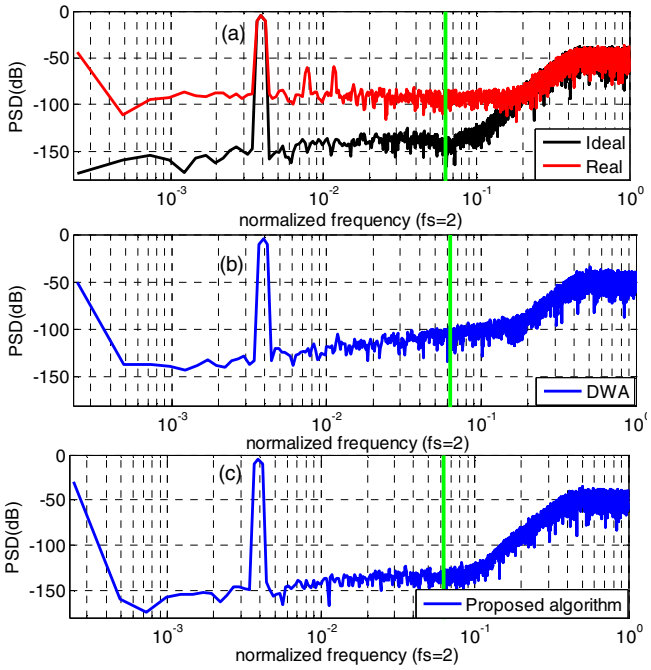

Figure 4. Output PSD with (a) ideal DAC and real DAC, (b) DWA DAC, and (c) proposed technique, (%1.5 Mismatch).

TABLE I. SUMMARY OF SIMULATION RESULTS.

DAC type	SNDR (dB)		SFDR (dB)	
	0.3% mismatch	1.5% mismatch	0.3% mismatch	1.5% mismatch
Real DAC	82.7	64.3	89.1	69.3
DWA	93.0	84.4	105.8	98.9
Proposed technique	96.0	95.9	108.4	108.0
Ideal DAC	96.5		109.4	

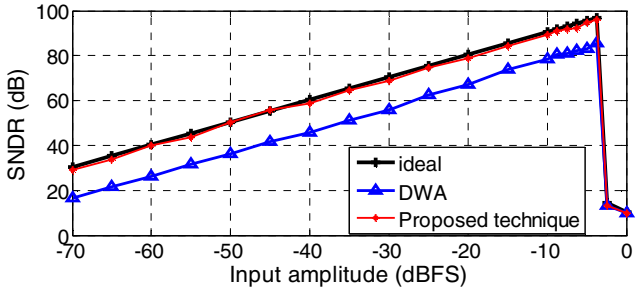

Figure 5. Simulated SNDR versus input signal amplitude

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