A Digital Calibration Technique Combined with DWA for Multibit ΣΔ ADCs

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***Abstract*— A purely digital correction technique combined with data weighted averaging (DWA) algorithm is presented to overcome the digital-to-analog converter's (DAC's) mismatch-induced errors in multibit ΣΔ modulators. This technique needs a foreground calibration process. Simulation results confirm the validity of this combined technique in low oversampling ratios (OSRs). This method enhances the pick signal to noise and distortion ratio (SNDR) about 31.5 dB with respect to the non-calibrated case (1.5 % mismatch) when the OSR is 8.**

Keywords-Multibit ΣΔ ADC; DAC mismatch error; calibration

I. INTRODUCTION

Using multibit quantization in sigma-delta modulators (ΣΔMs) enhances the stability and accuracy, relaxes the design of opamps, reduces the total quantization noise power and helps designer to decrease the over sampling ratio (OSR). Any decrease in OSR will lead to an increase in bandwidth, provided that the reference clock of the system is fixed. Nonetheless, the elements of multibit DAC, used in the feedback path, have inherent mismatches due to the fabrication process. This limits the total accuracy of the modulator and results in harmonic distortion in the modulator's output spectrum since the outermost DAC mismatch errors are directly added with the input signal.

A mismatch error shaping technique has been introduced in [2]. Using such mismatch shaping techniques, the DAC mismatch-induced errors can be adequately suppressed in the signal bandwidth if the OSR is sufficiently high (say, 16 or higher). However, in broadband applications where a low OSR should be used, the mismatch shaping techniques become ineffective even for second-order mismatch shaping [3]. A combination of hardware-based and digital processing-based mismatch shaping technique (NS-DEM) is presented in [4]. An integrator is used in its shaping process which is prone to overflow. The occurrence of the overflow depends on the input signal frequency and amplitude. The lower the frequency and the higher the signal amplitude, the more frequently it overflows. When overflow occurs frequently, the noise shaping is affected and the performance of the ΣΔM will be degraded. Higher order mismatch shaping techniques also have significant latency. Using them in feedback path of ΣΔMs can cause instability when the sample frequency is high. Hence in such applications, the digital calibration and correction techniques can be used.

A calibration technique has been presented in [5]. It works by modulating each DAC element in turn with an out-of-bandwidth digital sequence and digitally measurement the magnitude of the resulting spectral components. This technique needs placing a notch at *fs/2* (calibration signal frequency) in noise transfer function (*NTF*) and a pole at $z = \alpha$ which affects the depth of the notch and allows for trade-off between SNR and the calibration time. This technique affects the design of modulator where itself has lots of parameters to meet.

A digital correction technique based on the correlation method has been proposed in [6]. It calculates the correlation between the output signal and each of thermometer codes of DAC input to estimate the error of each unit element. The power spectral density (PSD) of output signal contains filtered PSD of both input signal and quantization noise. These two spectral contents affect both convergence time and accuracy of correlation process. In fact, the correlation convergence time and accuracy depend on the input signal. This correction technique also uses 2^N (N is the number of bits of the quantizer) digital filters to filter all thermometer codes with error transfer function (*etf*) of modulator, and 2^N real-time adders for correlation to estimate the errors [7].

In this paper a novel purely digital technique is presented to eliminate mismatch errors of DAC. This proposed technique is accurate and has fast convergence time. It just requires a real time multiplier, a real time adder and an ordinary divider to estimate the error. The correction part is similar to [7].

In Section II the idea of correction is described. The proposed error calibration idea is presented in Sect. III. In this Section the hardware requirements of the proposed technique is also expressed. The simulation results are presented in Section IV.

II. THE CORRECTION TECHNIQUE

The block diagram of a multibit ΣΔ modulator along with its DAC's correction block is shown in Fig. 1. The modulator's output signal is given by:

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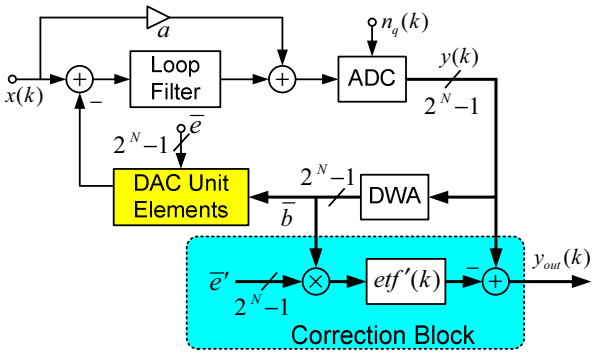

Figure 1. Linear model of a ΣΔM with its correction circuit. $\bar{b}$ is a vector of output thermometer codes of the quantizer, $etf'(k)$ is the estimation of $etf(k)$ and $\bar{e}'$ is the estimation of $\bar{e}$.

$$y(k)=x(k)\otimes stf(k)+n_q(k)\otimes ntf(k)+\ldots \left(\sum_{i=1}^{2^N-1} b_i(k).e_i\right)\otimes etf(k) \quad (1)$$

where $\otimes$ is the convolution operator, $n_q(k)$ is the quantization noise, $\bar{e}$ is a vector of the DAC's errors, and $stf(k)$, $ntf(k)$ and $etf(k)$ are the impulse responses of $y(k)$ to $x(k)$, $n_q(k)$ and $\bar{e}$, respectively. In Fig. 1, $\bar{b}$ is a vector of quantizer output thermometer codes, $etf'(k)$ and $\bar{e}'$ denote the estimation of $etf(k)$ and $\bar{e}$, respectively.

We assume that $\bar{e}$ is almost time-invariant. The first term in (1) is the desired output. The second term is the shaped quantization noise whose effect in the signal bandwidth is negligible. The third term is the DAC's error transferred to the output.

We have $\bar{b}$ and $etf'(k)$. Estimating $\bar{e}$, we would be able to reduce the 3rd term in (1). The error cannot be eliminated unless the $etf(k)$ and $\bar{e}$ be measured exactly. Estimation of $etf(k)$ is not so accurate. In a specific ΣΔM, $etf(k)$ is theoretically determined which differs from the real measurements because of the analog circuit non-idealities. In the proposed technique the error introduced in the 3rd term of (1) is reduced and then the remaining part of the error is shaped by DWA algorithm. Using DWA algorithm reduces the sensitivity of the final result to accuracy of estimation of $\bar{e}$ and $etf(k)$.

The corrected output signal is given by:

$$y_{out}(k)=y(k)-\left(\sum_{i=1}^{2^N-1} b_i(k)\,e_i'\right)\otimes etf'(k) \quad (2)$$

If $|ETF(e^{j\omega})|\approx 1$ in the signal bandwidth, it is not needed to implement $etf'(k)$.

III. The Proposed Calibration Technique

Fig. 2 shows the modulator of Fig. 1 with its calibration block. The calibration block is supposed to measure the unit element errors of DAC used in modulator. This DAC has 2^N-1 unit elements as usual and an additional one for the measurement process. The nominal value of elements is u and the real value of j^{th} element is $u_j = u\times(1+e_j)$, where e_j is the j^{th} unit element error. 2^N calibration phases are needed to measure the error of 2^N unit element of DAC. j^{th} calibration phase, φ_j, is allotted to measure the error of j^{th} unit element. Duration of each phase, T, is 2^{12} periods of the system clock, T_{CLK}; therefore the calibration time is $2^N\times 2^{12}\times T_{CLK}$.

There is no input signal during calibration time. In the proposed calibration technique a calibration signal, $X_C(k)$, is used which is the main system clock divided by $(P\times OSR)$. P is chosen such that the first harmonic of the calibration signal gets the place with lowest noise floor in output power spectrum density (PSD) of the modulator. In this manuscript, we choose $P=100$. During φ_j, the j^{th} element is excited by $X_C(k)$. The additional element takes the place of j^{th} element and the other elements works as usual.

The j^{th} element is excited by calibration signal, so the calibration signal is modulated by the error of j^{th} element, $(1+e_j)$, then it is transferred to the output by $ETF(z)$. Hence, the output signal is given by:

$$y_j(k)=x_C(k)\otimes etf(k).(1+e_j)+\ldots n_q(k)\otimes ntf(k)+\left(\sum_{i=1\,\&\,i\neq j}^{2^N} b_i(k).e_i\right)\otimes etf(k), \quad (3)$$

$$(j=1,2,\ldots,2^N)$$

where $y_j(k)$ is the output signal in the j^{th} calibration period.

The first term of (3) is the desired part which is used by arithmetic logic unit (ALU) to estimate the vector error of unit element errors, $\bar{e}'$. The second term is negligible in the signal bandwidth. The first harmonic of the calibration signal is used in the calibration as a low frequency signal. The DWA algorithm is employed to eliminate the effect of the third term.

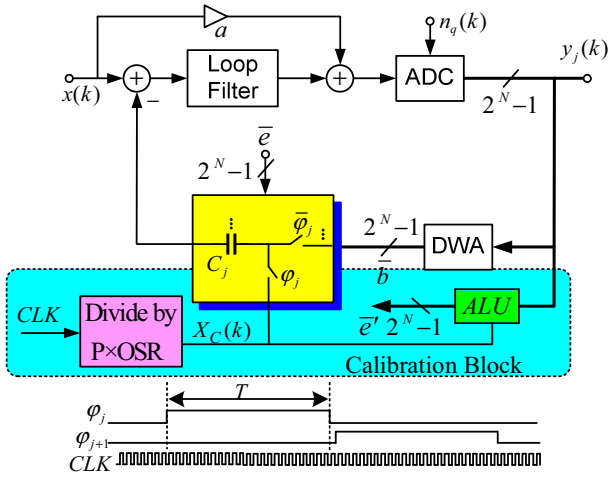

Figure 2. A ΣΔM with its calibration circuit.

The low frequency part of $y_j(k)$ is proportional to $(1+e_j)$ as shown in the first term of (3), where ideal transfer function of the j^{th} unit element of DAC is 1. Using the second order implementation of Goertzel algorithm [8] the amplitude of the tone at f = *(CLK-frequency) / (100× OSR)* is calculated in 2^{12} samples of $y_j(k)$. There would be 2^N different values ($a_1.a_2$ … , a_{2^N}) for different $Y_j(f)$ (j=1, 2…, 2^N). a_1, a_2 …, a_{2^N} are proportional to $(1+e_1)$, $(1+e_2)$ …, $(1+e_{2^N})$ respectively. The 2^N-th unit element of DAC is used as reference element for calibration purpose. It means that the errors of other elements are normalized by the error of the 2^N-th element as follows:

$$\frac{(1+e_j)}{(1+e_{2^N})}=\frac{a_j}{a_{2^N}}, \quad j=1,2...,2^N-1 \tag{4}$$

Assume $1+e_{2^N}\approx 1$,($e_{2^N}<<1$) and we can rewrite (4) as

$$e_j'=1-\frac{a_j}{a_{2^N}}, \quad j=1,2\ldots,2^N-1 \tag{5}$$

where e_j' is the estimated value of e_j.

The ALU unit shown in Fig. 2 encompasses the second order implementation of Goertzel algorithm and the logics needed to calculate the (5). In fact ALU processes the $y_j(k)$ and then estimates the e_j.

This calibration process could be a background one if the calibration frequency was out of signal bandwidth, but the large amount of out of band noise will reduce the calibration accuracy and increases the calibration time. The high frequency calibration signal also folds down high frequency noise to signal bandwidth because of circuit nonlinearity. Proper condition for the background calibration is introduced in [5] by placing a notch in *NTF(z)* out of signal band frequency, consequently there is not any noise in calibration signal frequency and the background calibration of errors are enough accurate. This out of signal band notch increases the amount of in-band noise and needs a change in design of modulator; however, modulator is designed for maximum SNR and SFDR, minimum power and stability requirements, therefore placing a notch in its *NTF(z)* complicates the design process. Also the background calibration process described in [5] reduces the dynamic range of modulator.

The proposed technique of this manuscript needs hardware to calculate the spectral amplitude of the first harmonic of the calibration signal in 2^{12} samples.

According to second order implementation of Geortzel algorithm, it needs a real multiplier and a real adder which work as fast as system clock. As shown in Fig. 1, *etf'*(k) should also be implemented. *etf'*(k) can be eliminated if $|ETF'(e^{jw})| \approx 1$ over the signal bandwidth. Simulation results are reported with $ETF'(z)=1$ (i.e. no digital filter is used). A clock generation unit is needed to make calibration phases, (φ_1 , φ_2 , … φ_{2^N}). Also, a logic circuit is responsible for implementation of DWA.

IV. Simulation Results

A single-loop 5th-order low pass ΣΔM with a 5-bit quantizer was simulated using MATLAB and SIMULINK to verify the validity of the proposed digital correction technique. 1.5% mismatch was introduced to unit elements of DAC. The input signal was a sinusoidal wave at -4.4 dBFS (DB Full Scale) with a frequency equal to *fs*/512 and an OSR of 8. Fig. 3 shows the modulator output spectrum in four different cases: real DAC, ideal DAC, real DAC with DWA algorithm and real DAC with the proposed correction technique. In Fig. 4 the SNDR versus the amplitude of input signal is shown when the ideal case, DWA algorithm and the proposed correction technique are separately utilized.

Table I summarizes the simulation results for different mismatch values among the DAC unit elements.

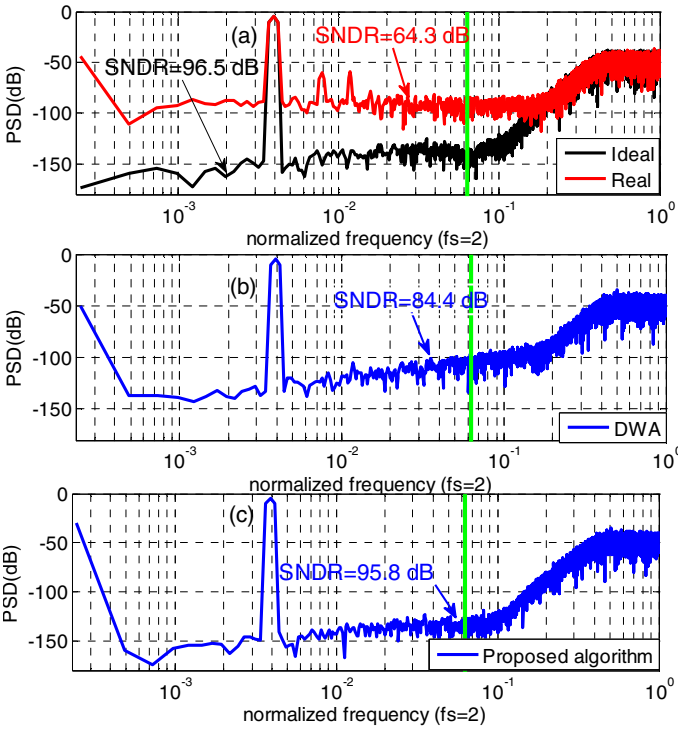

Figure 3. Output PSD with a) ideal DAC and real DAC, b) DWA DAC, c) Proposed technique, (%1.5 Mismatch).

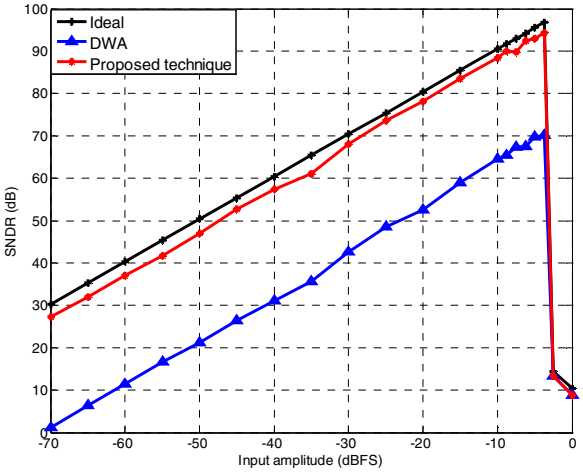

Figure 4. Simulated SNDR versus input signal amplitude.

TABLE I. PERFORMANCE COMPARISON (SNDR AND SFDR) OF OUTPUT SIGNAL

DAC type	SNDR (dB)		SFDR (dB)	
	0.3% mismatch	1.5% mismatch	0.3% mismatch	1.5% mismatch
Real DAC	82.7	64.3	89.1	69.3
DWA	93.0	84.4	105.8	98.9
Proposed technique	96.2	95.8	108.5	108.2
Ideal DAC	96.5		109.4	

As seen in Fig. 3, the performance of real DAC is very poor. Its PSD has large tones and its SNDR is 32.2 dB lower than the ideal one. For low OSR and large amount of mismatch, the DWA algorithm cannot shape the DAC noise to the out-of-band frequencies adequately. The SNDR achieved by the proposed correction technique is about 11.4 dB better than that resulted by DWA. Besides, the SNDR of the proposed technique is degraded only 0.7 dB with respect to the ideal DAC. The SNDR achieved by the proposed technique without combination with the DWA is about 91 dB.

V. CONCLUSION

A combination of DWA algorithm and a digital correction technique was presented to correct DAC mismatch errors in multibit ΣΔMs. The efficient, low cost, low power proposed technique corrects the main part of mismatch error in low OSR where shaping techniques cannot work properly. The remaining part is shaped by DWA. This combined technique eliminates the nonlinear effects of DAC. Its advantage over DWA is better seen when the OSR is low. The calibration part of this technique needs 2^{12+N} system clock periods and the measurement part is a foreground process where the correction process is a background one.

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