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Design of Electrical Stimulation Circuit in 180 nm/1.8 V Standard CMOS Process

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***Abstract*— This article presents an electrical stimulation circuit for use in implantable medical microsystems, which includes digital-to-analog converter, tuned cascade transistor structure, voltage level shifter circuit, and switches circuit for driving the stimulation current. In this research, DAC circuits and current directing switches are proposed in 180nm CMOS 1.8 V technology. Among the performed works, we can mention the increase of the current range up to 2.5 milliamperes and the stimulation voltage up to 12.6 volts to stimulate high-quality nerve tissues. In this context, a digital-to-analog converter circuit with a thermometer-coded structure has been designed and simulated with INL, DNL<0.5 LSB specifications, as well as SFDR=50.74 dB, SNDR=37.1 dB, and ENOB=5.87 Bits. Moreover the most critical parameter of the final system is the measured power consumption of 1.23 milliwatts.**

Keywords—Implantation system, electrical stimulation circuit, digital-to-analog converter (DAC), current driver, high voltage switches, low voltage technology, Monte Carlo analysis.

I. Introduction

The electrical stimulation unit consists of several subsystems, which include: a digital controller unit, digital-to-analog converter, high voltage switches, electrode, and voltage level shifter circuit [1-7]. In this project, the focus is on the optimal performance of the digital-to-analog converter and reducing the power consumption in the high-voltage switches responsible for stimulating the electrodes [8-10]. To reduce the power consumption in the electrical stimulation part, different ways have been investigated. One of these ways is how to stimulate the electrodes. In such a way that the electrodes are stimulated by a voltage applied to them, or by current injection, or by charge control [11]. Also, the way these stimulations and the shape of applied waveforms will have a significant effect on power consumption. The digital-to-analog converter circuit should be designed in such a way that it has a good resolution, and its output waveform, which is used to stimulate the electrodes, can also be easily controlled [12, 13].

The use of switches made with transistors in low voltage technology has made all the blocks of the electrical stimulation unit one-handed, and compared to high voltage technology, smaller dimensions, and lower cost are used. The use of high voltage switches in low voltage technology will bring the challenge that in order to disconnect and connect the switches, in order to protect the transistors from applying more than the permissible voltage on their drain-gate, we have to use structures to solve this problem. For this reason, circuits designed with these features need voltage-level shifter circuits, so that they can disconnect and connect high voltage switches during electrode stimulation cycles [2, 14].

This paper proposes an integrated electrical stimulation circuit implemented in 180 nm/1.8 V standard CMOS technology. The electrical stimulation circuit is designed to apply high voltage to nerve tissues, which makes this possible by using the structure of stack transistors. Also, the current stimulation method has been used for more precise control over nerve tissue stimulation. The proposed system operates at a voltage of 12.6 V and a maximum stimulation current of 2.5 mA.

The remains of the paper are arranged as follows. The second part presents the electrical stimulation circuit architecture and principles of operation. The results of the simulations, together with the prior art comparison, are described in Section III, and finally, the conclusions are reported in Section IV.

II. Proposed Stimulation Circuit

The most critical challenge of the electrical stimulation structure in implanting neural prostheses is directing the stimulation current through the switches to apply high voltage to the electrode. This can be done quickly in high-voltage technology. However in low-voltage technologies, due to the existing limitations, it has its challenges. The purpose of implementing the stimulation switches in low voltage technology in this project is to integrate the whole cochlear implant structure for its implementation in a low voltage technology and the more excellent compatibility of the switches with peripheral circuits [14]. Also, the maximum amplitude of the stimulation current and its waveform are of particular importance; therefore, it has been tried to design the proposed digital-to-analog converter circuit in such a way as to produce the optimal current waveform to reduce the power consumption in stimulating the electrodes.

The electrical stimulation circuit converts the information received through the electrode into nerve impulses in three ways: voltage stimulation, load stimulation, and current stimulation. According to the investigations, the best mode of electrical stimulation is the flow mode. Because, in this case, it is possible to control the stimulation method more precisely according to the patient's condition.

Fig. 1 shows the block diagram of the proposed structure. In this structure, a digital-to-analog converter circuit with a

coded thermometer structure, is controlled by a digital controller unit, produces an electrical stimulation current to be transferred to the electrode. This current is applied to the electrode through H-shaped bridge switches. Due to the high power required to excite the electrodes, the momentary application of this voltage to the DAC output will be problematic. To solve this problem, the adjusted cascade transistor structure is used, which provides high output impedance for DAC and prevents problems when high voltage is applied. H-bridge switches are used for biphasic stimulation of electrodes [2, 6, 15]. The advantage of this structure over the single-phase structure is that only one positive voltage source is used. The commands sent from the digital controller unit to control the switches in the form of voltage pulses, need to be transferred to higher voltage levels by an interface circuit called a voltage level shifter and then applied to the switches. However because the number of cascaded transistors is relatively large and need to be turned on and off, a bias circuit is used to turn them on.

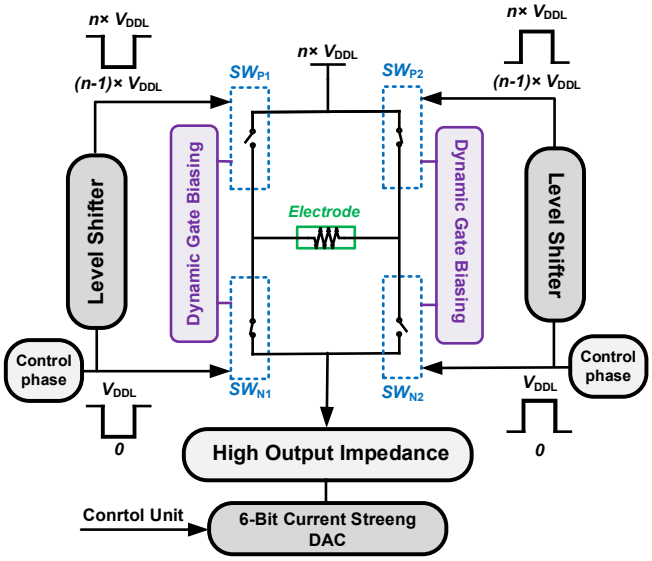

Fig. 1: Block diagram of the general structure of the electric drive circuit.

A. Thermometer-coded DAC

The work of the digital-to-analog converter is to receive a digital bit string and convert it into an analog output. In this structure, the output is the current, and the current size is the same for all cells, and when each current cell is turned on, the output current will increase by $\frac{I_{out}}{2^n}$. The advantage of this structure, in addition to uniformity, is the absence of glitches, and on the other hand, due to the tiny current of each cell, the size of the cells will be tiny. However since the number of required cells is 2^n, its total area will increase. Of course, due to the very high accuracy obtained from this structure, this limitation can be ignored to some extent.

One of the most essential advantages of this structure is that due to the simplicity of the current cells, which consist of only one NMOS transistor, the voltage changes in the source node of the transistor, which is connected to the ground is zero. There is no change in the current passing through it, which is shown in Fig. 2. Due to the measurement error, no two transistors are the same, and this effect is called mismatch. This effect in current source transistors can change their current and thus increase integral nonlinear error (INL). The relationship between the effect of mismatch on transistor current and determining the size of INL according to mismatch [16] is given in (2) and (3), respectively:

$$(\frac{\sigma_I}{I})^2 = \frac{1}{WL}(A_B{}^2 + \frac{4A_{VTH}{}^2}{(V_{gst})^2}) \quad (1)$$

$$INL = \frac{\sigma_I}{2I}\sqrt{2^N} \quad (2)$$

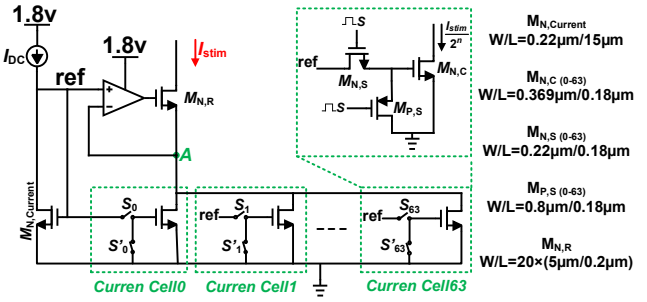

Fig. 2: Structure of Thermometer Coded DAC.

We aim is to design a digital-to-analog converter with a maximum output of 2.5 mA with a 6-bit resolution. So, the current source circuit for this structure must be able to provide the required current of each cell. Considering that the required resolution is 6 bits, the current of each cell will be calculated from the following equation:

$$I_{cell} = \frac{I_{out,\max}}{2^N} \xrightarrow{N=6\ ,\ I_{out,\max}=2.5mA} I_{cell} = \frac{2.5mA}{64} \approx 39\mu A \quad (3)$$

On the other hand, for a small current to pass through the current source transistor, we try to consider its current to be about 0.01 of the current of each cell.

This structure is designed based on the gain-increasing technique to increase the output impedance of the DAC. The gain-increasing technique increases power consumption. To reduce this problem, the op-amp in the feedback loop is turned off after biphasic stimulation. The output impedance can be calculated follows:

$$R_{out} = A.g_{m(M_{N,R})}.r_{0(M_{N,R})}.r_{0(M_{N,C})} \quad (4)$$

Where A is the operational amplifier gain.

B. High voltage current driver

The electrical model of the electrode is shown in Fig. 3. Implantable electrodes are modeled as a resistor in series with a capacitor, which is placed in parallel with a a huge resistor to prevent DC current from passing into the tissue. In this model, R_S=4 kΩ, R_{ct}=10 MΩ, C_{ct}=10 nF.

This structure allows biphasic stimulation of the electrode. In this way, first, an anodic phase stimulates the electrode by turning on the SW_{P1} and SW_{N2} switches. In the next phase, which is the cathode, to balance the charge in the electrode, by turning on the SW_{N1} and SW_{P2} switches, the current in the opposite direction of the previous phase stimulates the electrode. This is done to prevent the accumulation of charge, which can lead to the production of toxic chemicals or corrosion of the electrodes. After two phases are applied, a resting phase is applied through the simultaneous closing of the lower NMOS switches, which causes the two ends of the electrode to be shorted and discharge the remaining charge in it.

The advantage of this structure over unipolar structures is that it requires only one current source. Suppose the

unipolar circuits need two current sources for stimulation in the anodic and cathodic phases. Also, another advantage of the proposed circuit compared to similar structures is the reduction of the number of current directing switches.

Fig. 3 shows the proposed switches; each branch consists of a PMOS switch and an NMOS switch. To withstand the high voltage of V_{DDH} by standard transistors in 180 nm/1.8 V standard CMOS technology, a circuit with 14 transistors stacked together and able to withstand a supply voltage of $7\times V_{DDL}$ is used. NMOS transistors are implemented in deep N-wells, while PMOS transistors have local N-wells.

In this bias circuit, we need power supplies that are an integer multiple of V_{DDL}. These voltages are provided through a circuit that changes the pump charge voltage level. To control the highest PMOS transistor in the switches, a voltage level shifter circuit is used, which brings the zero to V_{DDL} input signal to $6\times V_{DDL}$ to $7\times V_{DDL}$.

In this bias circuit shown in Fig. 3, M_{A1-8} transistors act like resistance dividers. Therefore, the shown bias voltages are also shown as V_{B1-5} based on this design. Also M_{B1-6} and $M_{D1,2}$ transistors act as diodes. In this way, their body is connected to their drain in all NMOS and PMOS transistors. For example, when the voltage in the M_{B1} transistor reaches lower than $5\times V_{DDL}$, the diode turns on and returns to $5\times V_{DDL}$. This is true for other transistors with the same conditions (transistors shown in yellow). Now, when the transistor M_1 is turned on and the transistor M_{14} is turned off, the source of transistors M_{2-7} reaches $7\times V_{DDL}$, and the source of transistors M_{8-14} reaches $6\times V_{DDL}$, $5\times V_{DDL}$, $4\times V_{DDL}$, $3\times V_{DDL}$, $2\times V_{DDL}$ and V_{DDL}, respectively. Therefore, M_{A1-5} turn on and M_{A6-10} transistors turn off. This causes transistors M_{B1-4} to turn off and transistors M_{B5-8} to turn on. In the same way, the behavior of transistors is analyzed in the following classes. With these explanations, it can be seen that the voltage of the two ends of none of the transistors will exceed V_{DDL}.

The stack transistor switch has two functions: one is as a path for current to pass in the anodic and cathodic phases, connecting the current source to the electrode, and the other is as an isolation switch to protect the low-voltage digital-to-analog converter against the damage of the uniform high-voltage distribution. Will work To determine the size of the transistors in this structure, the size of each transistor that forms the output driver, considering that it is the main path of the switch, must be designed primarily, because they must pass a large current, up to 2.5 mA. Also, the dynamic bias circuit is designed and used to ensure that the voltage difference between the terminals of the switch stack transistors is maintained during the transition at 1.8 V. In addition to biasing the transistors related to the transfer switches, this circuit isolates the output of the stimulation circuit from the input signals It improves the efficiency of the circuit in this sense. Also, M_{A1-10}, M_{C1-6}, and $M_{E1,2}$ transistors should be selected so that the power of PMOS and NMOS transistors are almost the same. For this purpose, we consider the size of PMOS transistors to be

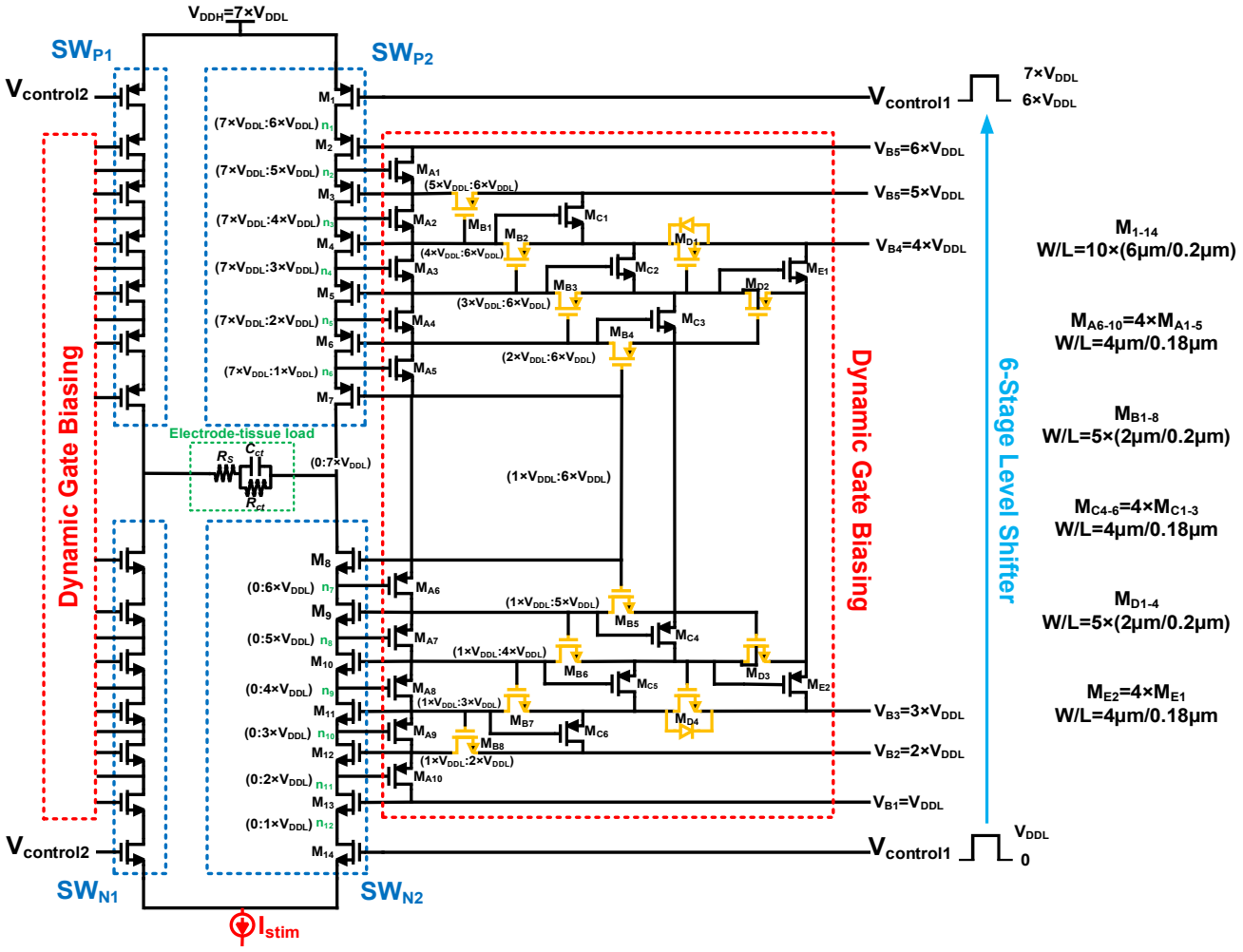

Fig. 3: Dynamic bias circuit structure of switches matrix.

about four times larger. Moreover, for M_{B1-8} and M_{D1-4} transistors, we choose relatively large sizes to increase the switching speed.

III. Simulation Results

First, In order to check the correct operation of the DAC, by applying a digital bit string with a rate of 10 Mpulse/sec to the DAC inputs, we have drawn its output current in terms of given bits, is shown in Fig. 4(a). As expected after the design, the output current range is 39 µA. That is, the least significant bit (LSB) of the desired converter circuit is 39 µA. Differential nonlinear error (DNL) and integral nonlinear error (INL) have calculated its using MATLAB software, which were obtained at room temperature conditions of DNL=0.203 LSB, and INL=0.260 LSB for the designed converter.

To check the converter's performance, Monte Carlo statistics analysis was performed on it. In 100 simulations with different mismatches, the maximum output current was measured and its histogram was drawn. As shown in Fig. 4(b), the maximum output current has reached 2.5 mA in most tests. Which indicates the correct operation of the designed circuit.

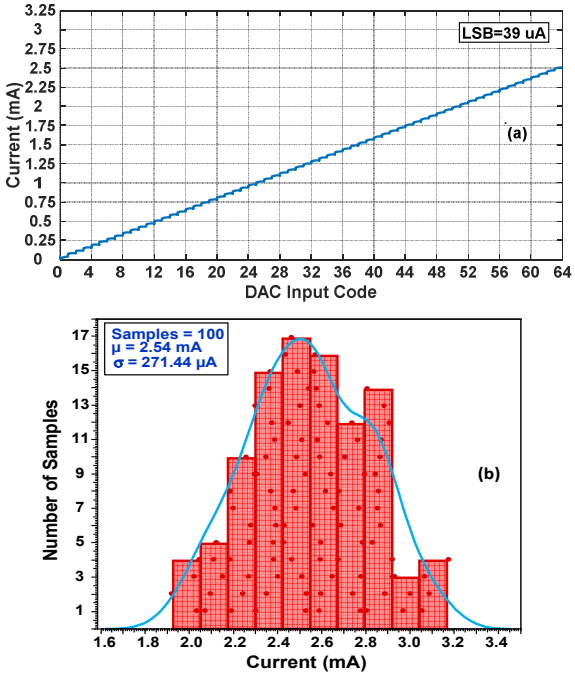

Fig. 4: (a) The anodic and cathodic currents versus DAC input code. (b) The histogram of the maximum amplitude of the output current in 100 different experiments with Monte Carlo analysis and considering mismatch.

Spurious free dynamic range (SFDR), signal-to-noise and distortion ratio (SNDR), and effective number of bits (ENOB) parameters have been calculated to investigate the dynamic behavior of the digital to analog converter. To calculate these parameters, a 6-bit ideal Flash analog-to-digital converter with thermometer-coded output is used. By applying a sinusoidal input with the input frequency f_{in}, from its output with the sampling frequency f_s and N points in the cycle number C, the sampled signals are applied to the DAC input, and the frequency response of the DAC is plotted, which is shown in Fig. 5. Also, Table I presents the simulation results in corners process.

$$f_{in} = \frac{f_{sample} \times Cycle}{N} \quad (5)$$

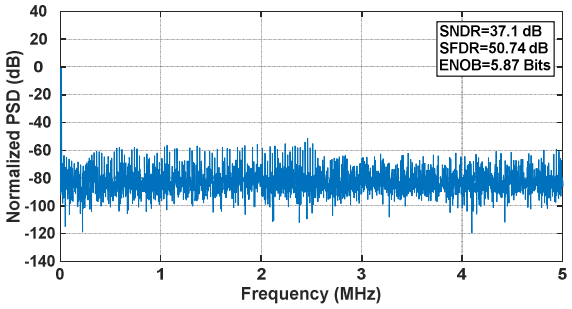

Fig. 5: SNDR and SFDR versus the input signal frequency.

Table I: Results of Simulating the DAC in Different Corners Process.

Parameters	FF(-40°C)	TT(27°C)	SS(85°C)
ENOB(Bits)	4.46	5.87	5.90
SNDR(dB)	28.63	37.1	37.2
SFDR(dB)	31.80	50.74	50.84

In the design of the high voltage electrical stimulation circuit using the accumulated transistors in the low voltage technology, it should be noted that the voltage difference between the bases of the transistors used in the circuit does not exceed the breakdown voltage of the parasitic well diode so that the transistor is not damaged. For this purpose, the terminals of the bulk transistors are connected to their sources to reduce the overdrive voltage of the stacked transistors. As mentioned before, in the structure of the high voltage electric stimulation circuit along with the dynamic gate biasing circuit, NMOS transistors are proposed in deep N-well so that their bulk can be connected to their source.

As shown in Fig. 6, the transient voltages of the drain-source, drain-gate, and gate-source terminals of M_7, M_8, M_{B6}, and M_{D3} transistors have been investigated. Some transistors have been investigated from the maximum to ensure the voltage applied to them. It can be seen that the amplitude of the applied voltage in each of the modes is lower than the breakdown voltage of the N-well diode. So it can be concluded that both the proposed bias circuit and the high voltage electrical stimulation circuit will have a good perform well in low voltage technology.

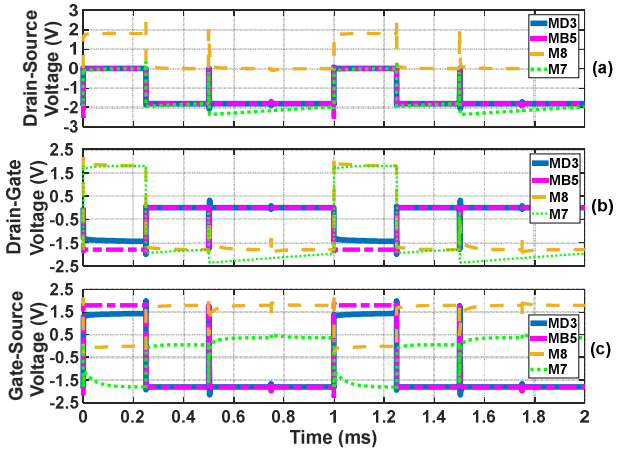

Fig. 6: (a) Drain-source voltage, (b) drain-gate voltage, and (c) gate-source voltage of transistors M_7, M_8, M_{B6}, and M_{D3}.

After the complete design of the circuit, the final simulations were performed on the electrical model of the

electrode. 250 µs are considered for each of the anodic and cathodic phases, which is a suitable timing according to the frequency of nerve stimulation. As shown in Fig. 7, the voltage difference between the two electrodes and the applied current for the electric stimulation of the electrode is, clearly showing the biphasic nature of the designed system.

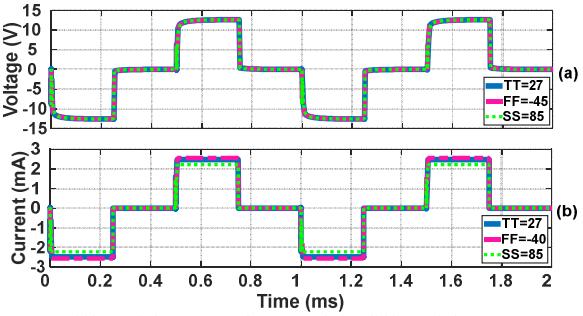

Fig. 7: (a) Differential output voltage, and (b) differential output current of the electrode in the final stimulation circuit.

Table II provides a summary and comparison of the performance between the proposed scheme and the prior art. The most important feature of the proposed design is the implementation of all circuits in 180nm CMOS 1.8V technology, which, in addition to the complete integration of the circuit, reduces the area and cost compared to high voltage technology. The excitation current range has increased, and without reducing DAC resolution, INL, and DNL nonlinearity errors have been reduced. The total power consumption has been improved according to the maximum current range and supply voltage of the excitation circuit.

TABLE II: PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS.

References	[2]	[10]	[17]	[18]	This Work
CMOS Process	0.18 µm High Voltage	0.18 µm High Voltage	0.18 µm High Voltage	0.18 µm low Voltage 3.3 V	0.18 µm low Voltage 1.8V
Supply Voltage (V)	9	12.8	6	12.5	12.6
Max stimulation current (mA)	0.5	0.992	1	2.08	2.5
Resolution DAC (bits)	6	5	6	5	6
INL	1.25	0.66	0.95	NA	0.260
DNL	0.16	0.2	0.5	NA	0.203
Power (mW)	0.572	NA	0.695	NA	1.23
Test	fabrication	simulation	fabrication	fabrication	simulation

IV. CONCLUSION

In this article, the general structure of the electrical stimulation system was first introduced, and its different parts were explained. These blocks included operational amplifier circuits, a digital-to-analog converter with thermometer-coded structure, and implantable electrostimulating switches. In the following, the proposed circuits for different system blocks were investigated for use in implantable microsystems in medicine. Parameters such as power consumption, the frequency response of op-amp and digital to analog converter, INL, and DNL errors and SNDR, SFDR, ENOB parameters for digital to analog converter and performance of high voltage switches in the stimulation of implantable electrodes were thoroughly investigated. Moreover, at the end, all the required simulations were reported with Cadence and MATLAB software to ensure the accuracy of the circuit performance.

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